GigaBit Logic

GaAs IC Data Book & Designer's Guide

May 1988

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IMPORTANT NOTICE

GigaBit Logic, Inc. reserves the right to make changes in the devices or the device specifications identified in this publication without notice. GigaBit advises its customers to obtain the latest version of device datasheets to verify, before placing orders, that the information being relied upon by the customer is current. The ADVANCE datasheets in this catalog provide specifications for products which are not yet complete or fully characterized. They provide design target information for customer planning purposes.

GigaBit Logic warrants performance of its IC products to current specifications in accordance with GigaBit's standard warranty terms and conditions.

Specifications contained in this data book supersede all data for these products published by GigaBit prior to May, 1988.

Welcome to the industry's (and world's!) first ***GaAs IC Data Book and Designer's Guide.*** Inside you will find complete, detailed information covering all of GigaBit's standard and ASIC product families as well as information describing foundry services, prototyping products, packaging, testing and reliability. The following two pages provide a product summary and table of contents. A complete listing of Sales Offices and Sales Representatives can be found at the end of this catalog.

STANDARD PRODUCT FAMILIES

GigaBit's standard 10G (logic), 12G (RAM), 14G (ROM) and 16G (analog and telecom) product families constitute the broadest range of catalog GaAs ICs in the industry. These devices are used by hundreds of customers worldwide because of their many advantages compared with silicon ICs, including:

- DC to 3 GHz clock and data rates
- <150 ps output transition times
- <100 to 150 ps loaded gate delays
- Radiation hardness approaching 10^8 rads
- Demonstrated high reliability stemming from a higher activation energy (1.4 eV) than silicon ICs
- 0°C to 85°C commercial operating temperature range and extended Mil. temp. range (-55°C to +125°C) or industrial temp. range (-40°C to +100°C) for some products
- Moderate power dissipation comparable to ECL 100K logic
- ECL and GaAs compatible I/O levels and inherent TTL compatible outputs

STANDARD CELL ASIC PRODUCTS

GigaBit's workstation-based standard cell library features an extensive array of pre-designed, pre-characterized cells optimized for 1 to 2 GHz speed at low power dissipation of 1 to 2 mW per gate. Loaded gate delays are typically 50 to 150 ps. The cell family is completely compatible with PicoLogic™ providing the user with the option to breadboard a design with PicoLogic™ and later convert to standard cells. Cell complexities vary from simple gates to 4-bit synchronous counters and phase/frequency comparators. Device complexities in excess of 5000 gates are supported. Complete packaging and test support is provided.

FOUNDRY SERVICES

GigaBit Logic is a world leader in advanced GaAs wafer processing and support services for foundry users, having processed over 100 custom circuit designs for a wide range of customers. Four fabrication processes are available to support a broad range of speed, power and functional device complexity requirements. Both D-MESFET and E/D-MESFET technologies are in production. Gate complexities of up to 3000 in production and up to 6000 for protoypes are achievable. Complete support services are provided.

PROTOYPING AND PRODUCTION SUPPORT PRODUCTS

To help designers apply GigaBit ICs easily, inexpensively, quickly and successfully the first time, GigaBit offers the 90GKIT HIgh Speed Prototyping Kit along with a high speed socket, heatsinks and component kits for use with the prototyping board in the 90GKIT. Virtually all design efforts can benefit through time and cost savings when these products are used in the breadboarding and proof of concept phases.

OUR COMMITMENT TO YOU

GigaBit Logic has only one business - GaAs integrated circuits. We are the oldest and most experienced commercial market GaAs IC maker having incorporated in 1981. We are committed to providing customers with the broadest range of standard, semi-custom and full custom ICs including digital, analog and interface circuits. We are committed to manufacturing highly reliable circuits in a controlled, documented environment. Our reputation has been established through execution of a commitment to deliver our products on time, in volume and at prices that reflect our high yields, increasing volume and continually improving manufacturing processes. Most importantly, we are committed to providing the highest level of support and service to our customers - who we recognize as the cornerstone of our business.

TABLE OF CONTENTS

SECTION 1: 10G PICOLOGIC™ FAMILY PRODUCTS

SECTION 2: 12G NANORAM & 14G NANOROM FAMILY PRODUCTS

SECTION 3: 16G FAMILY PRODUCTS

*See Section 10 for description of package identifier

10G PICOLOGIC™ FAMILY PRODUCTS

TABLE OF CONTENTS

10G PicoLogic™ Family Electrical Characteristics

ABSOLUTE MAXIMUM RATINGS

(Beyond which useful life may be impaired) (Notes 1, 4)

SYMBOL	PARAMETER	ABSOLUTE MAXIMUM RATINGS	NOTES
TSTOR	Storage Temperature	- 65 °C to + 150 °C	
TJ	Junction Temperature	- 55 °C to + 150 °C	
TC	Case Temperature Under Bias	- 55 °C to + 125 °C	2
VDDO	Output Driver Supply Voltage	-0.8 V to + 1.0 V	
VCC	TTL Supply Voltage	0 V to +7.0 V	
VSS	Supply Voltage	- 4.0 V to + 0.5 V	
VEE	Supply Voltage	- 7.0 V to VSS + 0.5 V	
VIN	Voltage Applied to Any Input; Continuous VSS = - 3.4 V, VEE = - 5.2 V	- 4.0 V to + 0.5 V	
I IN	Current Into Any Input; Continuous	- 0.5 mA to 1.0 mA	
VOUT	Voltage Applied to Any Output	-4.0V to + 7.0 V	3
IOUT	Current From Any Output; Continuous	-100 mA	
PD	Power Dissipation Per Output POUT = (VDDO-VOUT) x IOUT	100 mW	
VBB	Threshold Reference Input Voltage	-4.0V to +0.5V	
IBB	Input current (from interfacing family)	-0.5 mA to +1.0 mA	
VTTC	VDDO Internal Decoupling Cap. Return	-6.0 V to VDDO	
VTT	Load Termination Supply	-6.0 V to VDDO + 6.0 V	
VDCH	Output Driver Clamp Voltage	VSS to VDDO	
IDCH	Output Driver Clamp Current	-20 mA	5
VICH	Input Clamp High Voltage	-2.0 V to VDDL	
IICH	Input Clamp High Current	-20 mA	
VICL	Input Clamp Low Voltage	VSS to -0.4 V	
IICL	Input Clamp Low Current	20 mA	
VTRIM	Threshold Adjust Voltage	-7.0 V to VDDL	

Notes:
1. All voltages specified with VDDL defined as 0 V. Positive current is defined as current into the device.
2. TC is measured at case top for 40 and 68 pin packages and at case bottom for 36 pin packages.
3. Subject to IOUT and power dissipation limitations.
4. Power supply sequencing is not necessary, but since the VEE supply is used to bias off the normally-on depletion mode transistors, sustained (>5 secs.) application of VSS in the absence of VEE may result in excessive power dissipation and damage to the device. If VEE is heavily loaded, causing it to be held near ground potential, the use of a power diode between VEE and VSS is recommended to avoid passing excessive current through internal diodes used as decoupling capacitors.
5. Subject to IDCH and power dissipation limits.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN	NOM	MAX	UNITS	NOTES
TC	Case Operating Temperature (Std. parts)	0	25	85	°C	1
TCK	Case Operating Temperature ("K" suffix)	-40		100	°C	
TCM	Case Operating Temperature ("M" suffix)	-55		125	°C	
VDDL	Logic Supply Voltage		Gnd		V	
VDDO	Output Driver Supply Voltage	-0.8	Gnd	1.0	V	
VCC	TTL Supply Voltage	4.75	5.0	5.25	V	
VSS	Supply Voltage	- 3.5	- 3.4	- 3.3	V	
VEE	Supply Voltage	- 5.5	- 5.2	- 5.1	V	
VTTC	VDDO Internal Decoupling Return	VSS	VTT	VDDO	V	
VTT	Load Termination Supply Voltage	VSS	- 2.0	- 2.0	V	2
VDCH	Output Driver Clamp Voltage	-2.5	-2.0	VDDO	V	3
RLOAD	Output Termination Load Resistance	25	50	100	Ω	2
VTRIM	Input Threshold Adjust Voltage	VEE-1	VEE	VEE+1	V	

Notes:
1. Tcase measured at case top. **User attention to device thermal management is recommended.** See GigaBit Application Note 3, "Thermal Management of PicoLogic and NanoRam GaAs Digital IC Families" for a complete discussion of all aspects of device thermal management. Heatsinks are available from GigaBit.
2. The RLOAD and VTT combination used is subject to maximum output current and power restrictions.
3. VDCH is not used when driving GaAs logic but may be used to limit VOH when driving ECL. See App. Note 4.

DC CHARACTERISTICS (Notes 1,2,5,8)

Tc = Per datasheet min. and max., VSS = -3.5V to -3.3V, VEE = -5.5V to -5.1V, VDDL=VDDO = Gnd., unless otherwise indicated.

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	TEST CONDITIONS	NOTES
VOH	Output Voltage High	-0.8	-0.4	-0.3	V		
VOL	Output Voltage Low	-2.0	-1.9	- 1.8	V		
IOH	Output Current High		-70	-60	mA	VOH = -0.8V	3
VIH	Input Voltage High	-1.0		VDDL	V		
VIL	Input Voltage Low	VSS		- 1.6	V		6
I IN	Input Current	-500	100	500	µA	VIN = -1.0V to -1.6V	
VBBS	Threshold Reference Voltage	-1.40		-1.05	V		4
IBB	Reference Input Current		30	50	µA/Input	VBB = -1.3 V	
PD	Power Dissipation	----	----	----			7

Notes:
1. These characteristics are applicable from DC to 500 MHz.
2. Test conditions unless otherwise indicated: VBB = -1.3V, VTT = -2.0V, VTTC = VTT, Rload = 50Ω to VTT, VDCH = VDDO, VICH = VDDL, VICL = VSS, VTRIM = VEE.
3. IOH is the available source follower output current at VOH = -0.8V.
4. 40Ω source impedance. ΔVBBS/ΔTemp = +0.6 mV/°C; ΔVBBS/ΔVSS = +0.2 mV/mV. VBBS = -1.2 V is recommended for optimum noise immunity at max. operating speeds. Most 10G PicoLogic devices presently have a nominal -1.3 V VBBS threshold reference voltage output. Those devices with a -1.2 V nominal VBBS level are noted in the individual datasheets.
5. See specific datasheets for deviations, if any, to these characteristics.
6. Inputs may be tied to VSS to establish a fixed logic low level. However, AC performance may be degraded if VIL is < -2.0 V.
7. PD is specified in the individual datasheets and is measured at nominal supply voltages and 50% duty cycle, exclusive of VDDO output source follower power (typically 15 mW per loaded output) and output clamp power (if any).
8. For sequential parts, clock input edge rate is ≤ 2ns.

NOTE TO 10G FAMILY ELECTRICAL CHARACTERISTICS

These electrical characteristics tables are applicable to all devices in the 10G PicoLogic™ family of GaAs digital ICs only. 12G, 14G and 16G family circuits share many common electrical characteristics with the 10G family but are different enough to warrant separate specification of electrical characteristics in their individual datasheets contained in this publication.

The electrical characteristics of specific 10G products, which differ from the family characteristics above, are contained in the individual 10G product datasheets contained in this publication.

GigaBit Logic reserves the right to make changes to products and specifications without notice.

GigaBit Logic **10G000A**

Quad 3 Input NOR Gate

320 ps Gate Delay

10G PicoLogic™ Family

DISTINCTIVE CAPABILITIES

- 320 ps max. propagation delay
- Output rise and fall times of 150 ps
- 0°C to +85°C operating temperature range
- 10G PicoLogic compatible inputs and outputs
- VBB reference voltage for improved threshold tracking over temperature and power supply variation
- On-chip VBBS (-1.3V) reference voltage
- Supports a wide range of load resistor and termination voltage combinations
- Wire-OR output capability
- Available in flatpack, leadless chip carrier (LCC) or dice form
- Packages contain internal decoupling capacitors for optimum high frequency performance

APPLICATIONS

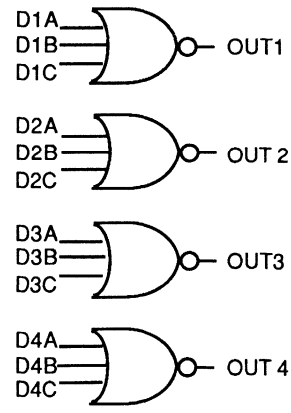
- Logic functions
- Precision gating/strobing
- Data distribution
- Digital multiplexing
- High speed TTL/CMOS to10G/ECL and 10G to TTL/CMOS translation ability

FUNCTIONAL DESCRIPTION

The10G000A is an ultra fast quad 3 input NOR gate featuring a maximum propagation delay of 320 ps for packaged parts. It offers a typical speed four times faster than equivalent ECL NOR gates. The10G000A is ideally suited for use in high performance systems requiring improved throughput, reduced signal skew and increased timing margin. It can also drive and be driven from CMOS and TTL gates, providing the user a high speed TTL/CMOS to10G/ECL translation capability.

For compatibility with other high speed logic families, the 10G000A features the PicoLogic™ family standard VBB input. This input allows the 10G000A's threshold voltage to be controlled by the driving logic family. Therefore, mismatches in threshold level due to temperature and power supply vaiations can be compensated, providing high system noise inmunity. An on-chip threshold voltage output (pin VBBS) is also provided. VBBS must be strapped to the VBB input when PicoLogic™ is used to drive the 10G000A. The 10G000A has input clamps VICH and VICL. When connected to -1.3V, these internally truncate an overdriven sine wave input signal to a square wave, thus allowing inputs to be driven with faster rise and fall times. When not used, the input clamps should be connected to VICL = VSS and VICH = VDDO for transient protection.

BLOCK DIAGRAM



10G000A ORDERING INFORMATION

PACKAGE TYPE	DELAY (Max @ 25°C)	
	320 ps	390 ps
40 I/O C-Leaded CC 40 I/O Leadless CC Dice	10G000A-C 10G000A-L	10G000A-4C 10G000A-4L 10G000A-4X

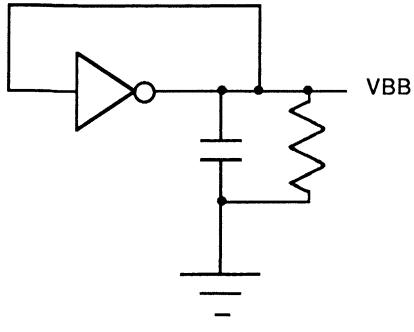
FUNCTIONAL DESCRIPTION (Continued)

A major design goal of the PicoLogic™ family is to provide full interface capability to other logic families without sacrificing noise immunity. Since each family exhibits differing input threshold sensitivity to temperature and power supply variations, it is necessary to "tell" the PicoLogic™ device which family it is interfacing to.This can easily be accomplished via the VBB input pin. A nominal -1.3V reference voltage is applied to the VBB pin to cause the PicoLogic™ threshold to equal and track the threshold of the interfacing logic family.

When the 10G000A is interfaced with other PicoLogic™ parts, VBB may be strapped to the VBBS output pin. The internal VBBS circuit generates a nominal -1.3V reference output with only a 17% VSS sensitiviity. It thus provides a convenient reference supply which can be used over the commercial temperature range of 0°C to + 85°C for a GaAs to GaAs interface.

If VBBS is not supplied by the other logic family, it may be generated by connecting an inverting device output to its input as illustrated below.

Generating the Switching Threshold (VBB) Reference Level from Interfacing Logic.



PIN DESCRIPTIONS

D1-4	Data inputs
OUT1-4	Outputs
VDDO	Output driver ground (0V)
VDDL	Internal logic ground (0V)
VSS	-3.4V power supply
VEE	-5.2V power supply
VTTC	VDDO internal decoupling capacitor return. VTTC is brought into the 10G000A package as the AC return lead for the internal VDDO output driver decoupling capacitor. It is not brought onto the 10G000A die.VTTC is typically equal to VTT (nominally -2.0V).
VDCH	Output driver clamp supply.When VDCH is connected to VTT = -2.0V the output driver high level is limited to approximately -0.6V, thus providing ECL output compatibility. When driving other GaAs devices, VDCH is typically left unconnected.
VICH,VICL	Input protection clamp supply. When connected to -1.3V, these allow an over-driven sine wave input signal to be truncated to a square wave, thus allowing inputs to be driven with faster rise and fall times. When not used, the input clamps should be connected to VICL =VSS and VICH =VDDO for transient protection.
VBB	GaAs threshold reference input voltage (nominal -1.3V). Provided to allow direct tracking of another family's reference voltage. Connect to VBBS for PicoLogic™ interface. When interfacing to other GaAs families, connect to that family's reference voltage.
VBBS	GaAs threshold reference voltage. Nominally equal to -1.3V with a 40Ω source impedance. Connect to VBB when interfacing with PicoLogic™.

TRUTH TABLE

INPUTS			OUTPUT
A	B	C	
H	X	X	L
X	H	X	L
X	X	H	L
L	L	L	H

X = Don't care input

DC CHARACTERISTICS

TC = 0 °C to + 85 °C, VSS = -3.5V to -3.3V, VEE = -5.5V to -5.1V, VDDL=VDDO = 0V, unless otherwise indicated.

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	TEST CONDITIONS
VIH	Input Voltage High	-0.7		VDDL	V	
VOH	Output Voltage High	-0.7			V	
VIL	Input Voltage Low	VSS		-1.8 V	V	
IIN	Input Current	-100	120	400	µA	VIN: -0.7 V to -1.8 V
ISS	Power Supply Current	-180	-110		mA	
IEE	Power Supply Current	-45	-25		mA	
PD	Power Dissipation		500	875	mW	

Note: The remaining DC Characteristics are specified in the 10G PicoLogic™ Family Electrical Characteristics Table at the beginning of this section. This table notes parameter deviations to Family Characteristics and provides specific supplementary characteristics only.

10G000A AC CHARACTERISTICS (Note 1,3)

VSS = -3.5V to -3.3V, VEE = -5.5V to -5.1V, VDDL=VDDO = 0V, unless otherwise indicated.

SYMBOL	PARAMETER	Tc= 0°C		Tc = +25°C			Tc= +85°C		UNITS	NOTES
		MIN	MAX	MIN	TYP	MAX	MIN	MAX		
T1	Prop. Delay, Low to High		330		300	320		350	ps	
T2	Prop. Delay, High to Low		330		300	320		350	ps	
T3	Output Rise Time		175		150	175		190	ps	2
T4	Output Fall Time		175		150	175		190	ps	2

10G000A-4 AC CHARACTERISTICS (Note 1,3)

VSS = -3.5V to -3.3V, VEE = -5.5V to -5.1V, VDDL=VDDO = 0V, unless otherwise indicated.

SYMBOL	PARAMETER	Tc= 0°C		Tc = +25°C			Tc= +85°C		UNITS	NOTES
		MIN	MAX	MIN	TYP	MAX	MIN	MAX		
T1	Prop. Delay, Low to High		390		360	390		410	ps	
T2	Prop. Delay, High to Low		390		360	390		410	ps	
T3	Output Rise Time		215		190	215		230	ps	2
T4	Output Fall Time		215		190	215		230	ps	2

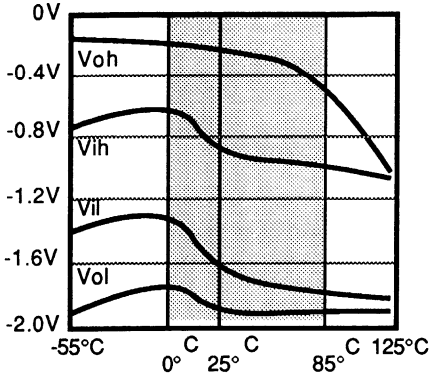
Note 1. Test conditions (unless otherwise indicated) :

VBB = -1.3 VICH = 0V VIH = -0.7V
VTT = -2.0V VICL = VSS VIL = -1.8V
VTTC = VTT VDCH = -2.0V VOH = -0.7V
RLOAD = 50Ω to -2.0V VOL = -1.8V
Input signal rise and fall time ≤ 150 ps

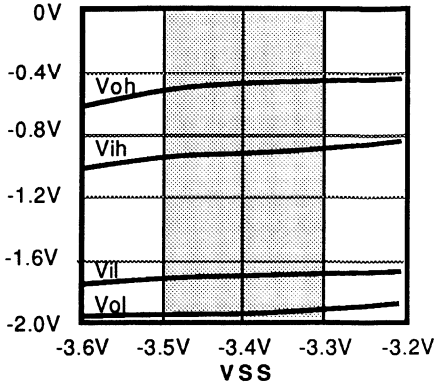
2. Rise and fall times are measured between 20% and 80% points.
3. All values of parameters T1 and T2 are 30 ps less for the "L36" and "F" packages.

TYPICAL PERFORMANCE CHARACTERISTICS

Vin & Vout vs. Temperature

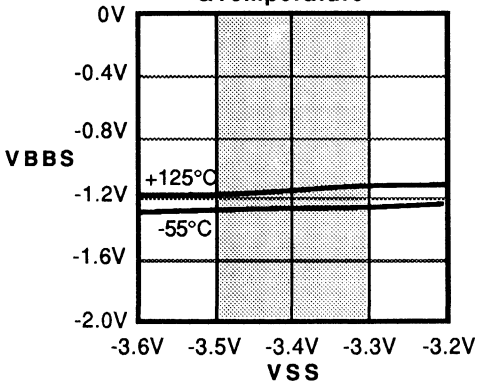


Vin & Vout vs. VSS

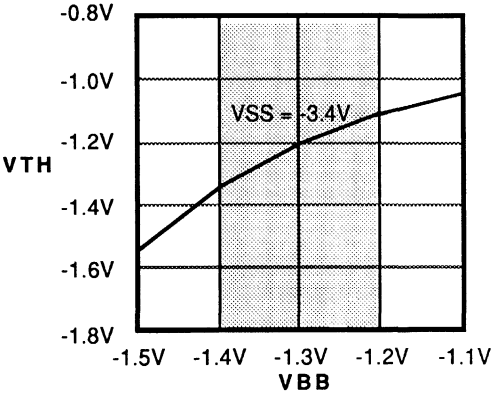


VBB = -1.3V. The VOH and VOL curves result when the inputs are driven from -0.6V to -1.8V. The VIH and VIL curves shown result in output levels from -0.6V to -1.8V.

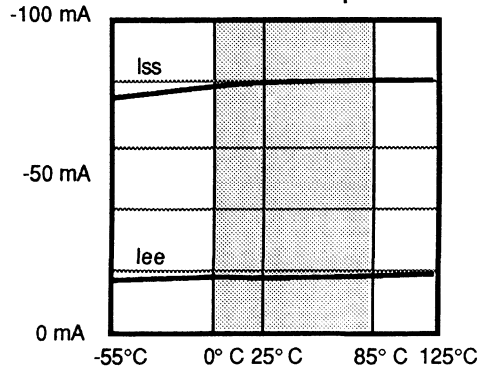
VBBS vs VSS &Temperature



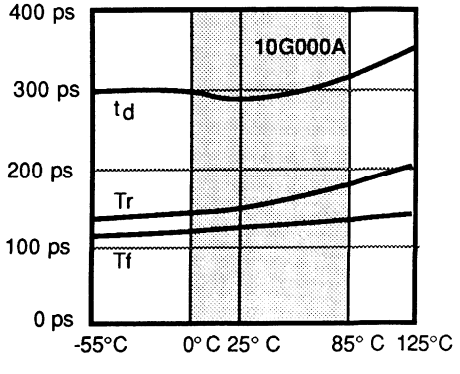
Input Threshold vs VBB



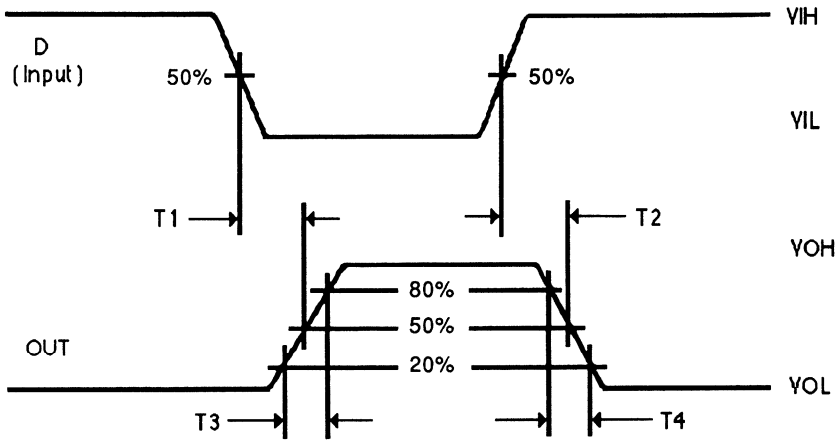
ISS & IEE vs. Temperature



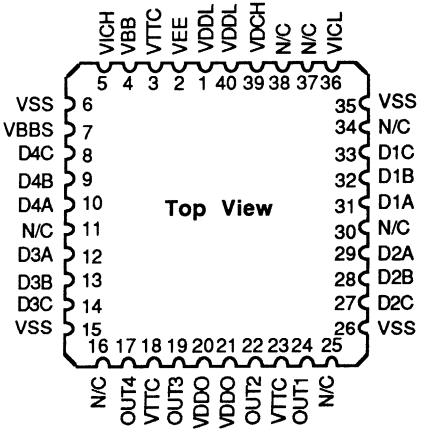
Prop. Delay and Rise and Fall Times vs. Temperature



SWITCHING WAVEFORMS



PIN FUNCTIONS - PACKAGE TYPES "L" AND "C"



GBL GigaBit Logic **10G001**

Quad 2 Input NOR Gate

320 ps Gate Delay

10G PicoLogic™ Family

DISTINCTIVE CAPABILITIES

- 320 ps max propagation delay
- Output rise and fall times of 150 ps
- 0°C to +85°C operating temperature range
- 10G PicoLogic compatible inputs and outputs
- VBB reference voltage for improved threshold tracking over temperature and power supply variation
- On-chip VBBS (-1.3V) reference voltage
- Supports a wide range of load resistor and termination voltage combinations
- Wire-OR output capability
- Available in flatpack, leadless chip carrier (LCC) or dice form
- Packages contain internal decoupling capacitors for optimum high frequency performance

APPLICATIONS

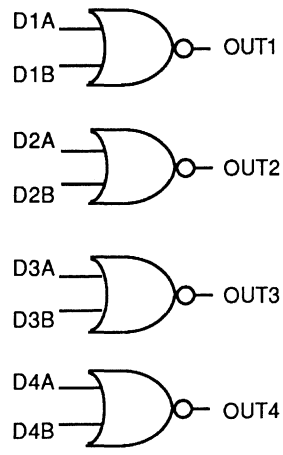
- Logic functions
- Precision gating/strobing
- Data distribution
- Digital multiplexing
- High speed TTL/CMOS to10G/ECL and 10G to TTL/CMOS translation ability

FUNCTIONAL DESCRIPTION

The10G001 is an ultra fast quad 2 input NOR gate featuring a maximum propagation delay of 320 ps for packaged parts. It offers a typical speed four times faster than equivalent ECL NOR gates. The10G001 is ideally suited for use in high performance systems requiring improved throughput, reduced signal skew and increased timing margin. It can also drive and be driven from CMOS and TTL gates, providing the user a high speed TTL/CMOS to10G/ECL translation capability.

For compatibility with other high speed logic families, the 10G001 features the PicoLogic™ family standard VBB input. This input allows the 10G001's threshold voltage to be controlled by the driving logic family. Therefore, mismatches in threshold level due to temperature and power supply variations can be compensated, providing high system noise inmunity. An on-chip threshold voltage ouput (pin VBBS) is also provided. VBBS must be strapped to the VBB input when PicoLogic™ is used to drive the 10G001. The 10G001 has input clamps VICH and VICL. When connected to -1.3V, these internally truncate an overdriven sine wave input signal to a square wave, thus allowing inputs to be driven with faster rise and fall times. When not used, the input clamps should be connected to VICL = VSS and VICH = VDDO for transient protection.

BLOCK DIAGRAM



10G001 ORDERING INFORMATION

PACKAGE TYPE	DELAY (Max @ 25°C)	
	320 ps	390 ps
40 I/O C-Leaded CC	10G001-C	10G001-4C
40 I/O Leadless CC	10G001-L	10G001-4L
Dice		10G001-4X

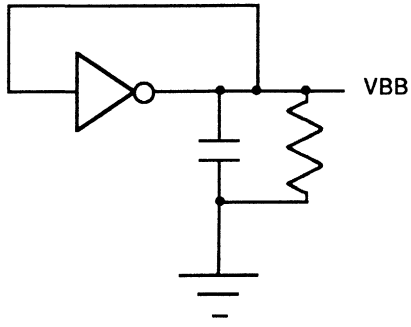
FUNCTIONAL DESCRIPTION (Continued)

A major design goal of the PicoLogic family is to provide full interface capability to other logic families without sacrificing noise immunity. Since each family exhibits differing input threshold sensitivity to temperature and power supply variations, it is necessary to "tell" the PicoLogic device which family it is interfacing to.This can easily be accomplished via the VBB input pin. A nominal -1.3V reference voltage is applied to the VBB pin to cause the PicoLogic threshold to equal and track the threshold of the interfacing logic family.

When the 10G001 is interfaced with other PicoLogic parts, VBB may be strapped to the VBBS output pin. The internal VBBS circuit generates a nominal -1.3V reference output with only a 17% VSS sensitiviity. It thus provides a convenient reference supply which can be used over the commercial temperature range of 0°C to + 85°C for a GaAs to GaAs interface.

If VBBS is not supplied by the other logic family, it may be generated by connecting an inverting device output to its input as illustrated below.

Generating the Switching Threshold (VBB) Reference Level from Interfacing Logic.



PIN DESCRIPTIONS

D1-4	Data inputs
OUT1-4	Outputs
VDDO	Output driver ground (0V)
VDDL	Internal logic ground (0V)
VSS	-3.4V power supply
VEE	-5.2V power supply
VTTC	VDDO internal decoupling capacitor return. VTTC is brought into the 10G001 package as the AC return lead for the internal VDDO output driver decoupling capacitor. It is not brought onto the 10G001 die.VTTC is typically equal to VTT (nominally -2.0V).
VDCH	Output driver clamp supply.When VDCH is connected to VTT = -2.0V the output driver high level is limited to approximately -0.6V, thus providing ECL output compatibility. When driving other GaAs devices, VDCH is typically left unconnected.
VICH,VICL	Input protection clamp supply. When connected to -1.3V, these allow an over-driven sine wave input signal to be truncated to a square wave, thus allowing inputs to be driven with faster rise and fall times. When not used, the input clamps should be connected to VICL =VSS and VICH =VDDO for transient protection.
VBB	GaAs threshold reference input voltage (nominal -1.3V). Provided to allow direct tracking of another family's reference voltage. Connect to VBBS for PicoLogic interface. When interfacing to other GaAs families, connect to that family's reference voltage.
VBBS	GaAs threshold reference voltage. Nominally equal to -1.3V with a 40Ω source impedance. Connect to VBB when interfacing with PicoLogic.

TRUTH TABLE

A	B	OUTPUT
H	X	L
X	H	L
L	L	H

X = Don't care input

DC CHARACTERISTICS

TC = 0 °C to + 85 °C, VSS = -3.5V to -3.3V, VEE = -5.5V to -5.1V, VDDL=VDDO = 0V, unless otherwise indicated.

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	TEST CONDITIONS
VIH	Input Voltage High	- 0.7		VDDL	V	
VOH	Output Voltage High	-0.7			V	
VIL	Input Voltage Low	VSS		- 1.8	V	
IIN	Input Current	-100	120	400	µA	VIN =-0.7V to -1.8V
ISS	Power Supply Current	-180	-110		mA	
IEE	Power Supply Current	- 45	-25		mA	
PD	Power Dissipation		500	875	mW	

NOTE: The remaining DC Characteristics are specified in the 10G PicoLogic™ Family Electrical Characteristics Table at the beginning of this section. This table notes parameter deviations to Family Characteristics and provides device specific supplementary characteristics only.

10G001 AC CHARACTERISTICS (Note 1,3)

VSS = -3.5V to -3.3V, VEE = -5.5V to -5.1V, VDDL=VDDO = 0V, unless otherwise indicated.

SYMBOL	PARAMETER	Tc= 0°C		Tc = +25°C			Tc= +85°C		UNITS	NOTES
		MIN	MAX	MIN	TYP	MAX	MIN	MAX		
T1	Prop. Delay, Low to High		330		300	320		350	ps	
T2	Prop. Delay, High to Low		330		300	320		350	ps	
T3	Output Rise Time		175		150	175		190	ps	2
T4	Output Fall Time		175		150	175		190	ps	2

10G001-4 AC CHARACTERISTICS (Note 1,3)

VSS = -3.5V to -3.3V, VEE = -5.5V to -5.1V, VDDL=VDDO = 0V, unless otherwise indicated.

SYMBOL	PARAMETER	Tc= 0°C		Tc = +25°C			Tc= +85°C		UNITS	NOTES
		MIN	MAX	MIN	TYP	MAX	MIN	MAX		
T1	Prop. Delay, Low to High		390		360	390		410	ps	
T2	Prop. Delay, High to Low		390		360	390		410	ps	
T3	Output Rise Time		215		190	215		230	ps	2
T4	Output Fall Time		215		190	215		230	ps	2

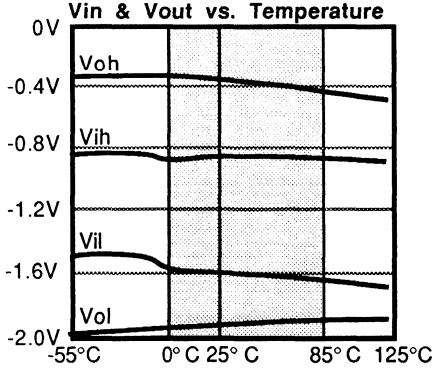
Note 1. Test conditions (unless otherwise indicated) :

VBB = -1.3 V VICH = 0V VIH = -0.7V
VTT = -2.0V VICL = VSS VIL = -1.8V
VTTC = VTT VDCH = -2.0V VOH = -0.7V
RLOAD = 50Ω to -2.0V VOL = -1.8V
Input signal rise and fall time ≤ 150 ps

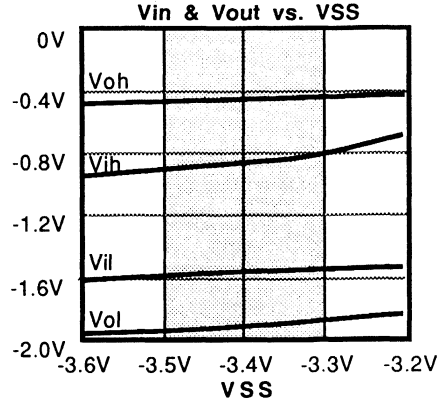
2. Rise and fall times are measured between 20% and 80% points.
3. All values of parameters T1 and T2 are 30 ps less for the "L36" and "F" packages.

TYPICAL PERFORMANCE CHARACTERISTICS

Vin & Vout vs. Temperature

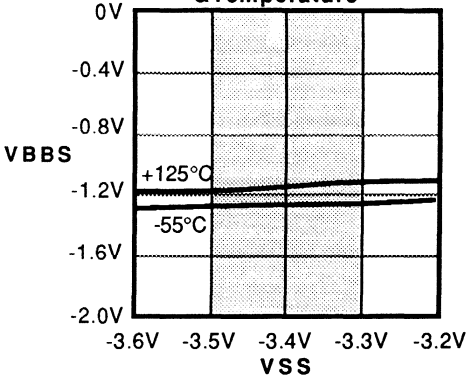


Vin & Vout vs. VSS

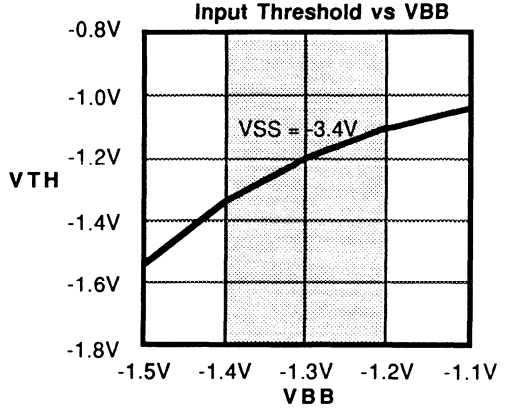


VBB = -1.3V. The VOH and VOL curves result when the inputs are driven from -0.7V to -1.8V. The VIH and VIL curves shown result in output levels from -0.7V to -1.8V.

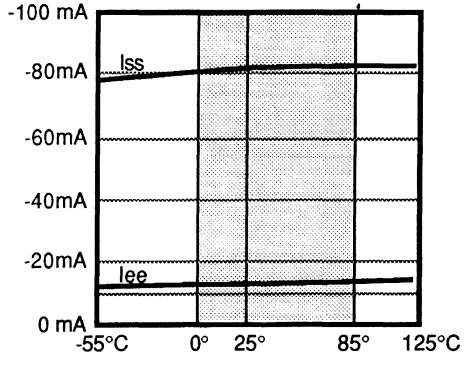
VBBS vs VSS &Temperature



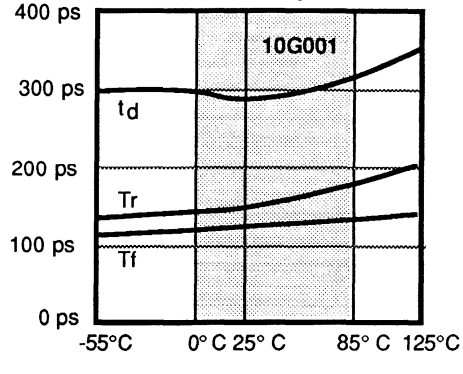
Input Threshold vs VBB



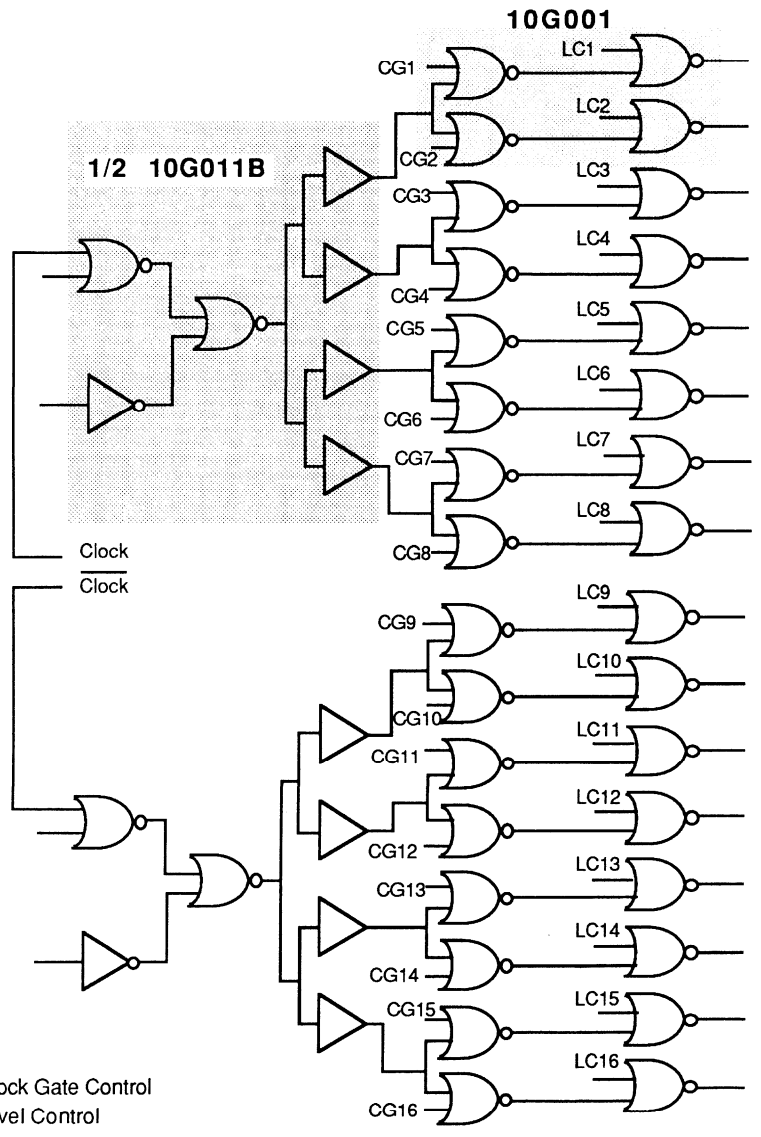
ISS & IEE vs. Temperature



Prop. Delay and Rise and Fall Times vs. Temperature



TYPICAL APPLICATION - TESTING



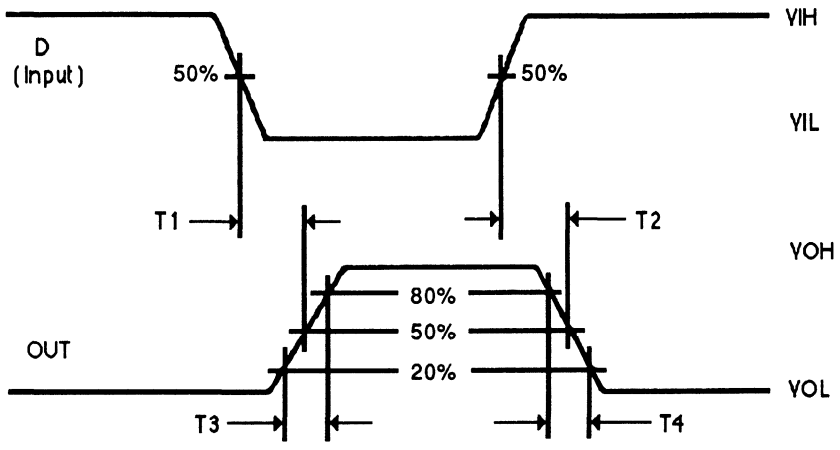
CG = Clock Gate Control
LC = Level Control

Output	CG	LC
CLK & $\overline{\text{CLK}}$	L	L
High	H	L
Low	X	H

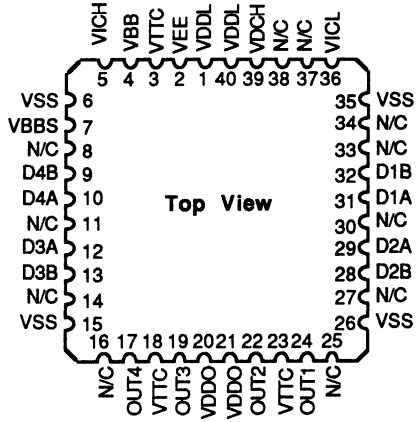
DESCRIPTION

This circuit can provide a clock (or clock complement) or high or low level data on each of 8 outputs. This is a generally useful signal generation scheme in many high precision testing applications where signal edge rates under 200ps are necessary.

SWITCHING WAVEFORMS



PIN FUNCTIONS - PACKAGE TYPES "L" AND "C"



Quad 2-Input XOR/XNOR/Line Receiver
1.8 GHz /600 ps Propagation Delay
10G PicoLogic™ Family

DISTINCTIVE CAPABILITIES

- -55°C to +125°C operation (10G002M)
- 150 ps typical output rise and fall times
- Differential DA inputs and true or inverted output
- ECL and 10G PicoLogic™ compatible I/O
- Temperature and voltage compensated using VBB threshold reference input
- On-chip VBBS (-1.3V) reference voltage supply
- GHz small signal amplifier
- Wire-OR output capability
- Available in C- leaded or leadless chip carrier or dice form
- Packages contain internal decoupling capacitors for optimum high frequency performance

APPLICATIONS

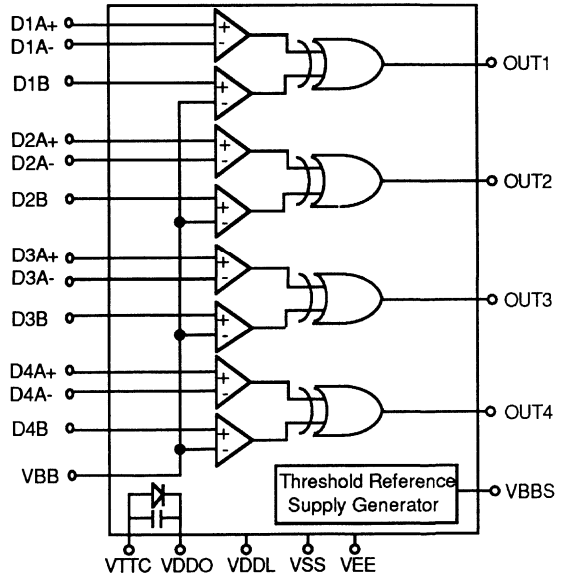
- Code Generation
- Precision pulse generation
- Level Comparator
- Differential Line Receiver
- Digital Phase Detector
- High speed ECL to GaAs translator

FUNCTIONAL DESCRIPTION

The 10G002 is an ECL or 10G PicoLogic™ compatible high speed quad XOR/XNOR gate. Because of its sensitive differential amplifier inputs, the 10G002 can also be used as a differential or single-ended line receiver or as a level comparator. In either application, the outputs can be inverted under control of the DB inputs. With the addition of an external low pass filter, the 10G002 can be used as a high frequency digital phase detector. The device features a nominal -1.3V GaAs/ECL threshold reference supply voltage output on pin VBBS. Maximum propagation delay and minimum guaranteed operating frequency at 25°C are 600ps and 1.8 GHz respectively at 800 mW power dissipation. Typical room temp. operating freq. is 2.0 GHz and higher speed operation is possible with some reduction in output level swing. Output transition times are typically 150ps. For extended temperature applications, the 10G002M is specified for operation over the -55°C to +125°C case temperature range.

The 10G002 is fabricated using GigaBit's high volume, production proven GaAs MESFET process technology.

BLOCK DIAGRAM

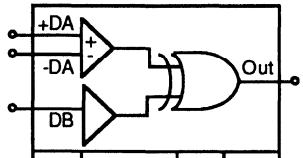


10G002/10G002M ORDERING INFORMATION

PACKAGE TYPE	10G002 (0°C- 85°C)		10G002M (-55°C - 125°C)	
	1.6 GHz	1.3 GHz	1.4 GHz	1.1 GHz
C-Leaded CC	10G002-2C	10G002-3C	10G002M-2C	10G002M-3C
Leadless CC	10G002-2L	10G002-3L	10G002M-2L	10G002M-3L
Dice		10G002-3X		10G002M-3X

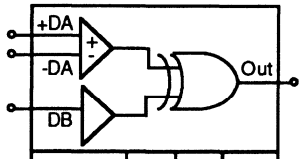
CONNECTION DIAGRAMS & TRUTH TABLES

XOR



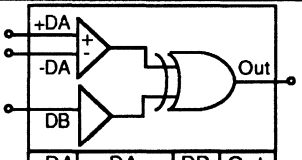
+DA	-DA	DB	Out
L	Vbb or H	L	L
L	Vbb or H	H	H
H	Vbb or L	L	H
H	Vbb or L	H	L

XNOR



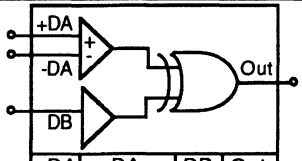
+DA	-DA	DB	Out
Vbb or H	L	L	H
Vbb or H	L	H	L
Vbb or L	H	L	L
Vbb or L	H	H	H

Line Receiver/ Comparator (Non-inverting)



	+DA	-DA	DB	Out
Receiver	H	L	L	H
	L	H	L	L
Comparator	V	Vth (<V)	L	H
	V	Vth (>V)	L	L
	V	V	X	U

Line Receiver/ Comparator (Inverting)



	+DA	-DA	DB	Out
Receiver	H	L	H	L
	L	H	H	H
Comparator	V	Vth (<V)	H	L
	V	Vth (>V)	H	H
	V	V	X	U

NOTES: X = Don't care, U = Undefined State
$-1.9V \leq V \leq -0.5V$
Vth = Threshold level, nominally VBB

FUNCTIONAL DESCRIPTION (cont.)

The operation of the 10G002 is illustrated in the adjacent connection diagrams and truth tables. The exclusive OR function of inputs DA+ and DB is formed by connecting the DA- input to the threshold reference level VBB or to the complement of the signal driving DA+ if this signal is differential. The exclusive NOR function utilizes the DA- and DB inputs and requires that the DA+ input be connected to VBB or the complement of the signal on DA-. As a differ- ential receiver, the10G002 accepts complementary signals on its DA inputs. The output is non-inverting when true and complement inputs are received on DA+ and DA- respectively with DB held low. An inverted output is obtained when either the DA connections are reversed or DB is held high. If one of the two DA inputs is replaced with a threshold reference level within the input's common mode range (-1.9V to -0.5V), the 10G002 performs a comparison between the other DA input and this level, producing an inverted or true output depending on the state of the B input.

When connected as either an XOR or XNOR gate, the 10G002 can function as a phase detector by producing an output binary signal whose duty cycle is proportional to the phase difference between the two inputs when the inputs are equal in frequency.

Since the output logic threshold level of various ECL and GaAs families will shift differently with temperature and supply voltage variation, the input threshold of the 10G002 is designed to track these movements. This is easily accomplished by connecting the interfacing logic family's threshold voltage to the 10G002's VBB input pin. This enables the 10G002's input threshold to track the threshold of devices connected to it, resulting in maximum noise immunity and minimum signal distortion over temperature and supply voltage variation. Some ECL devices (e.g. 10114,10115 100114,100125) and all second generation PicoLogic devices make the logic threshold level available on an output pin. In ECL it is termed VBB, and in PicoLogic it is referred to as VBBS. If unavailable, this voltage level can be generated by connecting the terminated output of an inverting gate back to its input with suitable filtering of the output to prevent oscillation.

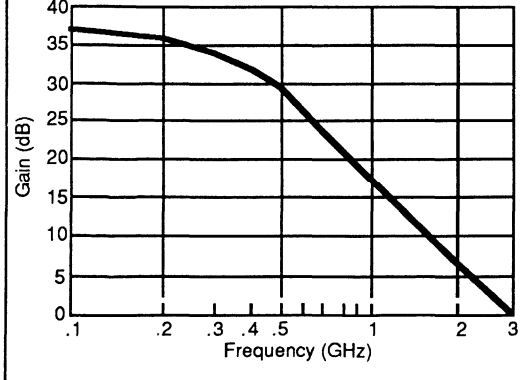
FUNCTIONAL DESCRIPTION (cont.)

When PicoLogic is used to drive the 10G002, the VBBS pin must be strapped to the VBB pin for proper device operation. Connecting VBBS to the VBB input is also appropriate, in some cases, for non-PicoLogic device interfaces. Examples of these are ECL-to-10G002 interface over a limited temperature range or when driving the10G002 from another GaAs device since GaAs logic output swings are generally much larger than ECL output swings. In any case, the VBB pin must always be connected to either the VBBS pin or to an external threshold reference voltage within the input's common mode range.

The 10G002 features two input clamp diodes which are brought out on pins VICH and VICL. These clamps can be used to internally limit a high peak-to-peak value input signal (i.e. when using the 10G002 as a phase detector and driving from a VCO with high output voltage), or to allow an improvement in an input sinewave signal edge speed by overdriving and clamping. When these pins are both connected to -1.3V, the internal input swing is limited to a range from approximately -.5V to -2.0V. When not used, VICH and VICL should be left unconnected.

Depending upon user choice of load resistor and termination voltage (VTT), the output high level (VOH) generated by the 10G002 (typically -0.4V to -0.5V) may require limiting when the 10G002 drives ECL logic. This is accomplished via an output driver clamp diode brought out on pin VDCH. For applications that require VOH limiting, consult GigaBit Application Note 4.

TYPICAL SMALL SIGNAL GAIN VS. FREQUENCY



PIN DESCRIPTIONS

D1A+ to D4A+	A differential data inputs, true
D1A- to D4A-	A differential data inputs, complement
D1-4B	B data inputs
OUT1-4	Outputs
VDDO	Output driver ground (0V)
VDDL	Internal logic ground (0V)
VSS	-3.4V power supply
VEE	-5.2V power supply
VTTC	VDDO internal decoupling capacitor return. VTTC is brought into the 10G002 package as the AC return lead for the internal VDDO output driver decoupling capacitor. It is not brought onto the 10G002 die.VTTC is typically equal to VTT (nominally -2.0V).
VDCH	Output driver high level clamp voltage. When driving other GaAs devices, VDCH is generally left unconnected.
VICH,VICL	Input protection clamp voltages. When connected to -1.3V, these allow an over-driven sine wave input signal to be truncated to a square wave, thus providing faster rise and fall times to the internal XOR gate. When not used, the input clamps should be left open. Inputs are internally clamped to VSS and VDDL.
VBB	Threshold reference level input. Provided to allow direct tracking of the driving logic family's output threshold voltage. Connect to VBBS when the 10G002 is driven from PicoLogic. When driving from ECL or other GaAs families, connect to that family's threshold voltage. This pin may not be left unconnected.
VBBS	PicoLogic threshold reference voltage output. Nominally equal to -1.3V with a 40Ω source impedance. Connect to VBB when interfacing with PicoLogic. ΔVBBS/ΔTemp. = 0.6mV/°C, ΔVBBS/ΔVSS = 200mV/V.

DC CHARACTERISTICS

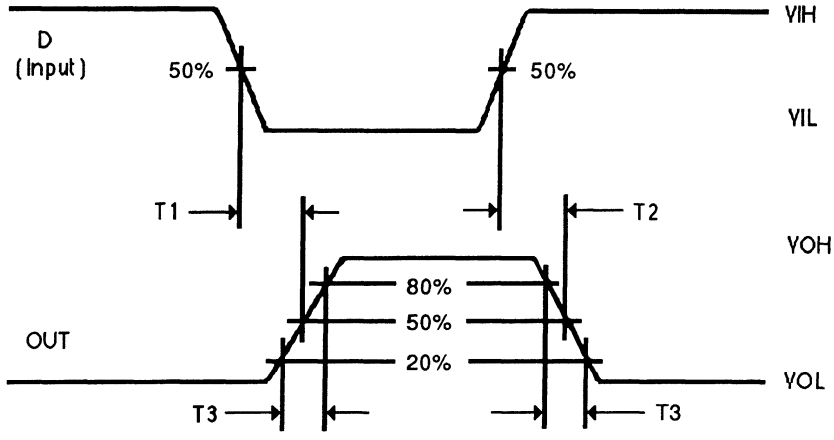
VSS = -3.5 V TO -3.3 V, VEE = -5.5 TO -5.1 V, VDDL = VDDO = Gnd., unless otherwise indicated

SYMBOL	PARAMETER	10G002 (0 to 85°C)			10G002M (-55 to +125°C)			Units
		Min	Typ.	Max	Min	Typ.	Max	
VOL	Ouput Voltage Low						-1.7	V
ISS	Power Supply Current		160	240		160	250	mA
IEE	Power Supply Current		55	75		55	75	mA
PD	Power Dissipation		800	1200		800	1200	mW

NOTE:

The remaining DC Characteristics are specified in the 10G PicoLogic™ Family Electrical Characteristics Table at the beginning of this section. This table notes parameter deviations to Family Characteristics and provides specific supplementary characteristics only.

SWITCHING WAVEFORMS



AC CHARACTERISTICS (Note 1)

10G002-2

VSS = -3.5V to -3.3V, VEE = -5.5V to -5.1V, VDDL=VDDO = 0V, unless otherwise indicated.

SYMBOL	PARAMETER	Tc = 0°C		Tc = +25°C			Tc = +85°C		UNITS	NOTES
		MIN	MAX	MIN	TYP	MAX	MIN	MAX		
T1	Prop. Delay, Low to High	350	600	350	450	600	400	650	ps	
T2	Prop. Delay, High to Low	350	600	350	450	600	400	650	ps	
T3	Output Rise/Fall Times		175		125	175		200	ps	2
F	Operating Frequency	1.8		1.8	2.0		1.6		GHz	

10G002-3

SYMBOL	PARAMETER	Tc = 0°C		Tc = +25°C			Tc = +85°C		UNITS	NOTES
		MIN	MAX	MIN	TYP	MAX	MIN	MAX		
T1	Prop. Delay, Low to High	400	650	400	500	650	450	700	ps	
T2	Prop. Delay, High to Low	400	650	400	500	650	450	700	ps	
T3	Output Rise/Fall Times		210		150	210		225	ps	2
F	Operating Frequency	1.5		1.5	1.8		1.3		GHz	

10G002-2M

SYMBOL	PARAMETER	Tc = -55°C		Tc = 25°C			Tc = 125°C		UNITS	NOTES
		MIN	MAX	MIN	TYP	MAX	MIN	MAX		
T1	Prop. Delay, Low to High	350	600	350	450	600	450	700	ps	
T2	Prop. Delay, High to Low	350	600	350	450	600	450	700	ps	
T3	Output Rise/Fall Times		175		125	175		210	ps	2
Fmax	Operating Frequency	1.8		1.8	2.0		1.4		GHz	

10G002-3M

SYMBOL	PARAMETER	Tc = -55°C		Tc = 25°C			Tc = 125°C		UNITS	NOTES
		MIN	MAX	MIN	TYP	MAX	MIN	MAX		
T1	Prop. Delay, Low to High	400	650	400	500	650	500	750	ps	
T2	Prop. Delay, High to Low	400	650	400	500	650	500	750	ps	
T3	Output Rise/Fall Times		210		150	210		240	ps	2
Fmax	Operating Frequency	1.5		1.5	1.8		1.1		GHz	

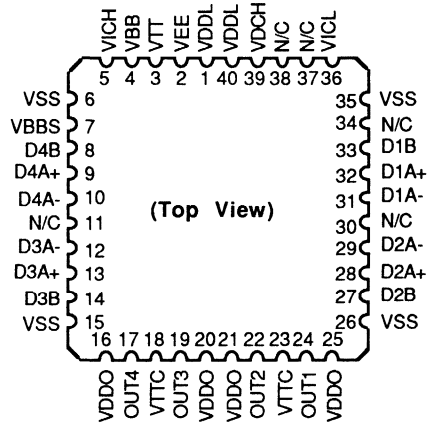
Notes: 1. Test conditions (unless otherwise indicated) :

VBB = -1.2V VICH = N/C VIH = -0.7V VOH ≥ -0.7V
VTT = -2.0V VICL = N/C VIL = -1.7V VOL ≤ -1.7V
VTTC = VTT VDCH = VDDO
RLOAD = 50Ω to -2.0V
Input signal rise and fall times ≤ 150 ps

2. Rise and fall times are measured at the 20% and 80% points of the transition from VOL max to VOH min.

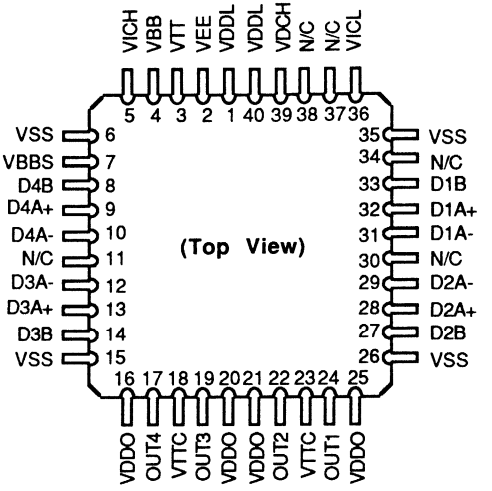
PACKAGE PINOUT DIAGRAMS

TYPE "L" PACKAGE



NOTES: Pin 1 is marked for orientation. N/C = No Connection.

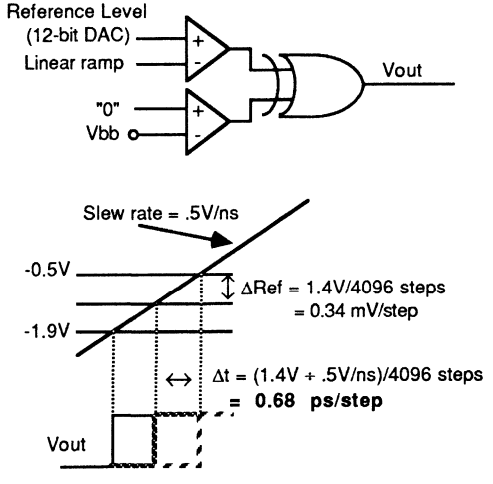
TYPE "C" PACKAGE



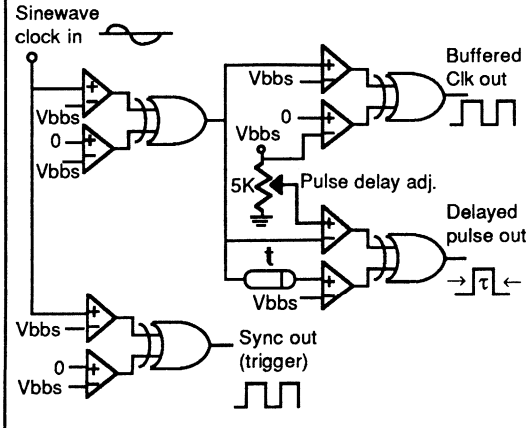
NOTES: Pin 1 is marked for orientation. N/C = No Connection.

TYPICAL APPLICATIONS

PRECISION TIME VERNIER



ADJUSTABLE DELAY PULSE GENERATOR



Dual AO/AOI Gate 4-Wide 5,4,3,2 / 2-Wide 3,2
800 ps Propagation Delay / 1.4 GHz
10G PicoLogic™ Family

DISTINCTIVE CAPABILITIES

- Dual AND/NAND gate operation
- 150 ps output rise and fall times
- Active low output enable control ($\overline{OE}$)
- ECL and 10G PicoLogic compatible I/O
- Temperature and voltage compensated using VBB threshold reference input
- -55/+125°C operation (10G003M)
- Wire-OR output capability
- On chip threshold reference voltage supply (VBBS)
- Available in 40 pin C-leaded or leadless chip carrier or dice form
- Packages contain internal decoupling capacitors for optimum high frequency performance

APPLICATIONS

- Logic functions including AND/NAND
- Precision gating/strobing
- Data distribution
- Digital multiplexing
- High speed level translator (10G, ECL, TTL/CMOS)

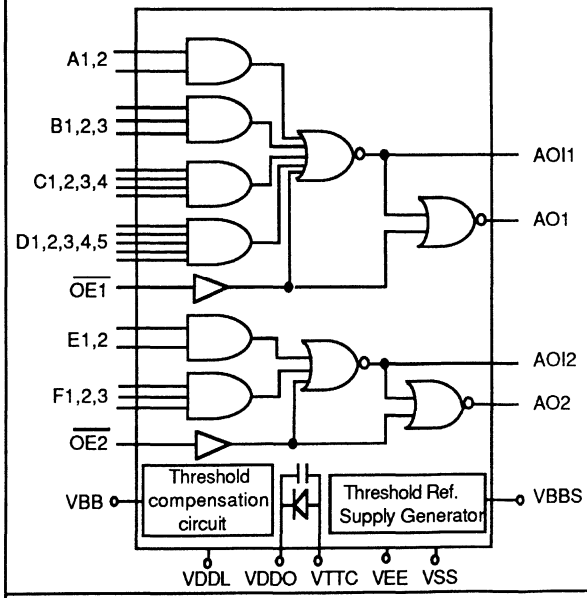
FUNCTIONAL DESCRIPTION

The 10G003 is an ultra fast dual AO/AOI gate capable of processing input signals from D.C. to 1.5 GHz. Maximum propagation delay at room temperature is 800 ps, three times shorter than equivalent ECL AO/AOI gates. The 10G003 features an output enable pin ($\overline{OE}$) to provide the capability for wired-OR bus connection.

For compatibility with other high speed logic families, the 10G003 features the Picologic™ family standard VBB input. This input allows the 10G003's threshold voltage to be controlled by the driving logic family. Therefore, mismatches in threshold level due to temperature and power supply variations can be compensated, providing high system noise immunity. An on-chip threshold voltage output (pin VBBS) is also provided. VBBS must be strapped to the VBB input when PicoLogic™ is used to drive the 10G003.

The 10G003 is a member of GigaBit's PicoLogic™ family of GaAs digital integrated circuits, and is fabricated using GigaBit's high volume GaAs MESFET process technology.

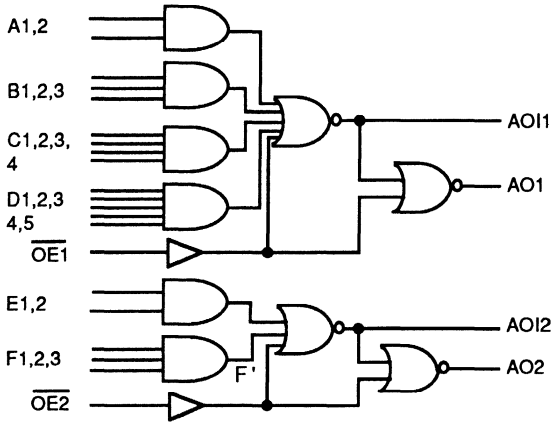
LOGIC DIAGRAM



10G003/10G003M ORDERING INFORMATION

PACKAGE TYPE	10G003(0°C/85°C) 1.4 GHz	10G003M (-55/125°C) 1.2 GHz
C-Leaded CC	10G003 2 C	10G003M - 2C
Leadless CC	10G003 - 2 L	10G003M - 2L
Dice	10G003 - 2 X	10G003M - 2X

10G003 Operation



F ' = Output of the 3-input AND gate

TRUTH TABLE (2-Wide 3,2 AO/AOI)

$\overline{OE}$	E1	E2	F '	AO2	AOI2
H	X	X	X	O	O
L	X	X	1	1	O
L	X	X	O	E1•E2	$\overline{E1•E2}$

Boolean Equations:

$AOI1 = [\,A1•A2 \cdot \overline{B1•B2•B3} \cdot \overline{C1•C2•C3•C4} \cdot \overline{D1•D2•D3•D4•D5}\,] \cdot \overline{OE1}$

$AO1 = [\,A1•A2 + B1•B2•B3 + C1•C2•C3•C4 + D1•D2•D3•D4•D5\,] \cdot \overline{OE1}$

$AOI2 = [\,\overline{E1.E2} \cdot \overline{F1•F2•F3}\,] \cdot \overline{OE2}$

$AO2 = [\,E1•E2 + F1•F2•F3\,] \cdot \overline{OE2}$

The operation of the 2-Wide 3,2 portion of the dual AO/AOI gate is described in the truth table above. All outputs can be forced low by bringing $\overline{OE}$ input high . If $\overline{OE}$ is low and F ' is 1 (i.e. F1=F2=F3=1) , AO2 is 1 and AOI2 is 0, independently of E1 and E2. If $\overline{OE}$ is low and F ' is 0 (i.e. F1=0 or F2=0 or F3=0), AO2 is the AND function for E1 and E2, and AOI2 is the NAND fuction for E1 AND E2.

Pin Descriptions

An....Fn	Data Inputs
$\overline{OE1}$	Output enable for 5 - 4 - 3 - 2 AO/AOI
$\overline{OE2}$	Output enable for 3 - 2 AO/AOI
AO1	5 - 4 - 3 - 2 AND - OR Output
AOI1	5 - 4 - 3 - 2 ANR - OR - INVERT Output
AO2	3 - 2 AND - OR Output
AOI2	3 - 2 AND - OR - INVERT Output
VDDO	Output driver ground pin (0 V)
VDDL	Internal logic ground connection (0V)
VSS	-3.4V power supply
VEE	-5.2V power supply
VTTC	The AC return pin for the package internal VDDO decoupling capacitor. VTTC is typically tied to VTT (nominally -2.0V)
VDCH	Output driver high level clamp voltage. When driving other GaAs devices, VDCH is generally left unconnected. When driving ECL, VDCH may be used to limit VOH. Consult Application Note 4 for detail.
VBB	Reference input to the 10G003's input threshold tracking circuit. Connect to the VBB supplied from ECL when driving the 10G003 from ECL. Connect to the VBBS pin when the 10G003 is driven from PicoLogic. This pin cannot be left unconnected.
VBBS	PicoLogic threshold reference output voltage. Connect to VBB when driving from PicoLogic. $\Delta VBBS/\Delta Temp = 0.6mV/°C$; $\Delta VBBS/\Delta VSS = 0.2\ mV/mV$.

DC CHARACTERISTICS

VSS = -3.5V to -3.3V, VEE = -5.5V to -5.1V, VDDL=VDDO = 0V, unless otherwise indicated.

Symbol	Parameter	10G003 (0 to 85°C)			10G003M (-55 to +125°C)			Units
		Min	Typ	Max	Min	Typ	Max	
VIH	Input voltage high				- 0.8			V
VIL	Input voltage low						- 1.8	V
I IN1	Input current ($\overline{OE1}$,$\overline{OE2}$)			1000			1000	µA
IIN2	Input current (all others)		150			150	750	µA
VBBS	Threshold reference voltage		-1.2			-1.2		V
ISS	Vss power supply current		170	270		170	300	mA
IEE	Vee power supply current		- 25	- 40		- 25	- 45	mA
PD	Power dissipation		700	1130		700	1250	mW

NOTE:

The remaining DC Characteristics are specified in the 10G PicoLogic™ Family Electrical Characteristics Table at the beginning of this section. This table notes parameter deviations to Family Characteristics and provides specific supplementary characteristics only.

AC CHARACTERISTICS (Notes 1, 2)

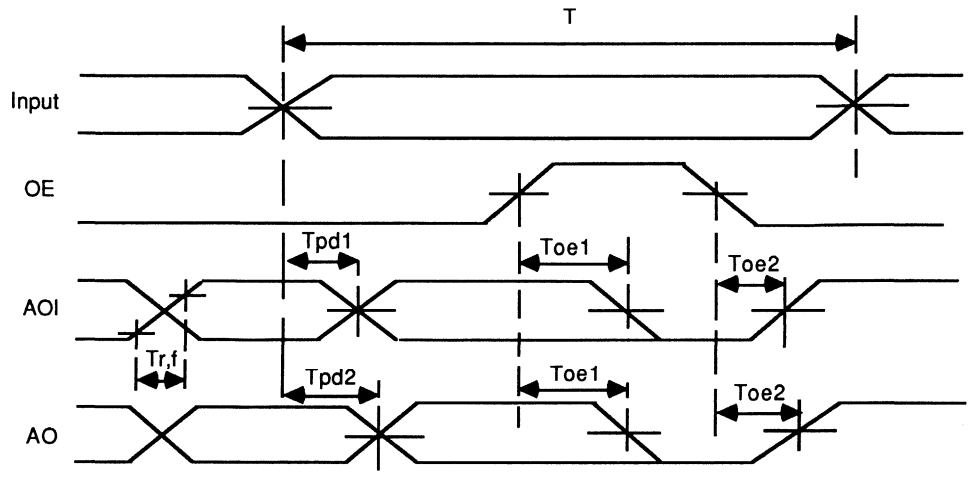
VSS= -3.5V to -3.3V, VEE= -5.5V to -5.1V, VDDL=VDDO=Gnd., unless otherwise indicated

SYMBOL	PARAMETER	10G003-2							10G003M-2							UNITS
		Tc= 0° C		Tc= 25° C			Tc= 85° C		Tc= -55° C		Tc= 25° C			Tc= 125° C		
		MIN	MAX	MIN	TYP	MAX	MIN	MAX	MIN	MAX	MIN	TYP	MAX	MIN	MAX	
1/(2T)	Operating Frequency	1.4		1.4	1.5		1.4		1.4		1.4	1.5		1.2		GHz
Tpd1	Input to AOI Output propagation delay	375	725	425	550	725	450	800	450	775	425	550	725	475	850	ps
Tpd2	Input to AO Output propagation delay	450	800	450	650	800	475	850	475	850	450	650	800	500	900	ps
Toe1	$\overline{OE}$ to Output High to low delay	350	600	350	475	600	375	675	375	650	350	475	600	425	725	ps
Toe2	$\overline{OE}$ to Output Low to High delay	350	600	350	475	600	375	675	375	650	350	475	600	425	725	ps
T r,f	Output rise and fall time		200		150	200		225		225		150	200		245	ps

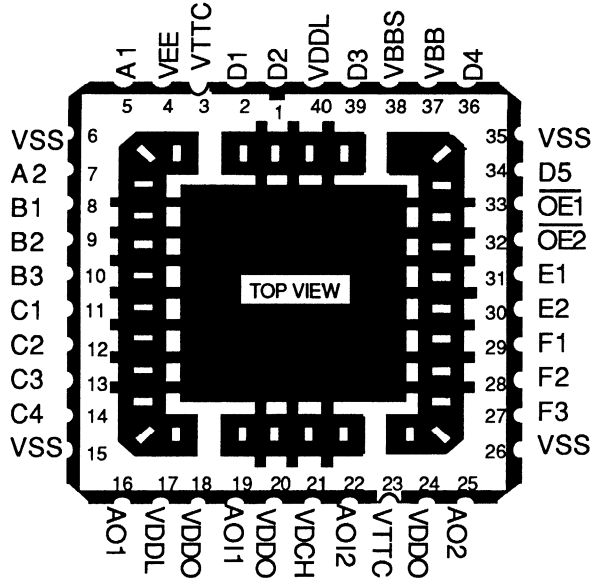
NOTES:

1. Test conditions (unless otherwise noted): VBB = -1.2V, VTT = -2.0V, VTTC = VTT, Rload = 50Ω to VTT, VDCH = VDDO, VIH = -0.7V, VIL = -1.7V, VOH ≥ -0.7V, VOL ≤ -1.7V. Input signal rise and fall times <150ps.
2. Output rise and fall times are measured at the 20% and 80% points of the transition from VOL max to VOH min.

SWITCHING WAVEFORMS



Pin Functions - Type "L" and "C" Packages



Quad 2:1 Multiplexer
1.8 GHz/3.6 Gbit/s NRZ Data Rate
10G PicoLogic™ Family

DISTINCTIVE CAPABILITIES

- 3.6 Gbit/sec output NRZ data rate
- 150 ps output rise and fall times
- Independent or common multiplexing controls
- ECL and 10G PicoLogic™ compatible I/O
- Temperature and voltage compensated using VBB threshold reference input
- Wire-OR output capability
- On-chip VBBS (-1.3V) reference voltage supply
- Available in 40 pin C-leaded or leadless chip carrier or dice form
- Packages contain internal decoupling capacitors for optimum high frequency performance

APPLICATIONS

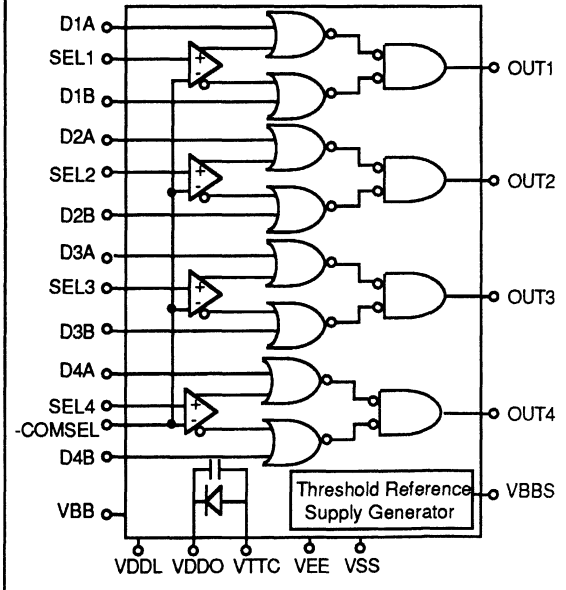
- High Speed Logic
- High Speed Fiber Optic Multiplexing

FUNCTIONAL DESCRIPTION

The 10G004 is an ECL and 10G PicoLogic™ I/O compatible ultra-fast quad 2:1 multiplexer with both independent and common multiplexing controls. Minimum 25°C multiplexing frequency is 1.8 GHz, making the 10G004 capable of generating a 3.6 Gbit/sec output NRZ data rate while dissipating just 700mW. Typical propagation delay is 450ps for the data inputs and 550ps for SEL and -COMSEL inputs. For compatibility with other high speed logic families, the 10G004 features the PicoLogic™ family standard VBB input which allows the input logic threshold to be controlled by the driving logic family. This way, mismatches in threshold level due to temperature and power supply variation can be compensated, providing high system noise immunity. An on-chip -1.3V threshold voltage output (pin VBBS) is also provided. VBBS must be strapped to the VBB input when PicoLogic™ is used to drive the 10G004.

The 10G004 is a member of GigaBit's PicoLogic™ family of GaAs digital integrated circuits, and is fabricated using GigaBit's high volume GaAs MESFET process technology.

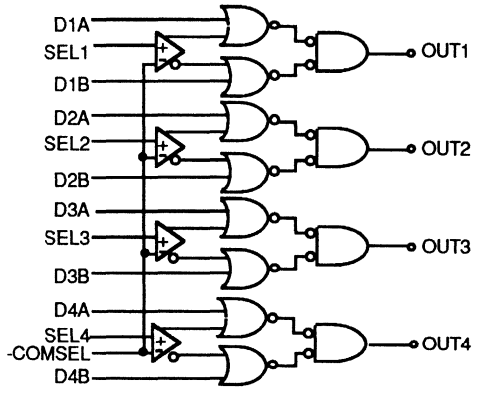
BLOCK DIAGRAM



10G004 ORDERING INFORMATION

PACKAGE TYPE	SPEED (Min. 0°C to 85°C)	
	1.6 GHz	1.3 GHz
C-Leaded CC	10G004-2C	10G004-3C
Leadless CC	10G004-2L	10G004-3L
Dice		10G004-3X

10G004 Operation



TRUTH TABLE

-COMSEL	SELn	DA	DB	OUT
VBBS	1	X	1	1
VBBS	1	X	0	0
VBBS	0	1	X	1
VBBS	0	0	X	0
1	VBBS	1	X	1
1	VBBS	0	X	0
0	VBBS	X	1	1
0	VBBS	X	0	0

The operation of the 10G004 is illustrated by referring to the logic diagram and truth table above. Each of the four multiplexers will select either the DA or DB input and direct it to the output in response to the individual SELn controls or the common select (-COMSEL) control. Each of the four SELn inputs (SEL1 ... SEL4) forms a differential input with the -COMSEL input. For this reason, the -COMSEL input must be tied to the threshold reference voltage VBBS when individual multiplex control is required. Similarly, when all four multiplexers are to be switched in common using -COMSEL, SEL1 through SEL4, must all be tied to the VBBS output.

When the SELn inputs are high (low), the DB (DA) inputs are selected and directed to the output. If the -COMSEL control is used instead, the function is reversed with a high on -COMSEL selecting the DA inputs and a low selecting the DB inputs.

Again, the select control inputs not being driven must be tied to the VBBS threshold output pin for proper operation.

Pin Descriptions

D1A - D4A	A data inputs
D1B - D4B	B data inputs
SEL1 - SEL4	Individual multiplexer input selection controls (differential input)
-COMSEL	Common select control for all four multiplexers (differential input)
OUT1- OUT4	Multiplexer outputs
VDDO	Output driver ground pin (0V)
VDDL	Internal logic ground connection (0V)
VSS	-3.4V power supply
VEE	-5.2V power supply
VTTC	The AC return pin for the package internal VDDO decoupling capacitor. VTTC is not brought onto the 10G004 circuit, and is typically tied to VTT (nominally -2.0V)
VDCH	Output driver high level clamp voltage. When driving other GaAs devices, VDCH is generally left unconnected. When driving ECL, VDCH may be used to limit VOH. Consult Application Note 4 for detail.
VBB	Reference input to the 10G004's input threshold tracking circuit. Connect to the VBB supplied from ECL when driving the 10G004 from ECL. Connect to the VBBS pin when the 10G004 is driven from PicoLogic. This pin may not be left unconnected.
VBBS	PicoLogic threshold reference output voltage. Nominally equal to -1.3V with a 40Ω source impedance. Connect to VBB when driving from PicoLogic. ΔVBBS/ΔTemp = 0.6mV/°C; ΔVBBS/ΔVSS = 0.2 mV/mV.

DC CHARACTERISTICS

Tc = 0°C to 85°C, VSS = -3.5 V to -3.3 V, VEE = -5.5 to -5.1 V, VDDL = VDDO = 0 V, unless otherwise indicated

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	TEST CONDITIONS
IINCS	COMSEL Input Current	-1000	350	1000	µA	Vin: -1.0 to -1.6 V
ISS	Power Supply Current		115	170	mA	
IEE	Power Supply Current		55	85	mA	
PD	Power Dissipation		700	1020	mW	

NOTE:

The remaining DC Characteristics are specified in the 10G PicoLogic™ Family Electrical Characteristics Table at the beginning of this section. This table notes parameter deviations to Family Characteristics and provides specific supplementary characteristics only.

AC CHARACTERISTICS (Note 1)

VSS = -3.5V to -3.3V, VEE = -5.5V to -5.1V, VDDL=VDDO = 0V, unless otherwise indicated.

10G004-2

SYMBOL	PARAMETER	Tc = 0°C		Tc = +25°C			Tc = +85°C		UNITS	NOTES
		MIN	MAX	MIN	TYP	MAX	MIN	MAX		
F	Multiplexing frequency	1.8		1.8	2.0		1.6		GHz	
T1	SELn, -COMSEL to output delay	350	700	350	550	700	400	825	ps	
T2	Data inputs to output delay	300	600	300	450	600	300	650	ps	
T3	Output rise and fall times		175		125	175		200	ps	2

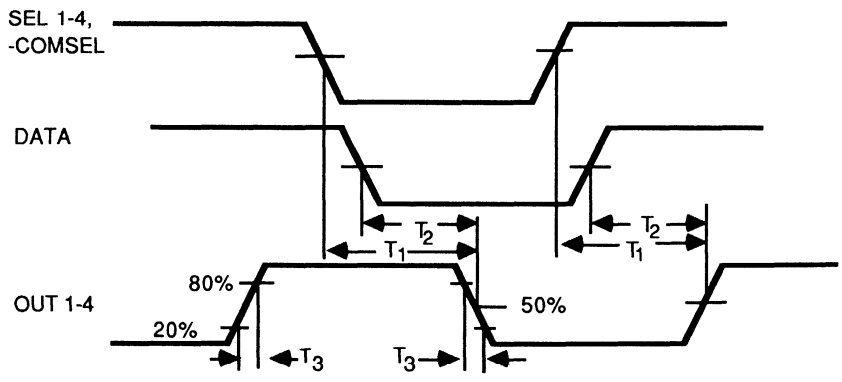
10G004-3

SYMBOL	PARAMETER	Tc = 0°C		Tc = +25°C			Tc = +85°C		UNITS	NOTES
		MIN	MAX	MIN	TYP	MAX	MIN	MAX		
F	Multiplexing frequency	1.5		1.5	1.8		1.3		GHz	
T1	SELn, -COMSEL to output delay	350	750	350	600	750	400	875	ps	
T2	Data inputs to output delay	300	650	300	500	650	300	700	ps	
T3	Output rise and fall times		210		150	210		225	ps	2

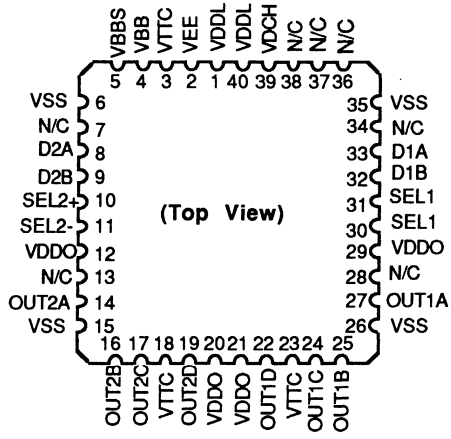
NOTES:

1. Test conditions (unless otherwise noted): VBB = -1.2V, VTT = -2.0V, VTTC = VTT, Rload = 50Ω to VTT, VDCH = VDDO, VIH = -0.7V, VIL = -1.7V, VOH ≥ -0.7V, VOL ≤ -1.7V. Input signal rise and fall times <150ps.
2. Output rise and fall times are measured at the 20% and 80% points of the transition from VOL max to VOH min.

SWITCHING WAVEFORMS



PIN FUNCTIONS - PACKAGE TYPES "L" AND "C"



NOTES:
Pin 1 is marked for orientation. N/C = no connection.

GBL GigaBit Logic

10G010
10G010M

Dual 2:1 Multiplexed Fanout Buffer
1.5 GHz Rate
10G PicoLogic™ Family

DISTINCTIVE CAPABILITIES

- Enhanced Version of the 10G011B
- 150 ps output rise and fall times
- 750 ps max. prop. delay
- ECL and 10G PicoLogic compatible I/O
- Temperature and voltage compensated using VBB threshold reference input
- Either inverting or non-inverting operation
- 70 mA output drive current
- Wire-OR output capability
- On-chip VBBS (-1.3V) reference voltage supply
- Available in 40 pin C-leaded or leadless chip carrier or dice form
- Packages contain internal decoupling capacitors for optimum high frequency performance

APPLICATIONS

- High Speed Logic
- Bi-Phase or Single Phase Clock Driver
- Capacitive Load Driver
- Address & Data Buffers

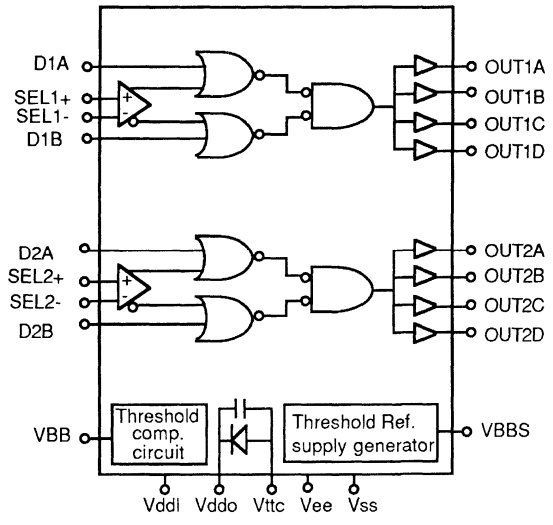
FUNCTIONAL DESCRIPTION

The 10G010 is an ECL and 10G PicoLogic™ I/O compatible ultra-fast dual 2:1 multiplexer with independent multiplexing controls and four output buffers. Due to its design, both true and complement clocks can be derived from a single ended clock input and buffered by one chip, minimizing clock skews. Four large source followers on each half can each drive two 50 ohm lines or the center of a 50 ohm bus with the option of wire-ORed outputs. Minimum 25°C operating frequency is 1.5 GHz. Typical propagation delay is 500ps for the data inputs and 575ps for the SEL+ and SEL- inputs.

For compatibility with other high speed logic families, the 10G010 features the PicoLogic™ family standard VBB input which allows the input logic threshold to be controlled by the driving logic family, thereby compensating for mismatches in threshold level due to temperature and power supply variation and providing high system noise immunity. An on-chip -1.3V threshold voltage output (pin VBBS) is also provided for strapping to the VBB input when PicoLogic™ is used to drive the 10G010.

The 10G010 is a member of GigaBit's PicoLogic™ family of GaAs digital integrated circuits, and is fabricated using GigaBit's high volume GaAs MESFET process technology.

BLOCK DIAGRAM

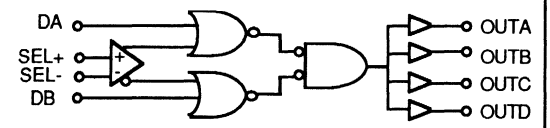


10G010/10G010M ORDERING INFORMATION

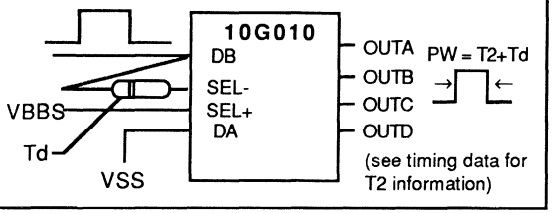
PACKAGE TYPE	10G010 (0°C/85°C)		10G010M (-55°C/125°)	
	1.3 GHz	1.1 GHz	1.3 GHz	1.0 GHz
C-Leaded CC	10G010-2C	10G010-3C	10G010M-2C	10G010M-3C
Leadless CC	10G010-2L	10G010-3L	10G010M-2L	10G010M-3L
Dice		10G010-3X		10G010M-3X

10G010 Operation

LOGIC DIAGRAM



TYPICAL APPLICATION - ONE SHOT



MULTIPLEXING TRUTH TABLE

SEL-	SEL+	DA	DB	OUTs
VBBS	1	X	1	1
VBBS	1	X	0	0
VBBS	0	1	X	1
VBBS	0	0	X	0
1	VBBS	1	X	1
1	VBBS	0	X	0
0	VBBS	X	1	1
0	VBBS	X	0	0

The operation of the 10G010 as a multiplexer is illustrated by referring to the logic diagram and truth table above. Each of the two multiplexers will select either the DA or DB input and direct it to the outputs in response to the individual SEL+ & SEL- controls. The SEL inputs may be driven either differentially or single ended with the unused input tied to VBBS or ECL derived VBB. It may also be wired as either an inverting or non-inverting Fanout Buffer with delays matched between the two halves within 50ps for either true or complement operation. Tying the B input high (VDDL) and the A input low (VSS) results in outputs which are inverted from the SEL-, and in phase with the SEL+ inputs, assuming that the unused SEL input is tied to the VBBS (-1.3V) reference. This feature allows the generation of a two phase clock from a single ended clock input, buffering it for distribution with skews at all outputs typically less than 50 ps.

Above is shown an application which will shorten a positive pulse similar to a one shot. This circuit can be configured to work on either the positive or negative edge of the input. Since the delay difference between A and SEL is minimal, the pulse width will be largely determined by the delay line.

Pin Descriptions

D1A, D2A	A data inputs
D1B, D2B	B data inputs
SEL1+,SEL2+	Positive select controls - high selects B (differential input)
SEL1-,SEL2-	Negative select controls - high selects A (differential input)
OUT1A - D	Multiplexer 1 outputs
OUT2A - D	Multiplexer 2 outputs
VDDO	Output driver ground pin (0V)
VDDL	Internal logic ground connection (0V)
VSS	-3.4V power supply
VEE	-5.2V power supply
VTTC	The AC return pin for the package internal VDDO decoupling capacitor. VTTC is not brought onto the 10G010 circuit, and is typically tied to VTT (nominally -2.0V)
VDCH	Output driver high level clamp voltage. When driving other GaAs devices, VDCH is generally left unconnected. When driving ECL, VDCH may be used to limit VOH. Consult Application Note 4 for detail.
VBB	Reference input to the 10G010's input threshold compensation circuit. Connect to the VBB supplied from ECL when driving from ECL. Otherwise connect to VBBS pin.
VBBS	PicoLogic threshold reference output voltage. Nominally equal to -1.3V with a 40Ω source impedance. Connect to VBB when driving from PicoLogic. ΔVBBS/ΔTemp = +0.6mV/°C; ΔVBBS/ΔVSS = 0.2 mV/mV.

NOTE: Neither VBB nor the signal inputs may be left unconnected.

Special Usage Precautions:

Typically, the 10G010 is used with multiple outputs loaded. Each source-follower output is capable of sourcing up to 70 mA of current depending on the load. Coupled with high output slew rates of 7V/ns, the result is very high instantaneous output switching currents. Following the relation for induced voltage transients, V = L dI/dt, considerable noise voltage can be induced in the power supply lines. Therefore, diligent attention to power supply decoupling and continuous power plane layout (refer to Application Note 2) is absolutely essential when using the 10G010. Given the limitations of real board designs, the 10G010 can exhibit phase jitter of the output signal, resulting in output duty cycle variation, under the following specific conditions: A input tied high (to VDD); SEL- set at threshold (-1.3V; ECL VBB or VBBS) and the signal applied to the SEL+ input in the approximate frequency range of 400 MHz to 600 MHz. If the input signal is outside this frequency range, any tendency for the output to exhibit phase jitter is absent. No other operating mode is problematic. Given this operating sensitivity, GigaBit recommends that the A input be tied low (to VSS) in any application where the data multiplexing feature of the 10G010 is not used; i.e. for fan-out or inverting fan-out buffer applications or when the 10G010 is driven differentially. If the multiplexing capability of the 10G010 is to be used, the signal should be applied to the SEL- input with the SEL+ input tied to threshold to preclude the possibility of output phase jitter. These restrictions do not limit the range of logic functions the 10G010 can perform. They provide a preferred connection scheme where there is more than one way to wire a given function. Refer to Applications Brief 2 for additional discussion of these issues.

DC CHARACTERISTICS

TC = -55°C to +125°C, VSS = -3.5 V to -3.3 V, VEE = -5.5 V to -5.1 V, VDDL = VDDO = 0 V, unless otherwise indicated

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
ISS	Power Supply Current		125	200	mA
IEE	Power Supply Current		50	80	mA
PD	Power Dissipation		690	1100	mW

NOTE:

The remaining DC Characteristics are specified in the 10G PicoLogic™ Family Electrical Characteristics Table at the beginning of this section. This table notes parameter deviations to Family Characteristics and provides specific supplementary characteristics only.

AC CHARACTERISTICS (Note 1)

VSS = -3.5V to -3.3V, VEE = -5.5V to -5.1V, VDDL=VDDO = 0V, unless otherwise indicated.

10G010-2

SYMBOL	PARAMETER	Tc = 0°C		Tc = +25°C			Tc = +85°C		UNITS	NOTES
		MIN	MAX	MIN	TYP	MAX	MIN	MAX		
F	Operating frequency	1.5		1.5	1.8		1.3		GHz	
T1	SEL+, SEL- to output delay	400	700	400	575	700	425	750	ps	
T2	Data inputs to output delay	360	625	360	500	625	385	675	ps	
T3	Output rise and fall times		175		125	175		195	ps	2

10G010-3

SYMBOL	PARAMETER	Tc = 0°C		Tc = +25°C			Tc = +85°C		UNITS	NOTES
		MIN	MAX	MIN	TYP	MAX	MIN	MAX		
F	Operating frequency	1.3		1.3	1.5		1.1		GHz	
T1	SEL+, SEL- to output delay	425	750	425	625	750	450	800	ps	
T2	Data inputs to output delay	385	675	385	550	675	410	725	ps	
T3	Output rise and fall times		200		150	200		225	ps	2

AC CHARACTERISTICS, cont. (Note 1)

10G010M-2

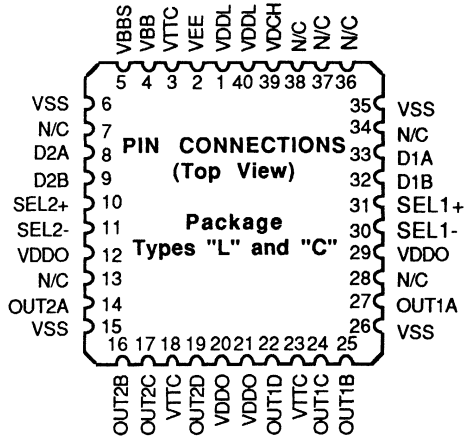
SYMBOL	PARAMETER	Tc = -55°C		Tc = +25°C			Tc=125°C		UNITS	NOTES
		MIN	MAX	MIN	TYP	MAX	MIN	MAX		
F	Operating frequency	1.4		1.5	1.8		1.3		GHz	
T1	SEL+, SEL- to output delay	400	700	400	575	700	450	800	ps	
T2	Data inputs to output delay	360	625	360	500	625	410	725	ps	
T3	Output rise and fall times		175		125	175		210	ps	2

10G010M-3

SYMBOL	PARAMETER	Tc = -55°C		Tc = +25°C			Tc=125°C		UNITS	NOTES
		MIN	MAX	MIN	TYP	MAX	MIN	MAX		
F	Operating frequency	1.2		1.3	1.5		1.0		GHz	
T1	SEL+, SEL- to output delay	425	750	425	625	750	460	825	ps	
T2	Data inputs to output delay	385	675	385	550	675	435	775	ps	
T3	Output rise and fall times		200		150	200		250	ps	2

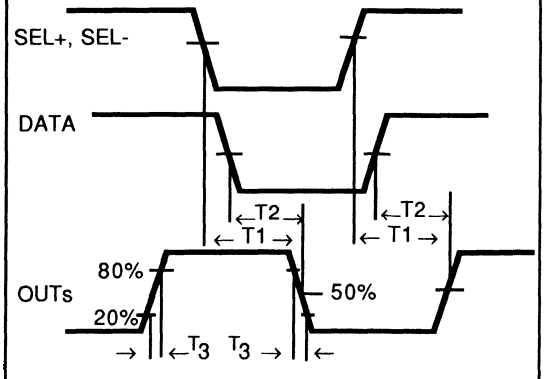
NOTES:

1. Test conditions (unless otherwise noted): VBB = -1.2V, VTT = -2.0V, VTTC = VTT, Rload = 50Ω to VTT, VDCH = VDDO, VIH = -0.7 V, VIL = -1.7 V, VOH ≥ -0.7 V, VOL ≤ -1.7 V. Input signal rise and fall times <150ps.
2. Output rise and fall times are measured at the 20% and 80% points of the transition from VOL max to VOH min.



Pin 1 is marked for orientation. N/C = no connection.

SWITCHING WAVEFORMS



GBL GigaBit Logic

10G011B
10G011BM

Dual 1 to 4 Fanout Buffer
1.6 GHz Rate
10G PicoLogic™ Family

DISTINCTIVE CAPABILITIES

- Low output skew and propagation delay
- Individual Input, Gate, and Enable pins on each buffer
- Greater than 60 mA drive capability per output
- PicoLogic and ECL compatible inputs and outputs
- Output stage supports a wide range of load resistor and termination voltage combinations.
- Wire-OR capabilty
- TTL/CMOS interface capability
- On chip VBBS (-1.3V) reference voltage
- Temperature and voltage compensated design
- Available in C-leaded or leadless chip carriers or in dice form
- Packages contain internal decoupling capacitors for optimum high frequency performance

APPLICATIONS

- Line Driver
- Clock Distribution and Fanout
- Capacitive Load Driver
- Data Buffer

FUNCTIONAL DESCRIPTION

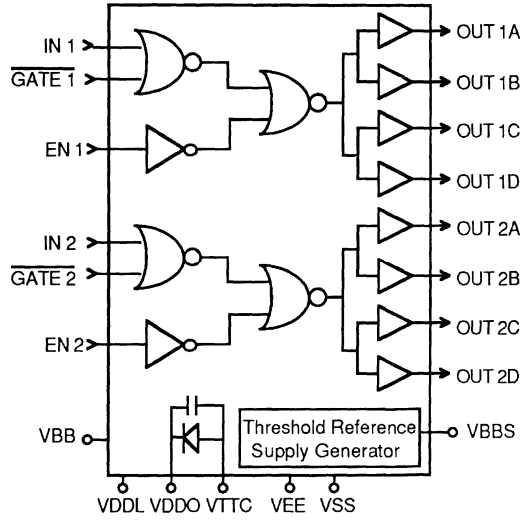
The 10G011B is a high speed, dual 1 to 4 fanout buffer. Because the 10G011B is a dual buffer, both true and complementary clock signals can be buffered by one chip, minimizing skew differences between the two clock phases. Each half of the device contains individual input, gate, and enable pins. Source-follower outputs allow the use of Wire-OR logic operations, facilitating clock gating.

The 10G011B is designed to drive capacitive loads with fast edge rates, providing greater than 60 mA of current drive capability per output.

For compatibility with other high speed logic families, the 10G011B features the PicoLogic family standard VBB input which allows the input logic threshold to be controlled by the driving logic family, thereby compensating for mismatches in threshold level due to temperature and power supply variation and providing high system noise immunity. An on-chip -1.3V threshold voltage output (pin VBBS) is also provided for strapping to the VBB input when PicoLogic is used to drive the 10G011B.

The 10G011B is a member of GigaBit's PicoLogic family of GaAs digital ICs and is fabricated using GigaBit's high volume GaAs MESFET process technology.

LOGIC DIAGRAM



10G011B/10G011BM ORDERING INFORMATION

PKG. TYPE	10G011B (0°C/85°C)		10G011BM (-55°C/125°C)	
	1.4 GHz	1.1 GHz	1.3 GHz	1.0 GHz
C	10G011B-3C	10G011B-4C	10G011BM-3C	10G011BM-4C
L	10G011B-3L	10G011B-4L	10G011BM-3L	10G011BM-4L
X	10G0	10G011B-4X		10G011BM-4X

FUNCTIONAL DESCRIPTION (cont.)

The signal on the IN (INput) pin is passed to the output only when $\overline{\text{GATE}}$ is logic low and EN (ENable) is logic high. For all other $\overline{\text{GATE}}$ and EN logic value combinations, the signal on the IN pin has no effect on the output. The detailed operation of the 10G011B is summarized in the truth table.

TRUTH TABLE

IN	$\overline{\text{GATE}}$	EN	OUT
X	0	0	0
0	0	1	0
X	1	0	0
X	1	1	1
1	0	1	1

PIN DESCRIPTIONS

$\overline{\text{IN1,2}}$	Signal inputs
$\overline{\text{GATE1,2}}$	Gate control inputs
EN1,2	Enable control inputs
OUT1A - D	Buffer1 outputs
OUT2A - D	Buffer 2 outputs
VDDO	Output driver ground pin (0V)
VDDL	Internal logic ground connection (0V)
VSS	-3.4V power supply
VEE	-5.2V power supply
VTTC	The AC return pin for the package internal VDDO decoupling capacitor. VTTC is not brought onto the 10G011B circuit, and is typically tied to VTT (nominally -2.0V)
VDCH	Output driver high level clamp voltage. When driving other GaAs devices, VDCH is generally left unconnected. When driving ECL, VDCH may be used to limit VOH. Consult Application Note 4 for detail.
VBB	Reference input to the 10G011B's input threshold compensation circuit. Connect to the VBB supplied from ECL when driving from ECL. Otherwise connect to VBBS.
VBBS	PicoLogic threshold reference output voltage. Nominally equal to -1.3V with a 40Ω source impedance. Connect to VBB when driving from PicoLogic. ΔVBBS/ΔTemp = +0.6mV/°C; ΔVBBS/ΔVSS = 0.2 mV/mV.

SPECIAL USAGE PRECAUTIONS

Because the 10G011B drives multiple outputs in phase with the input, there may be a tendency for an output to exhibit a jitter or phase noise induced by external coupling, depending on signal phase relationship and circuit delays. For this reason, it is essential that power plane decoupling recommendations found in Application Note 2 be diligently followed. Additionally, it has been found that use of the EN input will not result in output phase jitter and that use of the IN input is less likely than the GATE input to cause this problem. To further reduce the probability that output phase jitter will occur, it is mandatory that the GATE input and desirable that the IN input be driven with GaAs levels (Vih min. = -0.7V, Vil max. = -1.7V). If all four outputs are not required, then the A outputs should not be used. Also, phase jitter is most likely to occur when operating the device in the ranges of 400 to 500 MHz or 800 to 1000 MHz depending upon board layout and design.

DC CHARACTERISTICS

Tc = -55°C to +125°C, VSS = -3.5 to -3.3 V, VEE = -5.5 to -5.1 V, VDDL = VDDO = 0V, unless otherwise indicated

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
ISS	Power Supply Current		125	200	mA
IEE	Power Supply Current		50	80	mA
PD	Power Dissipation		690	1100	mW

NOTE:

The remaining DC Characteristics are specified in the 10G PicoLogic™ Family Electrical Characteristics Table at the beginning of this section. This table notes parameter deviations to Family Characteristics and provides specific supplementary characteristics only.

AC CHARACTERISTICS (Note 1)

10G011B-3

VSS = -3.5V to -3.3V, VEE = -5.5V to -5.1V, VDDL=VDDO = 0V, unless otherwise indicated.

SYMBOL	PARAMETER	Tc = 0°C		Tc = +25°C			Tc = 85°C		UNITS	NOTES
		MIN	MAX	MIN	TYP	MAX	MIN	MAX		
1/T1	Max Input Frequency	1.6		1.6	1.8		1.4		GHz	
T2	Delay, IN to OUT	300	625	300	500	625	325	675	ps	
T3	Delay, GATE to OUT	350	700	350	575	700	375	750	ps	
T4	Delay, EN to OUT	300	625	300	500	625	325	675	ps	
T5	Skew between OUT pins		50		30	50		50	ps	
T6	OUT rise and fall times		175		125	175		195	ps	2

10G011B-4

SYMBOL	PARAMETER	Tc = 0°C		Tc = +25°C			Tc = 85°C		UNITS	NOTES
		MIN	MAX	MIN	TYP	MAX	MIN	MAX		
1/T1	Max Input Frequency	1.3		1.3	1.5		1.1		GHz	
T2	Delay, IN to OUT	300	675	300	550	675	325	725	ps	
T3	Delay, GATE to OUT	350	750	350	625	750	375	800	ps	
T4	Delay, EN to OUT	300	675	300	550	675	325	725	ps	
T5	Skew between OUT pins		50		30	50		50	ps	
T6	OUT rise and fall times		200		150	200		225	ps	2

10G011BM-3

SYMBOL	PARAMETER	Tc = -55°C		Tc = +25°C			Tc = 125°C		UNITS	NOTES
		MIN	MAX	MIN	TYP	MAX	MIN	MAX		
1/T1	Max Input Frequency	1.5		1.6	1.8		1.3		GHz	
T2	Delay, IN to OUT	300	625	300	500	625	350	725	ps	
T3	Delay, GATE to OUT	350	700	350	575	700	400	800	ps	
T4	Delay, EN to OUT	300	625	300	500	625	350	725	ps	
T5	Skew between OUT pins		50		30	50		50	ps	
T6	OUT rise and fall times		175		125	175		210	ps	2

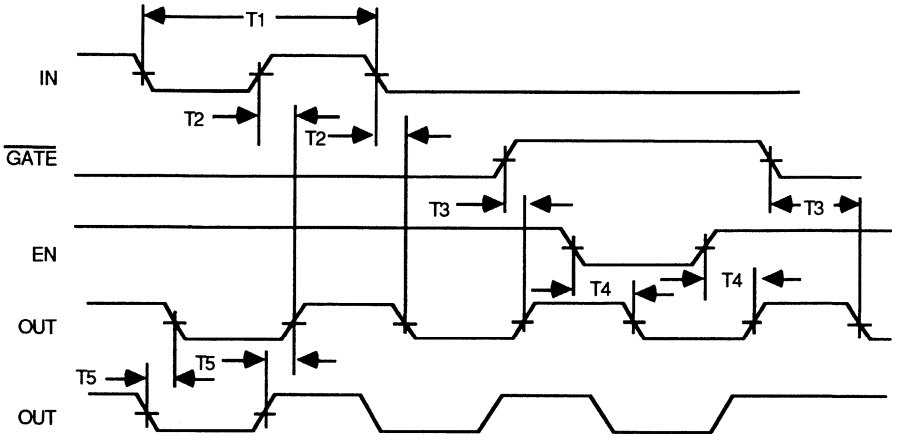
10G011BM-4

SYMBOL	PARAMETER	Tc = -55°C		Tc = +25°C			Tc = 125°C		UNITS	NOTES
		MIN	MAX	MIN	TYP	MAX	MIN	MAX		
1/T1	Max Input Frequency	1.2		1.3	1.5		1.0		GHz	
T2	Delay, IN to OUT	300	675	300	550	675	350	775	ps	
T3	Delay, GATE to OUT	350	750	350	625	750	400	825	ps	
T4	Delay, EN to OUT	300	675	300	550	675	350	775	ps	
T5	Skew between OUT pins		50		30	50		50	ps	
T6	OUT rise and fall times		200		150	200		250	ps	2

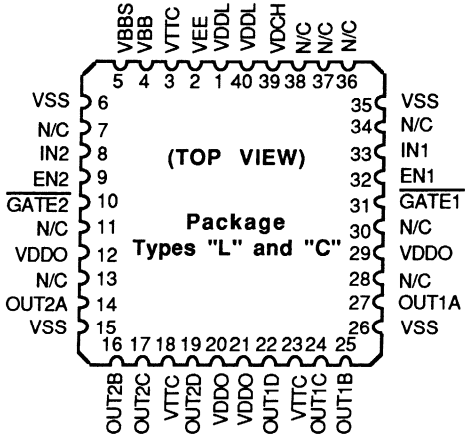
Notes:

1. Test conditions (unless otherwise noted): VBB = -1.2V; VTT = -2.0V; VTTC = VTT; Rload = 50Ω to VTT; VDCH = VDDO; VIH = -0.7 V; VIL = -1.7 V; VOH ≥ -0.7 V; VOL ≤ -1.7 V. Input signal rise and fall times <150 ps.
2. Output rise and fall times are measured at the 20% and 80% points of the transition from VOL max to VOH min.

SWITCHING WAVEFORMS



PACKAGE PIN FUNCTION



Pin 1 is marked for orientation. N/C = no connection

GigaBit Logic

10G012B
10G013

Dual Complementary Driver/Comparator
1.75 GHz / 500 ps Delay
10G PicoLogic™ Family

DISTINCTIVE CAPABILITIES

- High gain comparator input
- Fixed 50% output duty cycle (10G012B)
- Adjustable output overlap (10G013)
- <50 ps skew between complementary outputs
- >70 mA output drive capability
- 150 ps output rise & fall times
- On-chip -1.3V GaAs/ECL threshold reference voltage generator (VBBS)
- Temperature and voltage compensated
- Available in 40 I/O C-leaded and leadless chip carriers, 36 I/O flatpack or chip carrier or in die form
- Packages contain internal decoupling capacitors for optimum high frequency performance

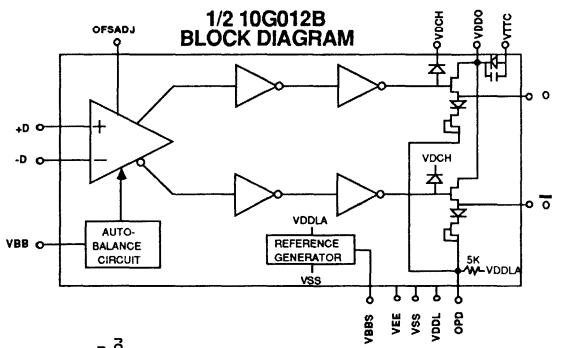
APPLICATIONS

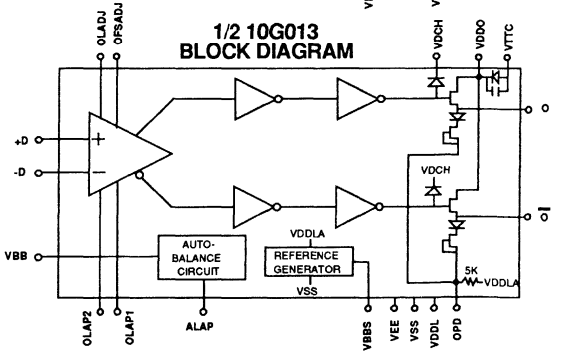
- Differential Line Driver
- Differential Line Receiver
- 2 - phase clock generator
- Laser Diode Driver
- High Speed Comparator
- Capacitive Load Driver

FUNCTIONAL DESCRIPTION

The 10G012B and 10G013 are versatile high speed dual drivers/comparators with differential outputs. The 10G013 provides controls to adjust the output overlap (time during which both outputs are simultaneously high or low). The 10G012B hard wires these controls internally so that the outputs exhibit a fixed 50% duty cycle with no overlap between them. Both devices feature 375 ps typical propagation delay with greater than 70 mA of output current drive capability. 150 ps output transition times and <50 ps output delay skew makes them ideally suited for driving a variety of capacitve loads with precision timing and high signal quality. The high gain differential input provides sensitivity to low level analog signals as well as ECL and GaAs levels. A convenient on-chip -1.3V supply (VBBS) can be strapped to either input when the device is driven single-ended from ECL or GaAs logic. The 10G012B/10G013 can be driven with up to 1.75 GHz input signals. Operation to >2.5 GHz is permissable but will result in less than 1Vp-p output signal swing. Small signal unity gain is approximately 2.0 GHz.

The 10G012B/10G013 are members of GigaBit's family of PicoLogic GaAs digital ICs and are fabricated using GigaBit's high volume GaAs MESFET process technology.





10G012B/10G013 ORDERING INFORMATION

Pkg. Type	SPEED (min. 0°C to 85°C)			
	10G012B		10G013	
	1.75 GHz	1.5 GHz	1.75 GHz	1.5 GHz
C L X	10G012B-C 10G012B-L	10G012B-3C 10G012B-3L 10G012B-3X	10G013-C 10G013-L	10G013-3C 10G013-3L 10G013-3X

10G012B/10G013 OPERATION

The 10G012B and 10G013 feature several control pins which allows the user to tailor their performance in a wide variety of applications.

VBB & VBBS

The VBB input should be connected to the threshold of the signal applied to the input whether it is single ended or differential. When driving from PicoLogic, this threshold level is VBBS (nom. -1.3V), and the VBB input must be connected to the VBBS output pin. When the 10G012B/10G013 are driven single ended from ECL, the VBB input and either the -D or +D input (whichever is used as the switching reference level) should be connected to the ECL VBB threshold reference voltage. This will insure that the ECL and PicoLogic thresholds will track across the interface so that maximum signal noise immunity is maintained. Similarly, when the 10G012B or 10G013 is driven from an analog signal source with an arbitrary threshold voltage (within the common mode range) applied to one of the two D inputs, this same reference voltage must also be connected to the VBB input. Unlike other PicoLogic devices, the10G012B/10G013 VBB input does not set the device input switching threshold level. It is used only as the reference input to the device's auto-balance circuit.

OFSADJ (Input Offset Adjust)

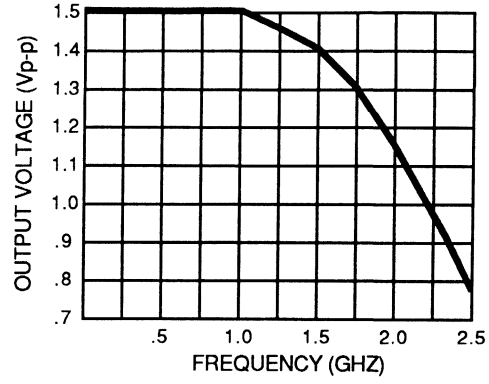
This input pin allows the input offset voltage of either part to be nulled. This may be easily accomplished by applying a ≤50 mV sinewave signal centered at -1.3V (or other level within the common mode range) to the +D input, with the -D input set to the samedc level, and varying OFSADJ in the range -6.0V≤OFSADJ≤-4.5V to produce a 50% duty cycle output. Because of the very high gain of these devices at even 1 GHz, it may be impractical to adjust the input offset by setting both +D and -D inputs to the same voltage level since the output is likely to oscillate betweeen high and low states.

OPD (Output Pull Down)

When OPD is connected to VSS, the outputs of both comparators are actively pulled low, with an approximate 10-15 mA current sink, without need for an external pull-down resistor to VTT. This simplifies the cascading of multiple devices when the interconnecting line length is kept short (≤0.2 in.). When interfacing to TTL/CMOS, if OPD is not desired it must be connected to +5.0V.

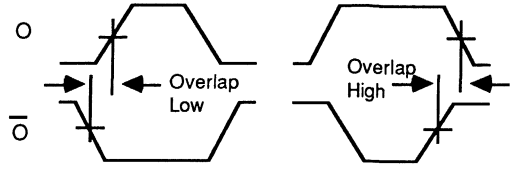
OPERATING FREQUENCY

The graph below shows peak-to-peak output voltage vs. frequency for a1Vp-p sinewave input. This illustrates that the 10G012B/013 are useable to higher frequencies than their top 1.75 GHz rating if some degradation in the output peak to peak level is permissable and allowing for a VOL level more positive than -1.7V. For a 1 Vp-p input, 1 Vp-p is available at the output to beyond 2.0 GHz although VOL will increase slightly above -1.7V.



10G013 OUTPUT OVERLAP PROGRAMMING

In clock buffering applications, it is useful to create overlap-low or overlap-high output phases of the input clock signal. Overlap-low means that the O and $\overline{O}$ outputs are both low for part of each input clock cycle, and are never simultaneously high. Overlap-high means that O and $\overline{O}$ are both high for some part of the clock cycle, and are never both low. This is illustrated in the diagram below. Pins OLAP1, OLAP2 and OLADJ (Overlap Adjust) control the amount of overlap between O and $\overline{O}$ outputs. Adjusting the output overlap via these three controls simultaneoulsly changes the duty cycle of the complementary outputs in opposite directions.

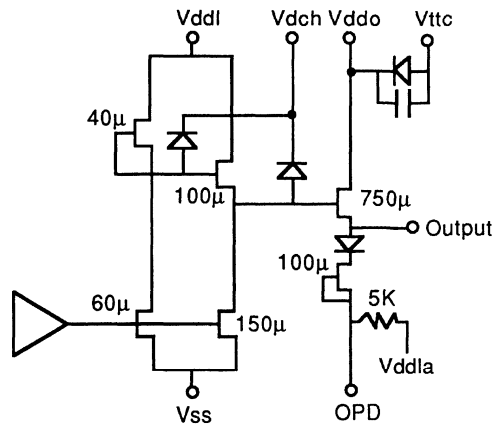


Since the overlap controls change the input threshold of the two differential inputs equally, the amount of overlap adjustment is directly proportional to the input signal rise and fall times. Fast input edge rates result in a small overlap adjustment range. 10G013 output overlap is programmed according to the table below:

Output Overlap	OLAP1	OLAP2	OLADJ
Adjustable from low to 0 to high	VEE	Open	VEE to VSS
Extra overlap high	VEE	VEE	VEE to VSS
No overlap	VEE	Open	ALAP

With OLAP1 set to VEE and OLAP2 left open, the amount of output overlap can be adjusted from overlap low to no overlap to overlap high by varying the voltage on pin OLADJ from VEE to VSS. Additional overlap high can be realized by setting OLAP2 to VEE. Zero output overlap can be set by connecting the OLADJ pin to the ALAP output pin with OLAP1 at VEE and OLAP2 open. This configures the 10G013 to operate the same as the 10G012B.

10G012B/10G013 OUTPUT CIRCUIT



PIN DESCRIPTIONS

+D	True data input.
-D	Complementary data input.
VDDO	Output driver ground connection. VDDOA and VDDOB are electrically separate.
VDDL	Logic ground connection. VDDLA and VDDLB are electrically separate.
VSS	- 3.4 V power supply
VEE	- 5.2 V power supply
OFSADJ	Input offset trim. (See text)
VDCH	Output driver high level clamp voltage. When driving other GaAs devices, VDCH is generally left unconnected. When driving ECL, VDCH may be used to limit VOH. See App. Note 4 for detail.
OLAP1, OLAP2	Used to adjust output overlap. (See text)
OLADJ	Overlap adjust input. (See text).
O	True data output.
$\overline{O}$	Complementary data output.
OPD	Active pull down for outputs. Leave open or connect to VSS. OPD can also be used in combination with an external pulldown resistor. Tie OPD to +5 V for TTL output interface.
ALAP	Auto-balance circuit output. Connect to OLADJ for zero output overlap.
VBB	Input signal threshold reference input to the auto-balance circuit.
VBBS	PicoLogic/ECL threshold reference voltage output (nom. -1.3V). Note that VBBS is derived from VDDLA. Therefore the A side must be powered to obtain VBBS.

DC CHARACTERISTICS

Tc = 0°C to 85°C, VSS = -3.5V to -3.3V, VEE = -5.5V to -5.1V, VDDL=VDDO = 0V, unless otherwise indicated.

Symbol	Parameter	Min	Typ	Max	Units	Test Conditions
I in	Input current	-100	60	200	µA	VIN = -1.0V to -1.6V
VCM	Input common mode range	-1.8		-0.8	V	
ISS	Power Supply Current		75	100	mA	
IEE	Power Supply Current		37	50	mA	
PD	Power dissipation		450	600	mW	

NOTE:

The remaining DC Characteristics are specified in the 10G PicoLogic™ Family Electrical Characteristics Table at the beginning of this section. This table notes parameter deviations to Family Characteristics and provides specific supplementary characteristics only.

AC CHARACTERISTICS (Note1)

10G012B/10G013

SYMBOL	PARAMETER	Tc = 0°C		Tc = +25°C			Tc=85°C		UNITS	
		MIN	MAX	MIN	TYP	MAX	MIN	MAX		
1/T1	Max. input frequency	1.75		1.75	1.9		1.75		GHz	
T2	Input to output delay	300	500	300	350	500	300	500	ps	
T3	Delay skew		50		20	50		50	ps	
T4	Output rise time		175		125	175		200	ps	2
T5	Output fall time		150		125	150		175	ps	2

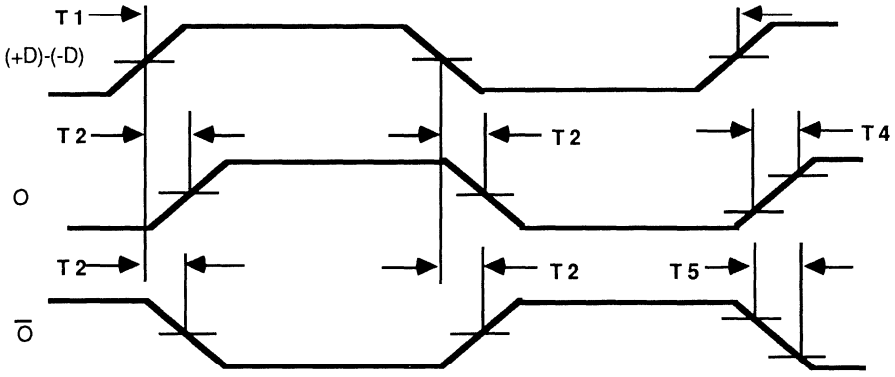
10G012B-3/10G013-3

SYMBOL	PARAMETER	Tc = 0°C		Tc = +25°C			Tc=85°C		UNITS	
		MIN	MAX	MIN	TYP	MAX	MIN	MAX		
1/T1	Max. input frequency	1.5		1.5	1.7		1.5		GHz	
T2	Input to output delay	300	500	300	375	500	300	500	ps	
T3	Delay skew		50		30	50		50	ps	
T4	Output rise time		175		125	175		200	ps	2
T5	Output fall time		150		125	150		175	ps	2

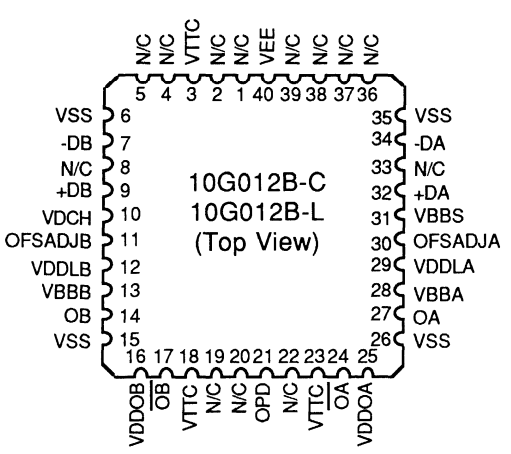
NOTES:

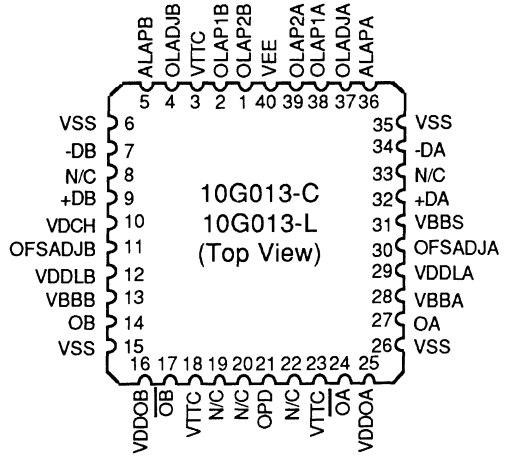
1. Test conditions (unless otherwise noted): VBB = -1.2V, VTT = -2.0V, VTTC = VTT, Rload = 50Ω to VTT, VDCH = VDDO, VIH = -0.7V, VIL = -1.7V, VOH ≥ -0.7V, VOL ≤ -1.7V, -D = -1.2V, Oladj = Autolap, Olap1 = VEE, Olap2 = N/C.
2. Output rise and fall times are measured at the 20% and 80% points of the transition from VOL max to VOH min.

SWITCHING WAVEFORMS



40 I/O PACKAGE PINOUTS - PACKAGE TYPES "L" AND "C"





GigaBit Logic **10G021A**

Dual Precision D Flip Flop
2.7 GHz Clock Rate
10G PicoLogic™ Family

DISTINCTIVE CAPABILITIES

- DC to 2.7 GHz operation
- 0°C to +85°C operating temperature range
- Ultra-low input sampling skew
- Individual clock, preset, and clear inputs on each flip flop
- Edge-triggered flip-flop design clocks on falling clock edge
- High gain ECL compatible differential inputs
- ECL and PicoLogic™ compatible complementary outputs
- Output stage supports a wide range of load resistor and termination voltage combinations
- Available in leaded or leadless chip carrier and dice form
- Packages contain internal decoupling capacitors for optimum high frequency performance

APPLICATIONS

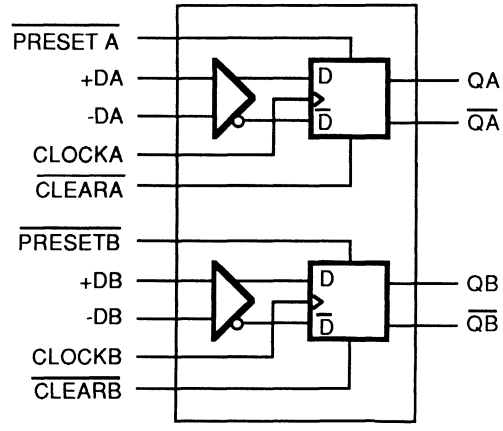
- Data repeaters/regenerators
- Decision circuits
- Synchronizers
- Data samplers

FUNCTIONAL DESCRIPTION

The 10G021A consists of two edge-triggered precision D flip-flops capable of operating at clock frequencies of over 2 GHz. Each flip-flop features individual clock, preset, and clear inputs. Each half of the 10G021A contains a high speed differential data input to which the input signal is applied. When the input stage is used as a line receiver or amplifier the data inputs can be driven differentially for maximum noise immunity. The - D input may also be used as a reference input to allow selection of the switching threshold. When the - D input is connected to an ECL generated VBB the + D input can be driven from an ECL compatible source. The complementary outputs are ECL and PicoLogic compatible, and support a wide range of load resistor and termination voltage combinations. The output driver has been designed for maximum symmetry between Q and $\overline{Q}$ output waveforms.The design of the 10G021A is such that high and low input data are sampled at the same point in time relative to the falling clock edge. This eliminates pulse lengthening or shrinking encountered with traditional D flip-flops which sample high and low data a gate delay apart in time. The 10G021A's precise data sampling translates to ultra low data sampling skew. Thus the 10G021A's output data eye pattern is highly symmetrical minimizing distortion of regenerated data.

The 10G021A is fabricated using GigaBit's high volume GaAs MESFET process technology.

BLOCK DIAGRAM



10G021A ORDERING INFORMATION

PKG. TYPE	SPEED (Min. @ 25°C)		
	2.7 GHz	2.3 GHz	1.8 GHz
C L Dice	10G021A-2C 10G021A-2L	10G021A-C 10G021A-L	10G021A-3C 10G021A-3L 10G021A-3X

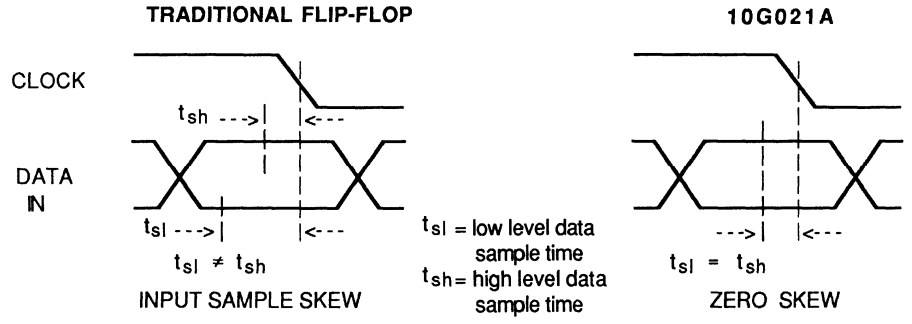
FUNCTIONAL DESCRIPTION (cont.)

The data at the D input is transferred to the Q output on the negative going edge of the clock pulse. When the clock input is at either the high or low level, the D input signal has no effect on the output. The preset and clear input signals can set the condition of the flip-flop at any time, regardless of the presence or absence of a clock edge. The detailed operation of the 10G021A is summarized in the truth table.

TRUTH TABLE

$\overline{PRESET}$	$\overline{CLEAR}$	CLOCK	DATA	Q	$\overline{Q}$
H	H	⌐	0	0	1
H	H	⌐	1	1	0
H	H	1	X	Q(t-1)	$\overline{Q}$(t-1)
L	L	NOT ALLOWED			
L	H	X	X	1	0
H	L	X	X	0	1

DATA SAMPLING



PIN DESCRIPTIONS

+D, -D	Differential data inputs. The effective data input voltage is the difference between the +D and -D inputs [i.e., (+D) - (-D)].
CLOCK	Clock input. The input sampling rate of the +D and -D inputs is equal to the CLOCK frequency.
$\overline{CLEAR}$	Active low clear input.
$\overline{PRESET}$	Active low preset input.
Q	True data output. The effective output data rate is equal to one half the CLOCK rate.
$\overline{Q}$	Complementary data output.
VDDO	Output driver ground (0V).
VDDL	Internal logic ground (0V).
VEE	- 5.2V supply voltage
VBBS	Nominal -1.2 V threshold reference supply.
VSS	- 3.4V supply voltage
VTTC	VDDO internal decoupling capacitor return. VTTC is brought into the 10G021A package as the AC return lead for the internal VDDO output driver power supply decoupling capacitor. It is not brought onto the 10G021A die. VTTC is typically equal to VTT (nominally - 2.0 V).
VDCH	Output driver high level clamp voltage. When driving other GaAs devices, VDCH is generally not used. When driving ECL, VDCH may be used to limit VOH. See Application Note 4 for details.
VTRIM	Temperature and threshold compensation voltage. Making VTRIM more or less positive relative to VEE (up to a 0.6V difference) will adjust the input threshold of the clock, preset, and clear pins.

DC CHARACTERISTICS

Tc = 0°C to 85°C, VSS = -3.5 V to -3.3 V, VEE = -5.5 V to -5.1 V, VDDL = VDDO = 0 V, unless otherwise indicated.

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	TEST CONDITIONS
VIH	Input Voltage High; Clock, Preset, Clear inputs	-0.8		VDDL	V	
VIL	Input Voltage Low; Clock, Preset, Clear inputs	VSS		-1.7	V	
IIN	Input Current	-250	225	600	µA	VIN: -0.8 V to -1.7 V
ISS	Power Supply Current	-250	-150		mA	
IEE	Power Suppy Current	-45	-20		mA	
PD	Power Dissipation		600	1100	mW	No Load

NOTE:

The remaining DC Characteristics are specified in the 10G PicoLogic™ Family Electrical Characteristics Table at the beginning of this section. This table notes parameter deviations to Family Characteristics and provides specific supplementary characteristics only.

10G021A-2

AC CHARACTERISTICS (Note 1)

VSS = -3.5V to -3.3V, VEE = -5.5V to -5.1V, VDDL=VDDO = 0V, unless otherwise indicated.

SYMBOL	PARAMETER	Tc= 0°C		Tc = +25°C			Tc= +85°C		UNITS	NOTES
		MIN	MAX	MIN	TYP	MAX	MIN	MAX		
1/T1	Max Clock Frequency	2.3		2.7			2.3		GHz	2, 6
T2	(+D)-(-D) Hold Time	0		0	-60		0		ps	
T3	(+D)-(-D) Setup Time	250		250	165		250		ps	
T4	Preset Pulse Width	750		750	500		750		ps	
T5	Preset Low to Q High		700		575	700		700	ps	
T6	Preset Low to $\overline{Q}$ Low		700		575	700		700	ps	
T7	Clear Pulse Width	750		750	500		750		ps	
T8	Clear Low to Q Low		750		625	750		750	ps	
T9	Clear Low to $\overline{Q}$ High		750		625	750		750	ps	
T10	Clock Low to Q High		625		525	625		625	ps	
T11	Clock Low to $\overline{Q}$ Low		625		525	625		625	ps	
T12	Clock Low to Q Low		625		525	625		625	ps	
T13	Clock Low to $\overline{Q}$ High		625		525	625		625	ps	
Tr	Output Rise Time		220		180	220		220	ps	3
Tf	Output Fall Time		140		125	140		140	ps	3
	Clock to Output Skew				60	75			ps	4
	Input Sample Skew				25				ps	5

10G021A AC CHARACTERISTICS (Note 1)

VSS = -3.5V to -3.3V, VEE = -5.5V to -5.1V, VDDL=VDDO = 0V, unless otherwise indicated.

SYMBOL	PARAMETER	Tc= 0°C		Tc = +25°C			Tc= +85°C		UNITS	NOTES
		MIN	MAX	MIN	TYP	MAX	MIN	MAX		
1/T1	Max Clock Frequency	2.0		2.3			2.0		GHz	2, 6
T2	(+D)-(-D) Hold Time	0		0	-50		0		ps	
T3	(+D)-(-D) Setup Time	265		265	175		265		ps	
T4	Preset Pulse Width	1000		1000	670		1000		ps	
T5	Preset Low to Q High		850		650	850		850	ps	
T6	Preset Low to $\overline{Q}$ Low		850		650	850		850	ps	
T7	Clear Pulse Width	1000		1000	670		1000		ps	
T8	Clear Low to Q Low		900		700	900		900	ps	
T9	Clear Low to $\overline{Q}$ High		900		700	900		900	ps	
T10	Clock Low to Q High		750		600	750		750	ps	
T11	Clock Low to $\overline{Q}$ Low		750		600	750		750	ps	
T12	Clock Low to Q Low		750		600	750		750	ps	
T13	Clock Low to $\overline{Q}$ High		750		600	750		750	ps	
Tr	Output Rise Time		240		200	240		240	ps	3
Tf	Output Fall Time		160		150	160		160	ps	3
	Clock to Output Skew				75	100			ps	4
	Input Sample Skew				30				ps	5

10G021A-3 AC CHARACTERISTICS (Note 1)

VSS = -3.5V to -3.3V, VEE = -5.5V to -5.1V, VDDL=VDDO = 0V, unless otherwise indicated.

SYMBOL	PARAMETER	Tc= 0°C		Tc = +25°C			Tc= +85°C		UNITS	NOTES
		MIN	MAX	MIN	TYP	MAX	MIN	MAX		
1/T1	Max Clock Frequency	1.5		1.8			1.5		GHz	2, 6
T2	(+D)-(-D) Hold Time	0		0	-40		0		ps	
T3	(+D)-(-D) Setup Time	300		300	190		300		ps	
T4	Preset Pulse Width	1300		1300	870		1300		ps	
T5	Preset Low to Q High		1150		900	1150		1150	ps	
T6	Preset Low to $\overline{Q}$ Low		1150		900	1150		1150	ps	
T7	Clear Pulse Width	1300		1300	870		1300		ps	
T8	Clear Low to Q Low		1200		950	1200		1200	ps	
T9	Clear Low to $\overline{Q}$ High		1200		950	1200		1200	ps	
T10	Clock Low to Q High		1050		850	1050		1050	ps	
T11	Clock Low to $\overline{Q}$ Low		1050		850	1050		1050	ps	
T12	Clock Low to Q Low		1050		850	1050		1050	ps	
T13	Clock Low to $\overline{Q}$ High		1050		850	1050		1050	ps	
Tr	Output Rise Time		275		250	275		275	ps	3
Tf	Output Fall Time		220		200	220		220	ps	3
	Clock to Output Skew				125	175			ps	4
	Input Sample Skew				40				ps	5

NOTES: 1. Test conditions (unless otherwise indicated):

-D = -1.2V	VDCH = VDDL	VTTC = VTT
VTT = -2.0V	VOH ≥ -0.7V	VTRIM = VEE
RLOAD = 50 Ohms to VTT	VOL ≤ -1.7V	

Data rate = one half the clock rate
Clock logic swing = 2V P/P sinusoid centered at -1.2V
Preset, Clear, and data input logic swing = 1V P/P pulse centered at -1.2V

2. 50% duty cycle at maximum clock frequency.
3. Output edge rates are specified at 20% to 80% output transition.
4. Clock to Output Skew is the maximum delay difference among T10, T11, T12, and T13.
5. Input Sample Skew is the relative difference in time between the point at which high level data and low level data are sampled by the falling edge of the Clock input.
6. Clock input rise and fall times should be less than or equal to 1 ns.

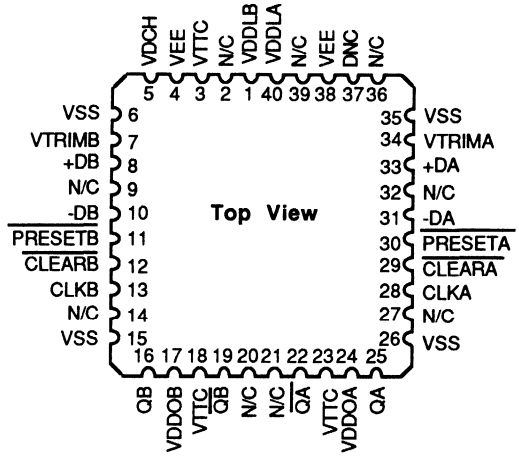
CLOCK SOURCES

GaAs logic will typically be used to drive the 10G021A CLOCK input. Alternatively, GigaBit Logic recommends the use of inexpensive VCO generators with 10 dBm or greater output power. Because ECL logic is typically limited to clock rates less than 500 MHz, the 10G021A CLOCK input will normally not be driven with ECL logic levels.

The 10G021A will operate with smaller peak to peak clock swings. The table below indicates the typical reduction in maximum clock frequency as a function of P/P sinusoidal clock levels.

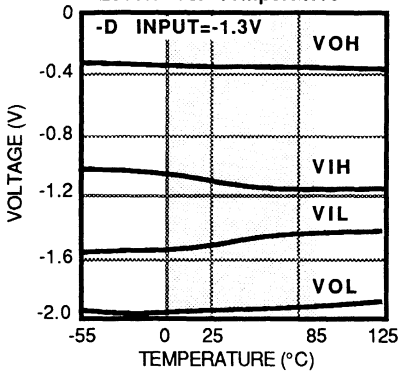
2.0V P/P	1.4V P/P	1.0V P/P
0	15%	30%

PIN FUNCTIONS - PACKAGE TYPES "C" OR "L"

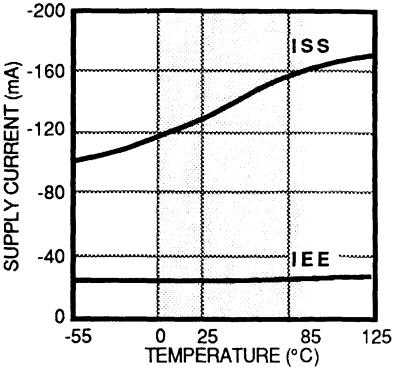


TYPICAL PERFORMANCE CHARACTERISTICS

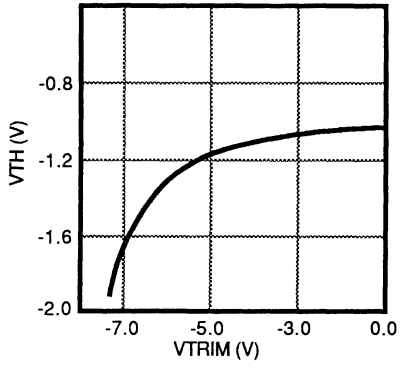
Data Input and Q Output Levels vs. Temperature



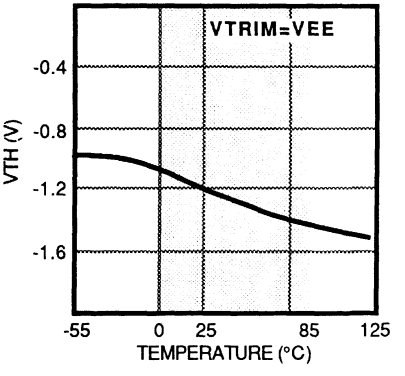
ISS & IEE vs. Temperature



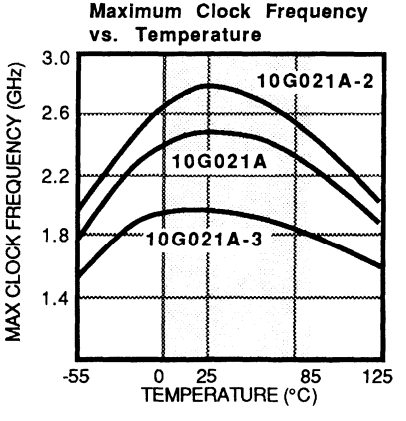
Clock, Preset, & Clear Threshold Voltage vs. VTRIM



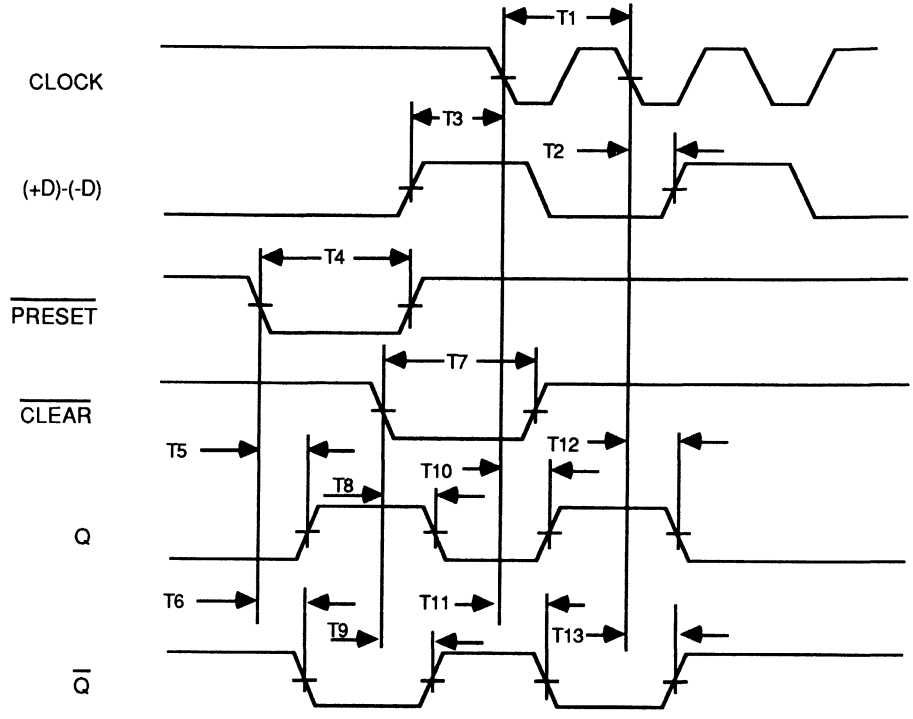
Clock, Preset, & Clear Threshold Voltage vs. Temperature



Maximum Clock Frequency vs. Temperature

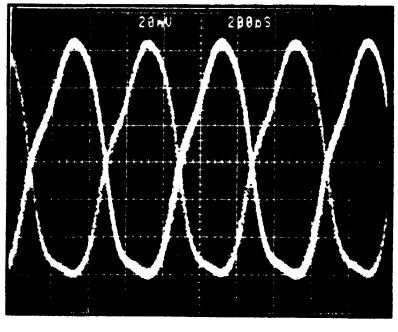


SWITCHING WAVEFORMS

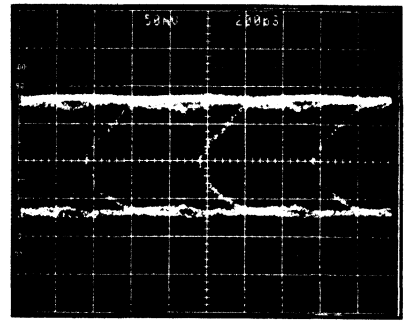


TYPICAL OUTPUT WAVEFORMS

10G021A Q Output Eye Pattern
2.5 GHz Clock Rate
Sinusoidal data rate = 1.25 GHz
(corrected vertical = 200mV/div.)



10G021A Q Output Eye Pattern
Data Input = 1.6 Gbps 2^7 - 1 pseudorandom bit stream generated by the 10G040 Multiplexer
1.6 GHz Clock Rate
(corrected vertical = 500 mV/div.)



Octal Register/Shift Register/PN Code Generator
1.5 GHz Clock Rate
10G PicoLogic™ Family

DISTINCTIVE CAPABILITIES

- 150ps typ. output rise and fall times
- Serial/parallel mode selection via the high speed mode select input (PAR/$\overline{SER}$)
- On-chip P/N code generation capability permits generation of >1Gbit/s pseudo-random bit streams
- ECL and 10G PicoLogic compatible I/O
- Temperature and voltage compensated using VBB threshold reference input
- On-chip VBBS (-1.2V) reference voltage supply
- 8 edge triggered flip-flop stages, inputs are latched on the rising edge of the clock
- Active high output enable control (OUTEN)
- Active low output reset control ($\overline{RESET}$)
- Additional serial input ($\overline{DSO}$) and output (OUT 7) for cascading multiple 10G022's
- Available in C-leaded or leadless chip carrier or dice form
- Packages contain internal decoupling capacitors for optimum high frequency performance

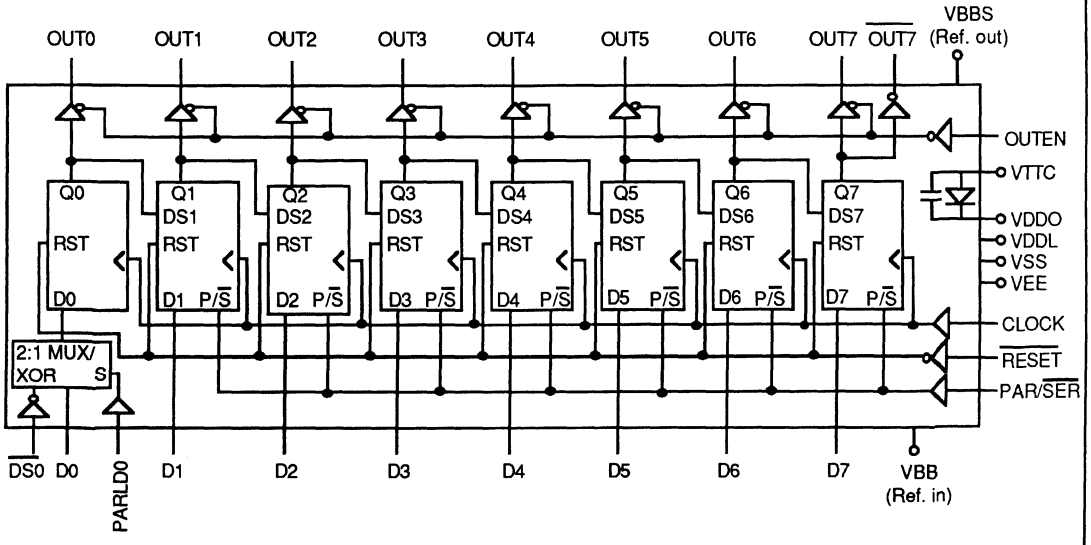
APPLICATIONS

- High resolution displays
- Digital RF memory
- High speed scramblers
- Convolutional and block encoders/decoders
- P/N code generation
- Testing
- Modulo N counters
- Spread spectrum systems

10G022 ORDERING INFORMATION

PACKAGE TYPE	SPEED (Min. 0°C to 85°C)	
	1.5 GHz	1.0 GHz
C-leaded CC	10G022-2C	10G022-3C
Leadless CC	10G022-2L	10G022-3L
Dice		10G022-3X

10G022 BLOCK DIAGRAM



PIN DESCRIPTIONS

SYMBOL	DESCRIPTIONS
D0 to D7	External parallel data inputs.
DS0	Serial input data. (inverted)
PARLD0	Control input to stage #0; it selects between DS0 or D0 data inputs. If PARLD0=HI, D0 is selected (next Q0=D0). If PARLD0=LO, $\overline{DS0}$ is selected (next Q0=$\overline{DS0}$).
PAR/SER	Select input. If PAR/$\overline{SER}$ = HI, the 10G022 is in the parallel mode (next Qn = Dn, for n =1 to 7). If PAR/$\overline{SER}$ = LO, the 10G022 is in the serial mode (next Qn = Q_{n-1}, for n = 1 to 7).
CLOCK	Buffered high speed clock input to every stage of the register. The low to high transition causes data to be latched.
OUTEN	Control input. Enables or disables the outputs (OUT0-OUT7). OUTEN = HI gives OUTn = Qn; OUTEN = LO gives the OUTn = LO disable condition for a wired-OR bus.
$\overline{RESET}$	Reset input. When LO, it resets all stages of the 10G022.
OUT0 to OUT7	Outputs from stages 0 thru 7. These outputs can be enabled or disabled under control of OUTEN.
$\overline{OUT7}$	Complement output from stage 7, continuously enabled.
VDDO	Output driver ground (0V)
VDDL	Internal logic ground (0V)
VSS	-3.4V power supply
VEE	-5.2V power supply
VTTC	VDDO internal decoupling capacitor return. VTTC is brought into the 10G022 package as the AC return lead for the internal VDDO output driver decoupling capacitor. It is not brought onto the 10G022 die. VTTC is typically tied to VTT (nominally -2.0V).
VDCH	Output driver high level clamp voltage. When driving other GaAs devices, VDCH is generally left unconnected.
VBB	Input to the 10G022's input threshold tracking circuit. Connect to the VBB supplied from ECL when driving from ECL. Connect to VBBS when the 10G022 is driven from PicoLogic™. This pin may not be left unconnected.
VBBS	PicoLogic™ threshold reference voltage supply. Nominally equal to -1.2V with a 40 source impedance. Connect to VBB when interfacing with PicoLogic.

FUNCTIONAL DESCRIPTION

The 10G022 is an ECL and 10G PicoLogic™ compatible ultra fast universal register that can be configured as an 8 stage cascadable shift register, an 8 bit parallel register or as a pseudo-random bit stream generator. It is designed specifically to support high speed bus applications, digital RF memory and pipelined architecture systems. The device features a worst case clock to output propagation delay of 850ps at room temperature and is typically capable of a max clock frequency of 1.7 GHz. Output rise and fall times are typically 150ps. As a member of GigaBit Logic's 10G family of PicoLogic IC's, the 10G022 is fabricated with GigaBit's high volume, production proven GaAs MESFET process technology.

Targeted for bus applications, the 10G022 features an output enable pin - OUTEN. When the outputs are disabled (OUTEN = LO), the information in each stage of the register is retained and the outputs will be disabled. In addition, the 10G022 is equipped with an asynchronous reset pin $\overline{RESET}$ which is capable of resetting all stages of the register. A LO signal on the $\overline{RESET}$ pin overrides all other inputs and forces all outputs LO except for $\overline{OUT7}$ which is forced HI. Operation of the $\overline{RESET}$ control is independent of the clock or any other pins.

A built- in XNOR gate in its serial input allows the 10G022 to be used as a high speed P/N code generator. In this mode it is ideally suited for applications that require the generation of long patterns of pseudo-random words at very high speeds e.g. testing, data scrambling, convolutional encoding and spread spectrum systems. A separate serial input to the first stage (DSO) and an output from the last stage (OUT7) facilitate cascading N, 10G022 registers to form a chain of serial registers, 8N bits long.

Since the output logic threshold level of various ECL and GaAs families will shift differently with temperature and supply voltage variation, the 10G022's input circuit is designed to track these movements. This is easily accomplished by connecting the interfacing logic family's threshold voltage to the 10G022's VBB input pin. This enables the 10G022's input threshold to track movements in the threshold of devices connected to it, resulting in maximum noise immunity and minimum signal distortion over temperature and supply voltage variation. Some ECL devices (e.g. 10114, 10115, 100114, 100125) and all second generation PicoLogic devices make the logic threshold level available on an output pin. In ECL it is termed VBB, and in

FUNCTIONAL DESCRIPTION (cont.)

PicoLogic™ it is referred to as VBBS. If unavailable, this voltage can be generated by connecting the terminated output of an inverting gate back to its input with suitable filtering of the output to prevent oscillation.

When PicoLogic is used to drive the 10G022, the VBBS pin must be strapped to the VBB pin for proper device operation. Connecting VBBS to the VBB input is also appropriate, in some cases, for non-PicoLogic device interfaces. Examples of these are ECL-to-10G022 interface over a limited temperature range or when driving the 10G022 from another GaAs device since GaAs logic output swings are significantly higher than ECL output swings.

FUNCTIONAL DESCRIPTION (cont.)

Depending upon user choice of load resistor and termination voltage (Vtt), the output high level (VOH) generated by the 10G022 may require limiting when the 10G022 drives ECL logic. One way to limit VOH is through the use of the output driver high level clamp diode which is brought out on pin VDCH. Other methods are explained in Application Note 4.

The 10G022 can function in the following modes:

- Parallel data in - parallel out
- Parallel data in - serial out
- Serial data in - parallel out
- Serial data in - Serial out
- P/N Code Generator

The state table for each of these modes is given below.

MODE STATE TABLE (note1)

MODE DESCRIPTION	($\overline{DS0}$)	D0 - D7	PAR/$\overline{SER}$ (Note 2)	PARLD0 (note 2)	OUTEN	$\overline{RESET}$	CLK	OUT0 - OUT7	$\overline{OUT7}$
8 Bit Parallel In/Parallel Out	X •	D0=(D0)n+1 • • • D7=$(D7)_{n+1}$	PAR/$\overline{SER}$=PARLD0=HI		HI	HI	⎍••	OUT0=$(D0)_{n+1}$ • • • • • • OUT7=$(D7)_{n+1}$	$\overline{OUT7}$ = $\overline{(D7)_{n+1}}$
8 Bit Serial In/Parallel, Serial Out	$\overline{DS0}$=$\overline{(DS0)_{n+1}}$	D0=X • • D7=X	PAR/$\overline{SER}$=PARLD0=LO		HI	HI	⎍	OUT0=$\overline{(DS0)_{n+1}}$ OUT1=(OUT0)n OUT2=(OUT1)n • • • • • • OUT7=(OUT6)n	$\overline{OUT7}$ = $\overline{(OUT6)_n}$
8 Bit Serial In/ Serial Out	$\overline{DS0}$=$\overline{(DS0)_{n+1}}$	D0=X • • D7=X	PAR/$\overline{SER}$=PARLD0=LO		LO	HI	⎍	OUT0=LO • • • • OUT7=LO	$\overline{OUT7}$ = $\overline{(Q6)_n}$
8 Bit P/N Code (Note 3) Generator	$\overline{DS0}$=D0=Qy D1=X D7=X	D0=$\overline{(DS0)}$=Qy	PAR/$\overline{SER}$=LO	PARLD0=QX	HI	HI	⎍		
Reset State (Reset=active)	X	X	X	X	X	LO	X	OUT0=LO • • • • OUT7=LO	$\overline{OUT7}$ = HI

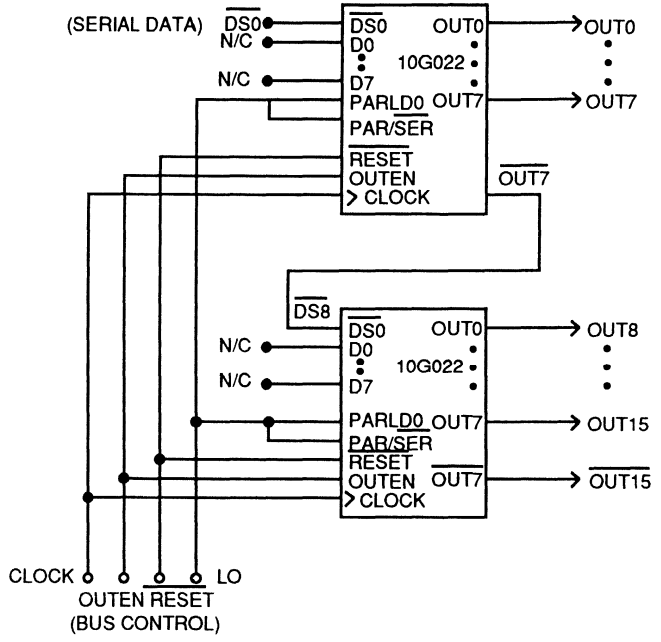
NOTES:

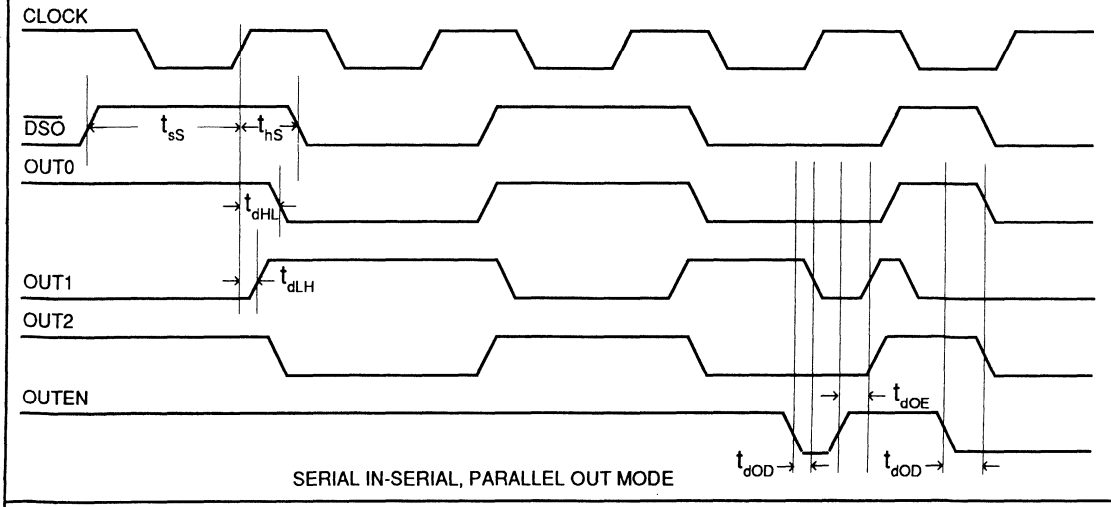
1) The subscript n+1 indicates the new logic value.
   For the outputs it means the new value of the output after the rising edge of the clock.
2) The pins PAR/$\overline{SER}$ and PARLD0 must be tied together in all cases except when the 10G022 is used as a P/N code generator.
   When PAR/$\overline{SER}$=PARLD0=LO the 10G022 operates as a shift register.
   When PAR/$\overline{SER}$=PARLD0=HI the 10G022 operates as a parallel in - parallel out register.
3) In the P/N code generator mode, the serial input $\overline{DS0}$ and D0 must be connected together. The inputs to the internal XNOR gate are $\overline{DS0}$ and PARLD0. See example following.

Serial In-Serial/Parallel Out Mode (8 BIT CASCADABLE SHIFT REGISTER)

When the 10G022 is operated in the serial in - serial, parallel out mode PAR/SER = PARLD0 and OUTEN = HI. The data inputs D0-D7 have no effect and DS0 may be fed from the (OUT7) output of another lower order similar (10G022) serial register. The (OUT7) output is continuously active despite the state of OUTEN, providing the necessary serial data for a higher order (10G022) shift register.

When the 10G022 is operated in the serial in - serial out mode the only difference is that OUTEN = LO disables the outputs. The only active output will then be OUT7.





SERIAL IN-SERIAL, PARALLEL OUT MODE

An option for faster 10G022 operation as a shift register (serial in - serial, parallel out) is to enable all parallel outputs (OUTEN = HI) with the serial connection between two registers formed when OUT7 of the less significant stage connects to D0 of the more significant one. During this mode of operation, PARLD0 is held HI and PAR/SER = LO. Stages of shift registers connected in this manner operate faster than as described above.

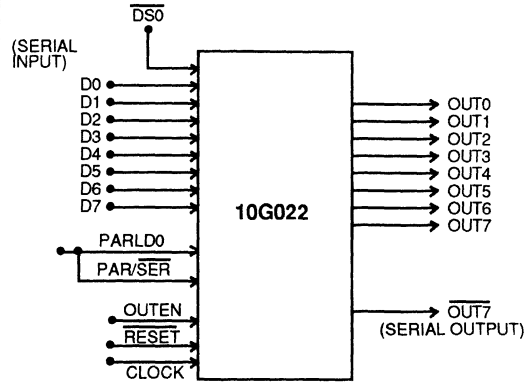
PARALLEL IN-PARALLEL OUT MODE (8 Bit Parallel Register)

When the 10G022 is operated in the parallel in-parallel out mode, PAR/$\overline{SER}$ = PARLD0 = HI. The data at the inputs D0-D7 are latched on the rising edge of the clock. If OUTEN = HI, the data will appear at the outputs in their true form.

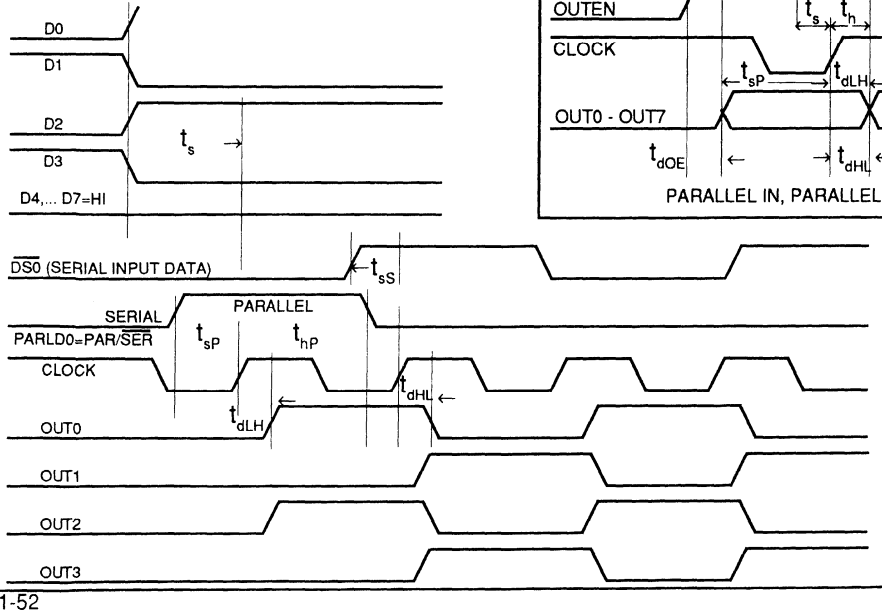
When the output enable is low (OUTEN = LO) the device remains fully functional with all data retained except that the outputs O_0 - O_7 are low, allowing wired-OR bus operation.

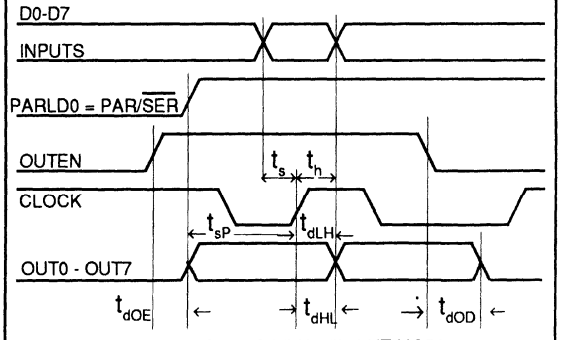
PARLD0 controls only the first stage of the register, while PAR/$\overline{SER}$ controls the remaining seven stages. PARLD0 = HI selects data from D0, while PARLD0 = LO selects (inverted) data from $\overline{DS0}$. For the remaining stages PAR/$\overline{SER}$ = LO selects data from the previous stage.

Many applications will employ the 10G022 in the parallel in-serial out mode. In this mode, a parallel word is latched and then serially shifted out. This operating mode is shown below.



PARALLEL IN, SERIAL OUT MODE

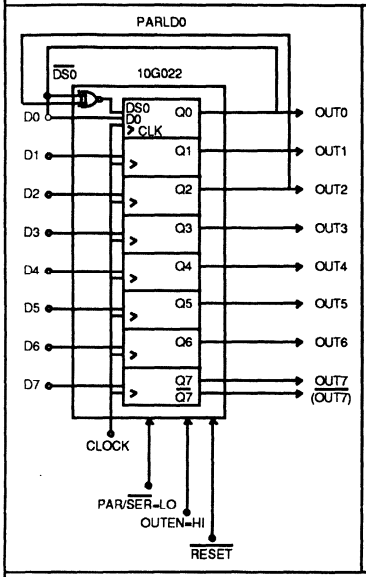




PARALLEL IN, PARALLEL OUT MODE

P/N Code Generator MODE

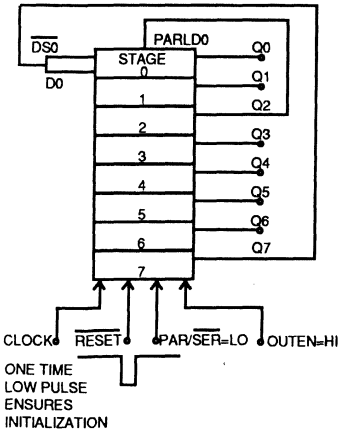
When PAR/$\overline{SER}$ = LO and $\overline{DS0}$ = D0 the 10G022 operates in the P/N code generation mode. The built-in exclusive NOR gate feeds the serial input of the first stage. The inputs of this XNOR gate are $\overline{DS0}$ and PARLD0. These two inputs can be driven from any of the outputs of the register, thus generating the desired random pattern. An example is shown below and instructions are given for generating various length P/N codes using one 10G022.



CLOCK PULSE	OUT0	OUT1	OUT2	OUT3	OUT4	OUT5	OUT6	OUT7
RESET→	0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	0	0
2	1	0	0	0	0	0	0	0
3	0	1	0	0	0	0	0	0
4	1	0	1	0	0	0	0	0
5	1	1	0	1	0	0	0	0
6	0	1	1	0	1	0	0	0
7	0	0	1	1	0	1	0	0

EXAMPLES:

Use of the 10G022 register as a P/N code generator using the built-in XNOR function at stage 0.



N=3 STAGES: Maximal length P/N code:
Feedback to the XNOR gate (Taps) from Q1 and Q2:
7 bit pattern (1101000)

N=4 STAGES: Maximal length P/N code:
Taps at Q0 and Q3:
15 bit pattern (101001101110000)

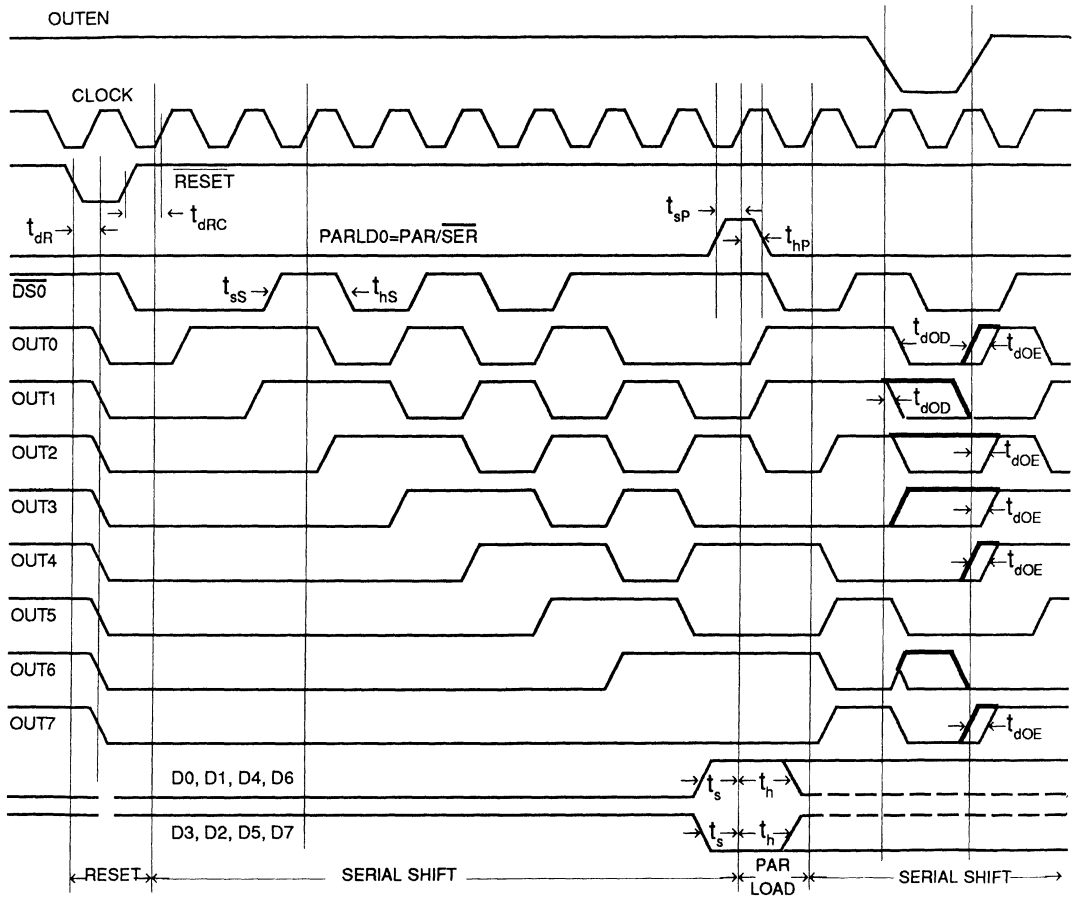
N=5 STAGES: Taps at Q1 and Q4:
31 bit pattern: (11001011011110101000100111000000)

N=6 STAGES: Taps at Q0 and Q5:
63 bit pattern:
(101010011001000100101101100011101000011010111001111011111000000)

N=7 STAGES: Taps at Q5 and Q6 gives maximal length P/N code
(2^7 -1=127 bits).

N=8 STAGES: It is not possible to achieve maximal (255 bit) length with only a single XNOR . Non maximal length: Taps at Q2 and Q7, gives a 217 bit code.

SWITCHING WAVEFORMS SUMMARY



SERIAL, PARALLEL IN-OUT MODE

internal transitions

opposite transition on the inputs

AC CHARACTERISTICS (Note 1)

VSS = -3.5V to -3.3V, VEE = -5.5V to -5.1V, VDDL=VDDO=Gnd, unless otherwise indicated.

SYMBOL	PARAMETER	10G022-2 Tc = 0°C to 85°C			10G022-3 Tc = 0°C to +85°C			UNITS	NOTES
		MIN	TYP	MAX	MIN	TYP	MAX		
fcSP	Clock frequency (serial and parallel modes)	1.5	1.7		1.0	1.2		GHz	
fcPN	Clock frequency (P/N code generator mode)		1.1			1.0		GHz	3
tsS	Setup time ($\overline{DS0}$ serial input)	0			0			ps	
thS	Hold time ($\overline{DS0}$ serial input)	250			250			ps	
ts	Setup time (parallel data inputs)	0			0			ps	
th	Hold time (parallel data inputs)	300			300			ps	
tsP1	Setup time (PAR/$\overline{SER}$)	75			75			ps	
tsP2	Setup time (PARLD0)	0			0				
thP1	Hold time (PAR/$\overline{SER}$)	100			100			ps	
thP2	Hold time (PARLD0)	350			350				
tdOE	Output enable delay time	400		700	450		800	ps	
tdOD	Output disable delay time	550		900	550		950	ps	
tdLH	Time delay (rising edge of clock to data outputs). Low to High	500		800	500		900	ps	
tdHL	Time delay (rising edge of clock to data outputs). High to Low	550		850	550		950	ps	
tdR	Time delay (falling edge of $\overline{RESET}$ to falling edge of outputs.)	750		950	750		1000	ps	
twR	$\overline{RESET}$ pulse width	600			600			ps	
tdRC	$\overline{RESET}$ release to clock delay	50			50			ps	
tr	Output rise time	100		200	100		200	ps	2
tf	Output fall time	100		150	100		150	ps	2

Notes: 1. Test conditions (unless otherwise indicated) :

VBB = -1.2V VDCH = VDDO VIH = -0.7V
VTT = -2.0V VIL = -1.7V
VTTC = VTT VOH ≥ -0.7V
RLOAD = 50Ω to -2.0V VOL ≤ -1.7V
Input signal rise and fall times ≤ 150 ps

2. Rise and fall times are measured at the 20% and 80% points of the transition from VOL max to VOH min.
3. Dependent upon feedback path from OUTn to XNOR inputs.

DC CHARACTERISTICS

Tc = 0°C to 85°C, VSS = -3.5V to -3.3V, VEE = -5.5V to -5.1V, VDDL = VDDO = Gnd unless otherwise indicated.

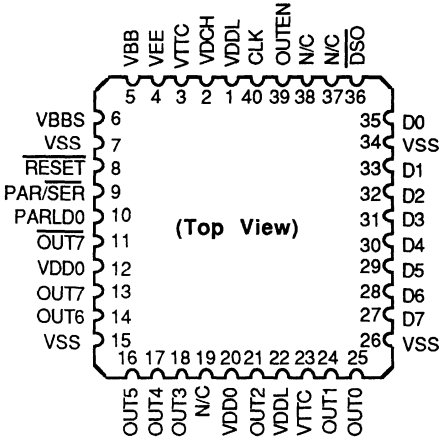
SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
VBBS	Threshold Reference Voltage		-1.2		V
ISS	Power Supply Current		340	490	mA
IEE	Power Supply Current		20	40	mA
PD	Power Dissipation		1.3	1.9	W

NOTE:

The remaining DC Characteristics are specified in the 10G PicoLogic™ Family Electrical Characteristics Table at the beginning of this section. This table notes parameter deviations to Family Characteristics and provides specific supplementary characteristics only.

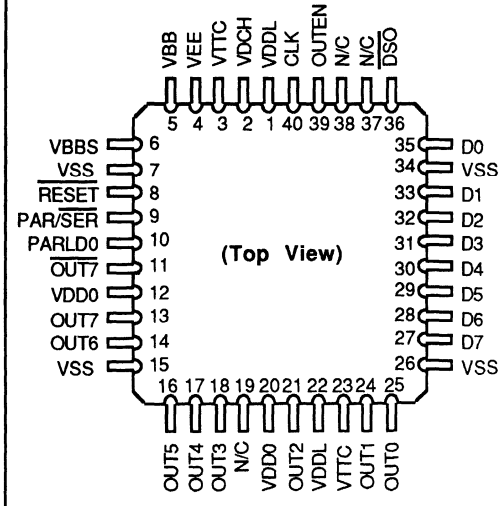
PACKAGE PINOUT DIAGRAMS

PACKAGE TYPE "L"



NOTES: Pin 1 is marked for orientation. N/C = No Connection.

PACKAGE TYPE "C"



NOTES: Pin 1 is marked for orientation. N/C = No Connection.

Quad D Flip Flop with 2:1 Muxed Inputs 1.9 GHz Clock Rate

10G PicoLogic™ Family

DISTINCTIVE CAPABILITIES

- 850 ps typical clock to output delay
- Individual or common clock inputs
- Differential outputs with common output enable control
- Common asynchronous clear control
- Temperature and voltage compensated design
- ≤ 50 ps clock to output delay skew
- ECL and PicoLogic™ compatible I/O
- Ouput Wire-OR capability
- Available in C-Leaded or Leadless chip carriers or dice form

APPLICATIONS

- Registered data or address MUX
- Pipeline register
- High speed state machines
- High speed status register

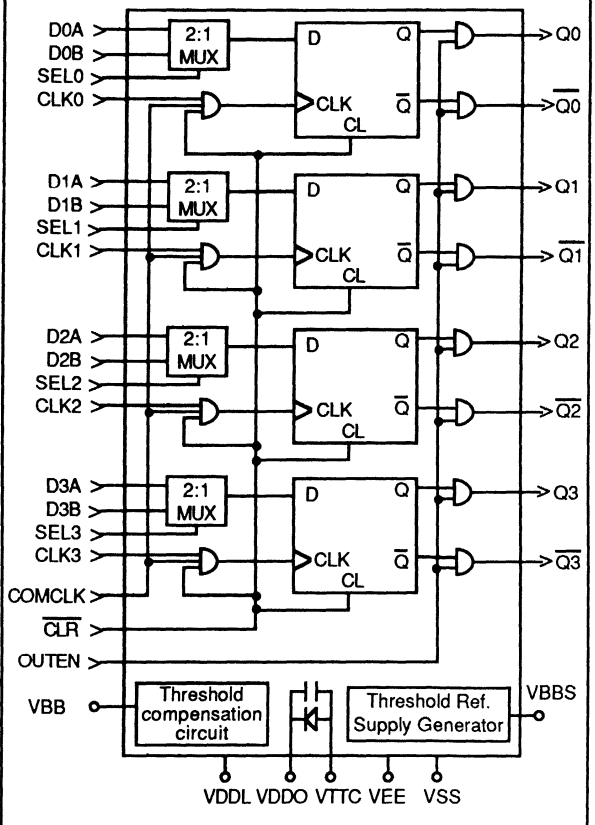
FUNCTIONAL DESCRIPTION

The 10G023 is an ultra-high speed quad D-type flip flop with individually 2:1 multiplexed data inputs (D0A-D3A, D0B-D3B). Data to each of the four stages is selected by an individual select control (SEL0-SEL3) and is latched into the flipflop by the rising edge of either the individual clock inputs (CLK0-CLK3) or the common clock input (COMCLK). An active low common clear ($\overline{CLR}$) input is provided for resetting the Q output of each flip flop asynchronously to a low level. All device outputs can be disabled (brought low), without interfering with the current state of the flip flop, via the output enable (OUTEN) control. This permits wired-OR bus connection.

The 10G023 can be clocked at 2.1 GHz typically. The operating frequency of the SEL input is much greater than half the clock frequency. Typical clock to output delay is 850 ps and the skew in output delay time is tightly matched to 30 ps typically which results in a highly symmetric output eye pattern.

The 10G023 is a member of GigaBit's Picologic family of GaAs digital ICs and is fabricated using GigaBit's high volume GaAs MESFET process technology.

BLOCK DIAGRAM



10G023 ORDERING INFORMATION

PACKAGE TYPE	SPEED (Min. 0°C to 85°C)	
	1.9 GHz	1.6 GHz
C-Leaded CC	10G023-2C	10G023-3C
Leadless CC	10G023-2L	10G023-3L
Dice		10G023-3X

10G023 OPERATION

Truth Table

Function	SELn	$\overline{CLR}$	OE	CLKn	COMCLK	DnA	DnB	Output Qn (t+1)
Clear*	X	L	H	X	X	X	X	L
Output Disabled	X	H	L	L or H	L or H	X	X	L
Output Enabled	X	H	H	L or H	L or H	X	X	Qn(t)
Select A	H	H	H	⎍⎍	H	DnA(t)	X	DnA(t)
Select B	L	H	H	⎍⎍	H	X	DnB(t)	DnB(t)
Select A	H	H	H	H	⎍⎍	DnA(t)	X	DnA(t)
Select B	L	H	H	H	⎍⎍	X	DnB(t)	DnB(t)
Clock Disabled	X	H	H	L	⎍⎍	X	X	Qn(t)
Clock Disabled	X	H	H	⎍	L	X	X	Qn(t)

* The $\overline{CLR}$ control gates the clock inputs. Therefore, when both CLKn and COMCLK are high, resetting $\overline{CLR}$ by returning it to its high state will cause data at the input pins to be clocked into the flip flops at the rising edge of $\overline{CLR}$.

The operation of the 10G023 is described in the truth table above. All flip flop stages are reset to low by bringing $\overline{CLR}$ low at any time. All outputs can be forced low for bus connection, without altering the current state of the flip flops, by bringing OUTEN low. The clock should not transition high when OUTEN is brought low so that the output state of each flip flop is maintained. When SEL is high, A Data are selected assuming both SEL and Data setup and hold time requirements are met. Setting SEL low selects the B Data inputs. At any time, the clock input can be disabled by setting the unused clock input(s) low. The current output state of each flip flop is maintained in this case.

PIN DESCRIPTIONS

D0A - D3A	A data inputs
D0B - D3B	B data inputs
SEL0 -SEL3	2:1 MUX select inputs
CLK0 - CLK3	Individual flip flop clock inputs
$\overline{COMCLK}$	Common clock input to all four flip flops
$\overline{CLR}$	Active low asynchronous clear control
OUTEN	Active high output enable control
Q0 - Q3	True data outputs
$\overline{Q0}$ - $\overline{Q3}$	Complement data outputs
VDDO	Output driver ground pin (0V)
VDDL	Internal logic ground connection (0V)
VSS	-3.4 V power supply
VEE	-5.2 V power supply
VTTC	AC return lead for the package internal VDDO decoupling capacitor. Typically connect to VTT.
VDCH	Output driver high level clamp voltage. When driving other GaAs devices, VDCH is generally left unconnected. When driving ECL, VDCH may be used to limit VOH. Consult Application Note 4 for detail.
VBB	Reference input to the 10G023's input threshold compensation circuit. Connect to the VBB supplied from ECL when driving the 10G023 from ECL. Connect to the VBBS pin when the 10G023 is driven from PicoLogic™. This pin may not be left unconnected.
VBBS	PicoLogic™ threshold reference output voltage. Nominally equal to -1.3V with a 40Ω source impedance. Connect to VBB when driving from PicoLogic™. ΔVBBS/ΔTemp = 0.6mV/°C; ΔVBBS/ΔVSS = 0.2 mV/mV.

DC CHARACTERISTICS

Tc = 0°C to 85°C, VSS = -3.5 V TO -3.3 V, VEE = -5.5 TO -5.1 V, VDDL = VDDO = Gnd, unless otherwise indicated

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	TEST CONDITIONS
I in 1	Input Current; Data, Sel, CLKn		200	500	µA	VIN = -1.0 V to -1.6 V
I in 2	Input Current; COMCLK, $\overline{CLR}$, OUTEN		500	1000	µA	
ISS	Power Supply Current		260	340	mA	
IEE	Power Supply Current		35	65	mA	
PD	Power Dissipation		1.0	1.5	W	

NOTE:

The remaining DC Characteristics are specified in the 10G PicoLogic™ Family Electrical Characteristics Table at the beginning of this section. This table notes parameter deviations to Family Characteristics and provides specific supplementary characteristics only.

AC CHARACTERISTICS (Notes 1, 2)

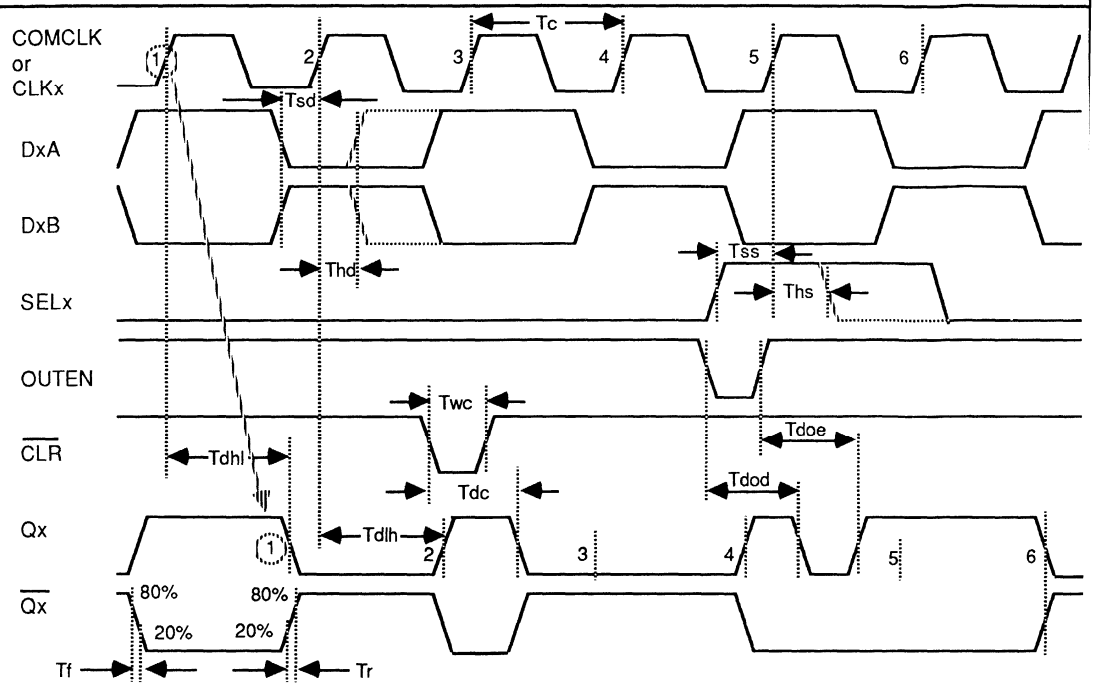
VSS= -3.5V to -3.3V, VEE= -5.5V to -5.1V, VDDL=VDDO=Gnd., unless otherwise indicated

		10G023-2							10G023-3							
SYMBOL	PARAMETER	Tc= 0° C		Tc= 25° C			Tc= 85° C		Tc= 0° C		Tc= 25° C			Tc= 85° C		UNITS
		MIN	MAX	MIN	TYP	MAX	MIN	MAX	MIN	MAX	MIN	TYP	MAX	MIN	MAX	
1/Tc1	Individual clock freq.	1.9		1.9	2.1		1.9		1.6		1.6	1.8		1.6		GHz
1/Tc2	Common clock freq.	1.6		1.6	1.8		1.6		1.3		1.3	1.5		1.3		ps
Tsd	Data setup time	-50		-50			-50		-40		-40			-40		ps
Tss	SEL setup time	-50		-50			-50		-40		-40			-40		ps
Thd	Data hold time	250		250			250		275		275			275		ps
Ths	SEL hold time	150		150			150		165		165			165		ps
Tdod	Output disable delay	375	650	350	500	550	350	650	400	700	350	550	600	400	700	ps
Tdoe	Output enable delay	350	600	350	450	500	350	600	350	650	350	500	550	350	650	ps
Twc	Clear pulse width	500					500		550					550		ps
Tdc	Output clear delay	600	950	600	850	900	600	950	600	1050	600	975	1000	600	1050	ps
Tdhl	Clock to output H-L delay	600	950	600	850	900	600	950	600	1050	600	975	1000	600	1050	ps
Tdlh	Clock to output L-H delay	600	950	600	850	900	600	950	600	1050	600	975	1000	600	1050	ps
	Clock to output skew		50		30	50		50		50		30	50		50	ps
Tr	Output rise time		175		175			200		200		175			225	ps
Tf	Output fall time		150		125			150		175		125			175	ps

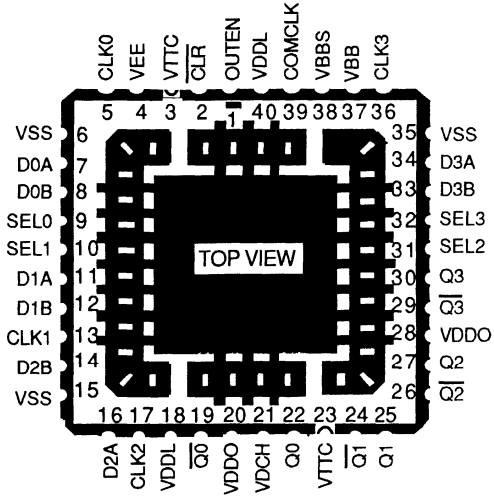
NOTES:

1. Test conditions (unless otherwise noted): VBB = -1.2V, VTT = -2.0V, VTTC = VTT, Rload = 50Ω to VTT, VDCH = VDDO, VIH = -0.7 V, VIL = -1.7 V, VOH ≥ -0.7 V, VOL ≤ -1.7 V. Input signal rise and fall times <150ps.
2. Output rise and fall times are measured at the 20% and 80% points of the transition from VOL max to VOH min.

SWITCHING WAVEFORMS



PIN FUNCTIONS - PACKAGE TYPES "L" AND "C"



NOTE: Pin 1 is marked for orientation.

Quad D Flip Flop with XOR Inputs
1.9 GHz Clock Rate
10G PicoLogic™ Family

DISTINCTIVE CAPABILITIES

- 850 ps typical clock to output delay
- Individual or common clock inputs
- Differential outputs with common output enable control
- Common asynchronous clear control
- ECL and PicoLogic™ compatible I/O
- Temperature and voltage compensated design
- ≤ 50 ps clock to output delay skew
- Ouput Wire-OR capability
- Available in C-Leaded or Leadless chip carriers or dice form

APPLICATIONS

- Cyclic Redundancy Check Code Generation
- Bit Extender for 10G061 Synchronous Counter
- Toggle (T) flip-flop with SEL as the toggle control
- Complementing Register for Subtraction
- Pseudo-random Word Generator
- Synchronous set-reset (S-R) flip-flop with $\overline{DA}$ as reset input and DB as the set input.

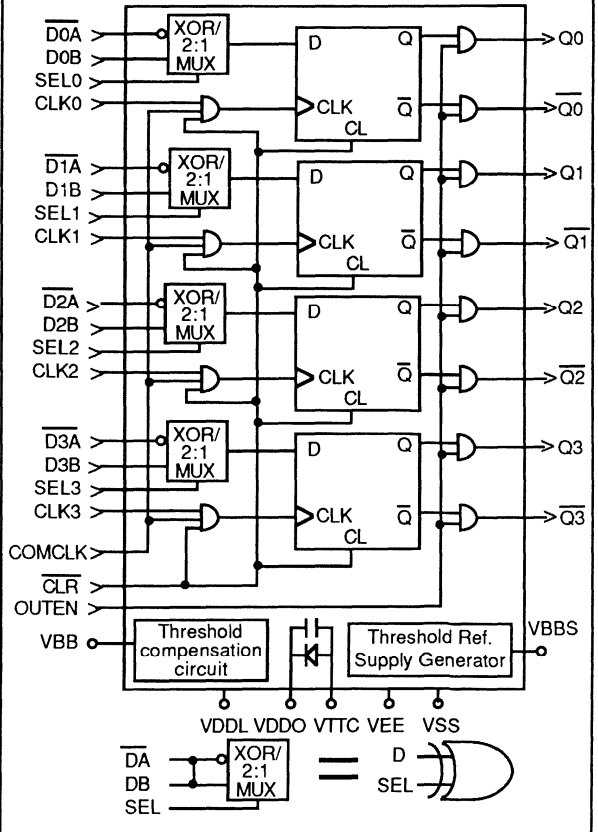
FUNCTIONAL DESCRIPTION

The 10G024 is a Gallium Arsenide quad D-type flip flop with XOR gate or 2:1 MUX data inputs ($\overline{D0A}$-$\overline{D3A}$, D0B-D3B). When the $\overline{DA}$ and DB inputs are connected together, data to each of the four stages is the XOR of this input and the SEL input, and is latched into the flip flop by the rising edge of either the individual clock inputs (CLK0-CLK3) or the common clock input (COMCLK). An active low common clear (CLR) input is provided for resetting each flip flop asynchronously to a low level. All device outputs can be disabled (brought low), without interfering with the current state of the flip flop, via the output enable (OUTEN) control. This permits wired-OR bus connection.

The 10G024 can be clocked at 2.1 GHz typically. Clock to output delay at room temp. is 850 ps and the skew in output delay time is tightly matched to 30 ps which results in a highly symmetric output eye pattern.

The 10G024 is a member of GigaBit's Picologic™ family of GaAs digital ICs and is fabricated using GigaBit's high volume GaAs MESFET process technology.

BLOCK DIAGRAM



10G024 ORDERING INFORMATION

PACKAGE TYPE	SPEED (Min. 0°C to 85°C)	
	1.9 GHz	1.6 GHz
C-Leaded CC Leadless CC Dice	10G024-2C 10G024-2L	10G024-3C 10G024-3L 10G024-3X

10G024 OPERATION (Truth Table with XOR Gate Inputs Configured)

Function	$\overline{CLR}$	OE	CLKn	COMCLK	$\overline{DnA}$ = DnB	SEL	Output Qn (t+1)
Clear *	L	H	X	X	X	X	L
Output Disabled	H	L	L or H	L or H	X	X	L
Output Enabled	H	H	L or H	L or H	X	X	Qn(t)
XOR	H	H	⊓	H	0	0	0
XOR	H	H	⊓	H	0	1	1
XOR	H	H	H	⊓	1	0	1
XOR	H	H	H	⊓	1	1	0
Clock Disabled	H	H	L	⊓	X	X	Qn(t)
Clock Disabled	H	H	⊓	L	X	X	Qn(t)

10G024 OPERATION (Truth Table with 2:1 MUX Inputs Configured)

Function	SELn	$\overline{CLR}$	OE	CLKn	COMCLK	$\overline{DnA}$	DnB	Qn (t+1)
Clear *	X	L	H	X	X	X	X	L
Output Disabled	X	H	L	L or H	L or H	X	X	L
Output Enabled	X	H	H	L or H	L or H	X	X	Qn(t)
Select A	H	H	H	⊓	H	$\overline{DnA(t)}$	X	$\overline{DnA(t)}$
Select B	L	H	H	⊓	H	X	DnB(t)	$\overline{DnB(t)}$
Select A	H	H	H	H	⊓	$\overline{DnA(t)}$	X	$\overline{DnA(t)}$
Select B	L	H	H	H	⊓	X	DnB(t)	DnB(t)
Clock Disabled	X	H	H	L	⊓	X	X	Qn(t)
Clock Disabled	X	H	H	⊓	L	X	X	Qn(t)

The operation of the 10G024 is described in the truth tables above. The device is configured for XOR gate inputs by connecting together the DA and DB inputs and using this as one XOR input, the other being the SEL input. With the inputs configured for 2:1 Muxing, when SEL is high, A data are selected. When SEL is low, B data are selected. All flip flop stages are reset to low by bringing CLR low at any time. All outputs can be turned off for bus connection, without altering the current state of the flip flops, by bringing OUTEN low.

Data are clocked into the flip flop assuming the appropriate setup and hold time requirements are met. At any time, the clock input can be disabled by setting the unused clock input(s) low. The current state of each flip flop is maintained in this case.

* When both clock signals are in the high state, application of $\overline{CLR}$ will cause data at the inputs to be clocked into the flip-flops at the rising edge of the $\overline{CLR}$ pulse. Hence, avoid reseting $\overline{CLR}$ (returning to the high state) when both CLKn and COMCLK are high.

PIN DESCRIPTIONS

$\overline{D0A}$ - $\overline{D3A}$	A data inputs
D0B - D3B	B data inputs
SEL0-SEL3	MUX select or XOR gate inputs
CLK0 - CLK3	Individual flip flop clock inputs
COMCLK	Common clock input to all four flip flops
$\overline{CLR}$	Active low asynchronous clear control
OUTEN	Active high output enable control
Q0 - Q3	True data outputs
$\overline{Q0}$ - $\overline{Q3}$	Complement data outputs
VDDO	Output driver ground pin (0V)
VDDL	Internal logic ground connection (0V)
VSS	-3.4 V power supply
VEE	-5.2 V power supply
VTTC	AC return lead for the package internal VDDO decoupling capacitor. Typically connect to VTT.
VDCH	Output driver high level clamp voltage. When driving other GaAs devices, VDCH is generally left unconnected. When driving ECL, VDCH may be used to limit VOH. Consult App. Note 4 for detail.
VBB	Reference input to the 10G024's input threshold compensation circuit. Connect to the VBB supplied from ECL when driving the 10G024 from ECL. Connect to the VBBS pin when the 10G024 is driven from PicoLogic™. This pin may not be left unconnected.
VBBS	PicoLogic™ threshold reference output voltage. Nominally equal to -1.3V with a 40Ω source impedance. Connect to VBB when driving from PicoLogic™. ΔVBBS/ΔTemp = 0.6mV/°C; ΔVBBS/ΔVSS = 0.2 mV/mV.

CRC ERROR DETECTION SCHEMES

DEFINITION:

Cyclical redundancy check (CRC) is an efficient method to detect errors in digital transmission systems. CRC codes are the remainder (R(x)) of the division between the data to be transmitted (M(x)) and a standard check polynomial P(x).

$$M(x) = Q(x) \cdot P(x) + R(x)$$

The code R(x) is appended to the serial data M(x). Therefore, the data transmitted becomes $T(x) = M(x) + R(x)$.

CRC error detection uses modulo - 2 arithmetic. Since modulo - 2 has no carries or borrows, addition and substraction yield the same result. Hence,

$$T(x) = M(x) + R(x) = M(x) - R(x) = Q(x) \cdot P(x)$$

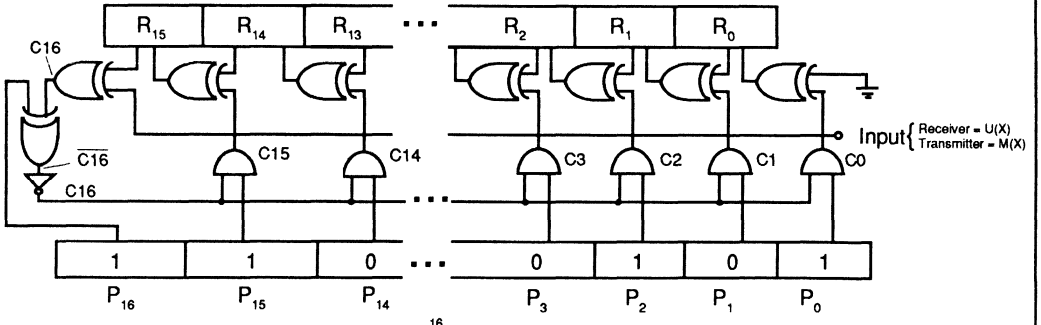
To check the validity of the data, the receiver simply divides the received data U(x) by the same standard polynomial P(x). If there are no errors, U(x) is equal to the transmitted polynomial T(x), and the division results in a remainder of zero.

$$\frac{U(x)}{P(x)} = \frac{T(x)}{P(x)} = \frac{Q(x) \cdot P(x)}{P(x)} = Q(x) + 0$$

CRC 16 CODE IMPLEMENTATION

a) Conceptual Diagram

Transmitter: $R(X) = \sum_{i=0}^{15} R_i X^i$ [Remainder of M(X)/P(X)]; Receiver: R(X)=0 if no errors [Remainder of U(X)/P(X)]

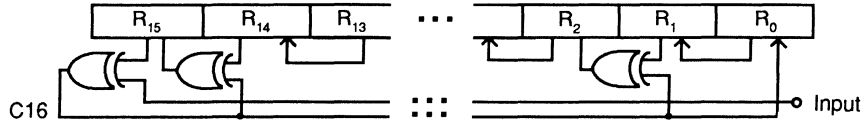


$$P(X) = \sum_{i=0}^{16} P_i X^i = X^{16} + X^{15} + X^2 + 1$$

b) Simplified Diagram [M(X)/P(X) or U(X)/P(X)]

$P_i=0 \rightarrow Ci=0 \rightarrow R_{i-1} \oplus Ci = R_{i-1} \oplus 0 = R_{i-1}$; $0 \le i \le 15$

$P_i=1 \rightarrow Ci=C16 = \overline{(R_{15} \oplus \text{Input}) \oplus 1} = \overline{\overline{R_{15} \oplus \text{Input}}} = R_{15} \oplus \text{Input}$; $P_{16} = 1$; $0 \le i \le 15$

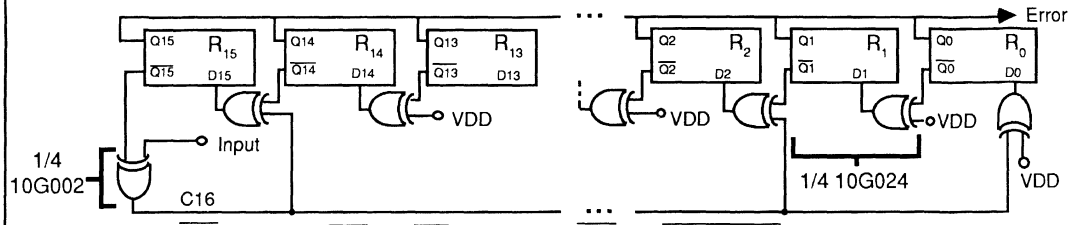


NOTE: CRC recommended references: C. Deierling, "Exclusive-OR inputs give you many uses for GaAs flip-flop." Electronic Design, (December 10, 1987), pg. 59; Krishna Rallapa, "CRC error detection schemes ensures data accuracy." EDN, (September 5, 1978), pg. 119.

CRC 16 IMPLEMENTATION USING FOUR 10G024's AND ONE 10G002

CRC 16 CHECKER:

In order to check if the remainder is 0 (no error), we suggest to wire-OR the Q outputs of all flip-flops. Therefore, only $\overline{Q}$ is available to perform the division.



$D15 = \overline{Q14} \oplus C16 = \overline{Q14} \oplus (\overline{Q15} \oplus Input) = \overline{Q14} \oplus (\overline{Q15 \oplus Input}) = Q14 \oplus (Q15 \oplus Input)$

NOTE: R_4 to R_{11} (two 10G024's) can be replaced by one 10G022

CRC 16 GENERATOR: Same circuit as above except:

1). A disable should be added to force C16 to VDD and allow the 10G024's to function as shift registers only, Q15 being the output.

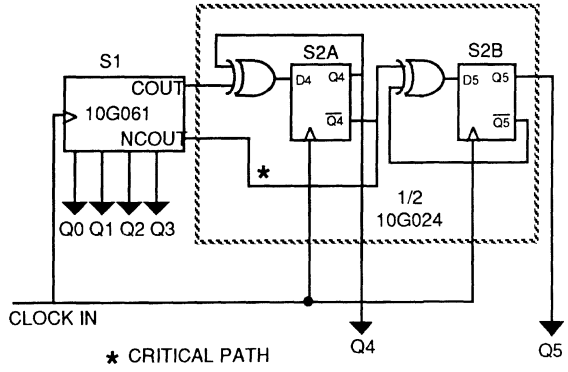
2). Q15 should be muxed with the input in order for the transmitted data to be alternatively the input [M(X)] or Q15 [remainder R(X) appended to M(X)].

TWO BIT SYNCHRONOUS EXTENSION OF THE 10G061 USING THE 10G024

TRUTH TABLE AT COUNT 1110 OF Q1

10G061 Count	Cout	Q4	D4	Q4•Cout	Q5	D5	
1110	0	0	0	0	0	0	
1111	1	0	1	0	0	0	
0000	0	1	1	0	0	0	16 Counts*
•	•	•	•	•	•	•	
•	•	•	•	•	•	•	
•	•	•	•	•	•	•	
1110	0	1	1	0	0	0	
1111	1	1	0	1	0	1	
0000	0	0	0	0	1	1	16 Counts*
•	•	•	•	•	•	•	
•	•	•	•	•	•	•	
•	•	•	•	•	•	•	
1110	0	0	0	0	1	1	
1111	1	0	1	0	1	1	
0000	0	1	1	0	1	1	16 Counts*
•	•	•	•	•	•	•	
•	•	•	•	•	•	•	
•	•	•	•	•	•	•	
1110	0	1	1	0	1	1	
1111	1	1	0	1	1	0	
0000	0	0	0	0	0	0	

* If N 10G061 are cascaded, then counts = 16•N



* CRITICAL PATH

$D5 = (\overline{Q4 + Cout}) \oplus \overline{Q5}$

$= (Q4 \cdot Cout) \oplus \overline{Q5}$

$= (Q4 \cdot Cout) \oplus Q5$

$D4 = Q4 \oplus Cout$

S1 is a 10G061 counter in free counting mode (please refer to the 10G061 datasheet, pg. 3, for more details). When the 10G061 reaches 15 (1111, i.e. terminal count), COUT pulses high for one clock period. This causes S2A to toggle since $D4=\overline{Q4}=Q4 \oplus 1$. This circuit could be expanded to multiple 10G061 counters with S1 being the most significant counter.

DC CHARACTERISTICS

Tc = 0°C to 85°C, VSS = -3.5 V TO -3.3 V, VEE = -5.5 TO -5.1 V, VDDL = VDDO = Gnd, unless otherwise indicated

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	TEST CONDITIONS
I in 1	Input Current; Data , SEL, CLKn	-500	200	500	µA	VIN = -1.0 V to -1.6 V
I in 2	Input Current; COMCLK, CLR, OUTEN	-1000	500	1000	µA	
ISS	Power Supply Current		260	340	mA	
IEE	Power Suppy Current		35	65	mA	
PD	Power Dissipation		1.0	1.5	W	

NOTE:

The remaining DC Characteristics are specified in the 10G PicoLogic™ Family Electrical Characteristics Table at the beginning of this section. This table notes parameter deviations to Family Characteristics and provides specific supplementary characteristics only.

AC CHARACTERISTICS (Notes 1, 2)

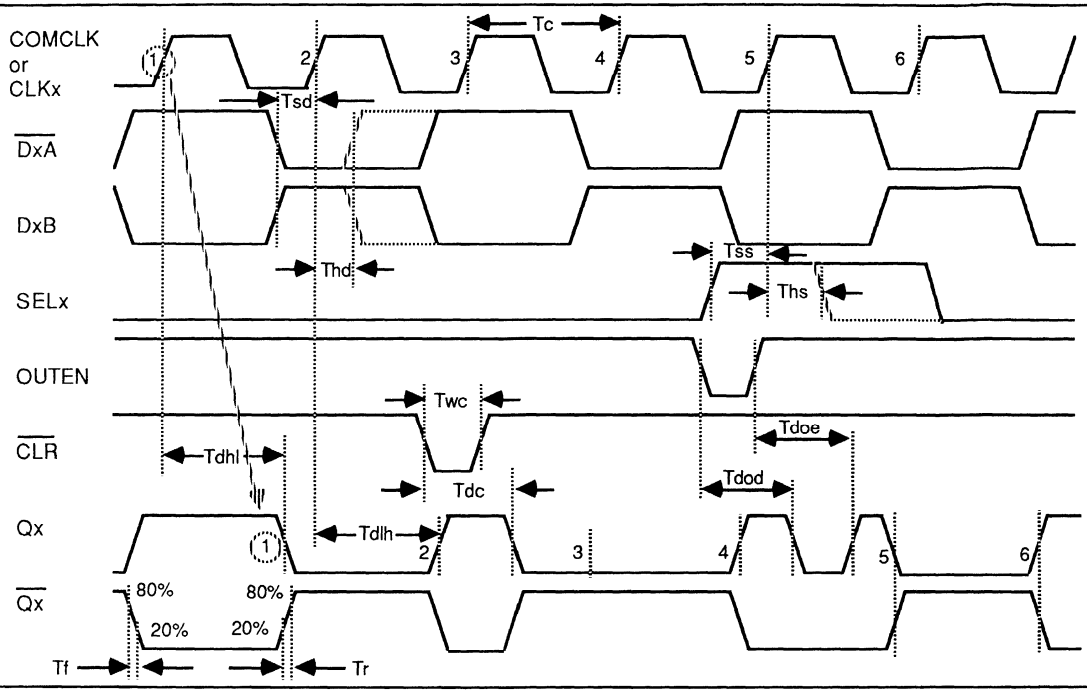
VSS= -3.5V to -3.3V, VEE= -5.5V to -5.1V, VDDL=VDDO=Gnd., unless otherwise indicated

		10G024-2							10G024-3							
SYMBOL	PARAMETER	Tc= 0° C		Tc= 25° C			Tc= 85° C		Tc= 0° C		Tc= 25° C			Tc= 85° C		UNITS
		MIN	MAX	MIN	TYP	MAX	MIN	MAX	MIN	MAX	MIN	TYP	MAX	MIN	MAX	
1/Tc1	Individual clock freq.	1.9		1.9	2.1		1.9		1.6		1.6	1.8		1.6		GHz
1/Tc2	Common clock freq.	1.6		1.6	1.8		1.6		1.3		1.3	1.5		1.3		ps
Tsd	Data setup time	-50		-50			-50		-40		-40			-40		ps
Tss	SEL setup time	-50		-50			-50		-40		-40			-40		ps
Thd	Data hold time	250		250			250		275		275			275		ps
Ths	SEL hold time	150		150			150		165		165			165		ps
Tdod	Output disable delay	375	650	350	500	550	350	650	400	700	350	550	600	400	700	ps
Tdoe	Output enable delay	350	600	350	450	500	350	600	350	650	350	500	550	350	650	ps
Twc	Clear pulse width	500					500		550					550		ps
Tdc	Output clear delay	600	950	600	850	900	600	950	600	1050	600	975	1000	600	1050	ps
Tdhl	Clock to output H-L delay	600	950	600	850	900	600	950	600	1050	600	975	1000	600	1050	ps
Tdlh	Clock to output L-H delay	600	950	600	850	900	600	950	600	1050	600	975	1000	600	1050	ps
	Clock to output skew		50		30	50		50		50		30	50		50	ps
Tr	Output rise time		175		175			200		200		175			225	ps
Tf	Output fall time		150		125			150		175		125			175	ps

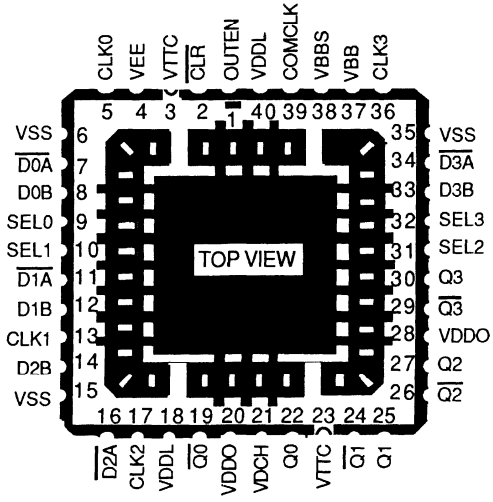
NOTES:

1. Test conditions (unless otherwise noted): VBB = -1.2V, VTT = -2.0V, VTTC = VTT, Rload = 50Ω to VTT, VDCH = VDDO, VIH = -0.7 V, VIL = -1.7 V, VOH ≥ -0.7 V, VOL ≤ -1.7 V. Input signal rise and fall times <150ps.
2. Output rise and fall times are measured at the 20% and 80% points of the transition from VOL max to VOH min.

SWITCHING WAVEFORMS



PIN FUNCTIONS - PACKAGE TYPES "L" AND "C"



NOTE: Pin 1 is marked for orientation.

GigaBit Logic

8:1 Time Division Multiplexer
Parallel to Serial Converter • 1.45 Gbit/s NRZ Data Rate
10G PicoLogic™ Family

DISTINCTIVE CAPABILITIES

- Complete single chip time multiplexer system
- DC to 1.45 GHz operation (Typ.)
- 8:1 and 4:1 operating modes
- Cascadable to 16:1, 32:1 or 64:1 with on-chip synchronization circuitry
- Parallel or ripple data input modes
- Programmable 8-phase clock ÷ 8 output
- Strobed latch design results in precise output data eye
- Clock ÷ 4 output for 32:1 cascading
- ECL and PicoLogic compatible I/O
- Complementary high speed serial data outputs with reclocking capability
- Available in C-Leaded or leadless chip carrier or in dice form

APPLICATIONS

- High data rate fiber optic and microwave receivers/ transmitters and drop-and-insert systems
- High capacity local area networks
- High resolution graphic display terminals
- Digital RF memory
- Board-to-board or computer-to-peripheral data communications
- High data rate word or test vector generation

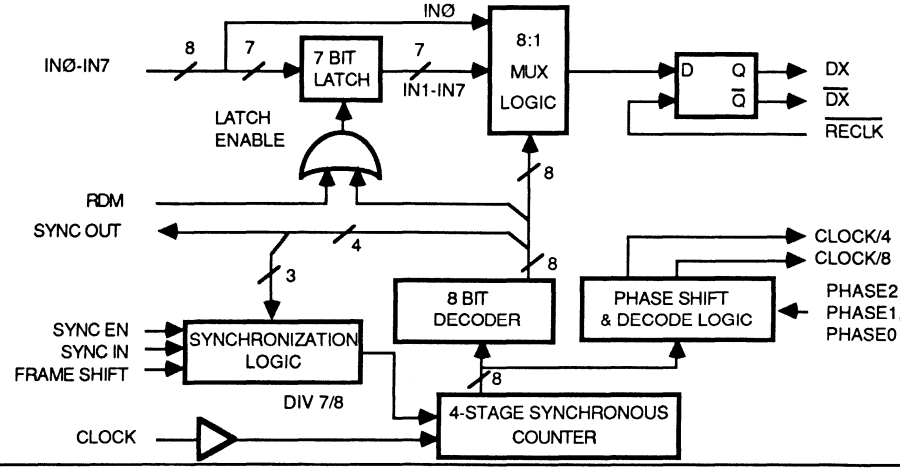
FUNCTIONAL DESCRIPTION

The 10G040A is a complete, single chip digital time division 8:1 multiplexer capable of parallel to serial conversion at rates extending from DC to 1.45 Gbit/s NRZ. The 10G040A features synchronization circuitry which greatly simplifies the timing control when devices are cascaded to wider word size. Data can be accepted either as 8-bit parallel input words or bit-serial using the ripple data mode control, which also permits the 10G040A to be operated as a 4:1 MUX. Both CLOCK÷8 and CLOCK÷4 outputs are provided. The phase of the Clock÷8 output can be programmed in 1-bit period increments to simplify the timing control of logic providing data to the 10G040A. The 10G040A is fabricated using GigaBit's high volume GaAs MESFET process technology.

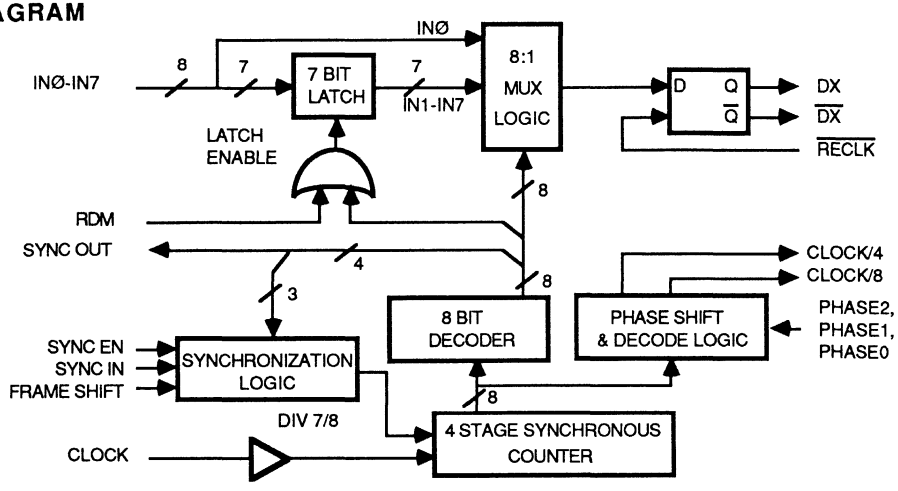
10G040A ORDERING INFORMATION

PACKAGE TYPE	SPEED (Min. 0°C to 85°C)		
	1.25 GHz	1.0 GHz	750 MHz
Leadless CC	10G040A-L	10G040A-3L	10G040A-4L
C- Leaded CC	10G040A-C	10G040A-3C	10G040A-4C
Dice			10G040A-4X

10G040A BLOCK DIAGRAM



10G040A BLOCK DIAGRAM



PIN DESCRIPTIONS

Signal Pins

IN0-IN7
Multiplexer data input signal lines.

DX, $\overline{DX}$
Complementary, high speed serialized bit stream output pins.

SYNC OUT
SYNC OUT provides a sync pulse of one CLOCK period duration every time data from IN1 appears at the outputs. Sync Out is used when cascading multiple devices for greater than 8 channel capacity.

SYNC IN
This input pin is used to receive the SYNC OUT pulse from another 10G040A when multiple multiplexers are cascaded. Tie low (to VSS) when not used.

FRAME SHIFT
Each time a low-to-high transition is applied to FRAME SHIFT, the 10G040A's internal counter will divide by seven instead of eight , swallowing one clock period and shifting frame timing by one bit. Tie FRAME SHIFT low (to VSS) when not used.

CLOCK
High speed external clock input pin. The clock signal on this pin drives the 10G040A's internal sequencing counter. The NRZ data rate at the DX and $\overline{DX}$ outputs is equal to the CLOCK input frequency.

CLOCK/4
This output pin provides a clock output equal to one quarter of the master CLOCK frequency. CLOCK/4 is used when cascading 10G040A's to achieve higher order multiplexing ratios.

CLOCK/8
CLOCK/8 is an output clock equal to one eighth of the master CLOCK frequency. CLOCK/8 is normally used to clock interfacing logic through which data to IN0-IN7 is gated. The phase of CLOCK/8, with respect to the time of input data sampling, is digitally adjustable via the PHASE0,1,2 control pins.

$\overline{RECLK}$
This input pin controls the function of the 10G040A's output data reclocking latch. Tie $\overline{RECLK}$ low (to VSS) to allow data to pass through the latch without being retimed. When a delayed version of the clock is applied to the $\overline{RECLK}$ pin, data will be re-timed through the output latch, reducing output jitter approximately 50 ps.

Control Pins

RDM
The RDM (Ripple Data Mode) input pin selects whether the 10G040A samples input data on pins IN0-IN7 in ripple or parallel mode. RDM = 0 (tied low to VSS) selects parallel mode; RDM = 1 (tied high to VDDL) selects ripple mode.

PHASEØ, PHASE1, PHASE2
These three input pins are used to select one of 8 phases of the CLOCK/8 output. See the notes in the AC Char. table for programming information.

SYNC ENABLE
This input pin enables or disables the SYNC IN signal input. The SYNC IN pin is enabled when SYNC ENABLE is tied high (to VDDL); SYNC IN is disabled when SYNC ENABLE is tied low (to VSS). When not used, SYNC ENABLE must be tied low. This pin can also be used to shift frame timing in a manner similar to the FRAME SHIFT input (see text).

VBB
Reference input to the 10G040A's input threshold compensation circuit. Connect to the VBB supplied from ECL when driving the 10G040A from ECL. Connect to the VBBS pin when the 10G040A is driven from PicoLogic. This pin may not be left open.

VBBS
PicoLogic threshold reference output voltage. Nominally equal to -1.3V with a 40Ω source impedance. Connect to VBB when driving from PicoLogic.
$\Delta VBBS/\Delta Temp = 0.6mV/°C$;
$\Delta VBBS/\Delta VSS = 0.2$ mV/mV.

Power Supply Pins

VDDO, VDDL
These pins are the ground (0V) connections for the output driver and internal logic circuitry, respectively.

VSS = -3.4V power supply.

VEE = -5.2V, low current input stage pull-down power supply.

VTTC
AC return lead for the package internal VDDO decoupling capacitor. Connect to VTT.

Functional Description, cont.

INPUT MODES (PINS IN0-IN7)
The 10G040A has two basic input modes: "parallel mode", where inputs IN1- IN7 are sampled simultaneously and stored in the input latch, and "ripple mode", where each input bit is sequentially sampled 1 clock period apart and are all transparent (not latched) through to the output during their respective time slice. In either mode, IN0 is not latched. The input mode is selected by the control pin RDM. Parallel mode is selected by tying this pin low and ripple mode is selected by tying RDM high. In normal 8:1 operation, parallel mode is easiest to use since the CLOCK/8 output can be used to control the timing of data into the Mux. Through adjustment of the CLOCK/8 phase using the control pins PHASE0, PHASE1 and PHASE2, it is possible to compensate for interconnect delays and guarantee maximum timing margin between the input sampling time of the MUX and the data valid period of the input data. Some systems make use of multiphase clocking which results in data pulses that are staggered in time. In these applications, ripple mode may be most appropriate since the sampling times for each of the input pins are staggered in a manner that matches the timing skews of the eight individual inputs. Ripple mode is also used to configure the 10G040A to operate as a 4:1 multiplexer which is capable of maximum data rate operation.

2. OUTPUT MODES (DX, $\overline{DX}$, and $\overline{RECLK}$ PINS)
The 10G040A high speed serial output appears on pins DX and $\overline{DX}$. When the $\overline{RECLK}$ pin is tied low to Vss, output data flows through the reclocking latch and is not re-timed. Data eye pattern asymmetry in this case is <200ps. When a delayed version of the clock is applied to $\overline{RECLK}$, output data is re-timed by the latch, reducing output jitter approximately 50ps. In this case, the CLOCK line should be daisy-chained to the $\overline{RECLK}$ pin and terminated only at the $\overline{RECLK}$ input.

3. SUBMULTIPLE CLOCK OUTPUTS AND CONTROL PINS (CLOCK/8, CLOCK/4 AND PINS PHASE0,1,2)
The 10G040A provides CLOCK/4 and CLOCK/8 outputs to provide synchronous clocking to interfacing input circuitry. In addition, they can be used in conjunction with a PLL to provide a stable, synthesized master CLOCK from a stable ECL clock.

The phase of the CLOCK/8 output is digitally programmable to any one of eight phases, each differing by one high speed CLOCK period in time. When the CLOCK/8 output is used to control interfacing data input logic, the user generally will program the CLOCK/8 phase necessary to acheive proper timing between the Mux and interfacing circuitry. This is accomplished by providing a 3-bit static code to input pins PHASE0, PHASE1 and PHASE2 and changing this code as necessary to assure that input data is stable during the sampling period.

4. FRAME GENERATION AND TIMING

The 10G040A features a ÷7/÷8 counter controlled by on-chip synchronization logic with FRAME SHIFT, SYNC EN and SYNC IN control inputs. Any of these three inputs can put the dual modulus counter into the ÷7 mode causing the device to effectively "swallow" one counter state or clock pulse. The swallowed clock pulse always corresponds to bit time 0 (counter state 0) meaning that the data bit ordinarily sampled on the IN0 line will be swallowed, or ignored. This has the effect of shifting frame timing one bit position. Since the control logic for bit time 0 is also the control logic which generates the signal causing data on inputs IN1 thru IN7 to be held in the input latch, this signal is also swallowed. The result is that, in parallel mode only, output data is not updated and the last stored byte of data is replayed at the output. The data output will not be updated until the counter is returned to the ÷8 mode. Therefore, if it is necessary to determine from the output whether or not frame timing (frame synchronization) is correct, then the control input causing the ÷7 counter mode must be alternately inhibited. In ripple data input mode, when a ÷7 operation occurs, due to any of the three controlling inputs, bit time 0 is still swallowed but IN1-IN7 are updated at the output because the 7-bit input latch is always transparent in this mode.

There are timing differences between the manner in which FRAME SHIFT, SYNC EN and SYNC IN cause the counter to switch to the ÷7 mode. SYNC IN should only be used when multiple 10G040As are cascaded to form wider width multiplexers. In this case, the SYNC OUT pulse from cascaded device A (called the master) is driven into the SYNC IN input of cascaded device B (termed the slave). The amount of overlap between the received SYNC OUT pulse from the master and the internal SYNC OUT pulse of the slave is compared by the slave and used to determine whether or not a ÷7 counter mode should be initiated in the slave. In this manner, multiple cascaded devices are automatically synchronized (see section on Cascading and SYNC OUT/SYNC IN Timing for examples).

The FRAME SHIFT and SYNC EN controls are also used to shift frame timing or position. In particular, SYNC EN is quite useful in alternating ÷7 and ÷8 modes as a means of controlling the frame synchronization process. When the FRAME SHIFT pin is pulsed with a rising edge anytime between Clock1 to slightly after Clock6 during the time in which Byte A data is input, Bit0 (Clock0) of the SECOND following output data byte will be swallowed or lost. In ripple mode, this means that Bit0 of output Byte C is lost. In parallel mode, Bit0 of a repeated Byte B is swallowed. Byte B is repeated during the time at which Byte C would normally appear at the output because the input latch does not capture Byte C (recall that the latch command is also swallowed). The Switching Waveforms Summary drawing makes this operation clear.

Compared with the FRAME SHIFT command, SYNC EN operates identically except that it is an active high level signal and its effect occurs on the IMMEDIATELY following data byte. When SYNC EN is brought high during the time interval when data Byte A is input, following the example above, data bytes will appear at the output in the order AACD and not ABBD as is the case for the FRAME SHIFT command example. In both cases, the first bit of the repeated byte (Bit0) is swallowed. Note that Byte A , not Byte B is repeated in response to SYNC EN, illustrating its more immediate affect on the output. SYNC EN, when used to shift frame timing, must meet minimum specified high time requirements and must go high anytime following Clock0 up to Clock6 in order for Bit0 of the IMMEDIATELY following byte to be swallowed.

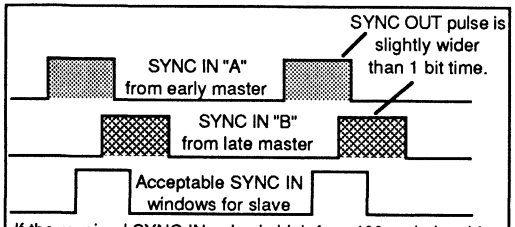
SYNC OUT / SYNC IN TIMING; SYNCHRONIZATION OF CASCADED 10G040As

The 10G040A is designed to be cascaded to provide the ability to form wider word size multiplexers and to achieve higher data rates than is possible with a single device. Cascaded devices are automatically synchronized via use of the SYNC OUT signal and SYNC IN input as explained in the previous section. Devices are configured for auto sync as follows:

1. Tie the SYNC EN pins of all slaves high (to VDDL) and that of the master low (to VSS);
2. Connect the SYNC OUT signal, delayed 600ps, of the master to the SYNC IN pins of all slaves.

Each slave now has its internal phase detection circuitry enabled to compare the amount of overlap between the received SYNC OUT pulse from the master and its

own internally generated SYNC OUT pulse. There is, however a possible difficulty with this type of operation since the slave may potentially be sync'ed to either of two possible states of the master. This is due to the fact that the slave senses the level of the SYNC IN from the master during its internal sync time, and only requires this to be in the high state for 400ps. This results in the potential for redundant sync'ing as described below.



If the received SYNC IN pulse is high for >400ps during this window the master and slave will be in sync and the slave will count to 8; otherwise the slave will attempt to sync itself by dividing by 7 and swallowing a count.

In the sketch above, BOTH SYNC-IN "A" and "B" timing meet the requirement for the master and slave to be in sync; hence the slave will not swallow a count and will not resynchronize. To avoid this possible redundant sync state, the following scheme will assure that only the SYNC-IN "A" state will exist. The master device should be given a FRAME SHIFT after the parts have been turned on long enough to stabilize. If the slave was initially sync'ed to SYNC-IN A (early master) the FRAME SHIFT pulse will cause SYNC IN A to occur earlier in time and move in front of the acceptable window. As a result, the Slave will swallow a pulse and the SYNC-IN A condition will be re-established. If the slave is initially sync'ed to SYNC-IN B, the application of a FRAME SHIFT to the master will advance the master's SYNC OUT pulse to the SYNC-IN A condition, which is the desired in-sync state. It is also necessary to assure that the CLOCK and SYNC-OUT/SYNC-IN path delays match sufficiently such that >400 ps of overlap occur. Marginal overlap could result in initial syncing per the SYNC-IN A timing which might slip due to temperature, noise, etc. causing a slave to swallow a count and arrive at the SYNC-IN B condition.

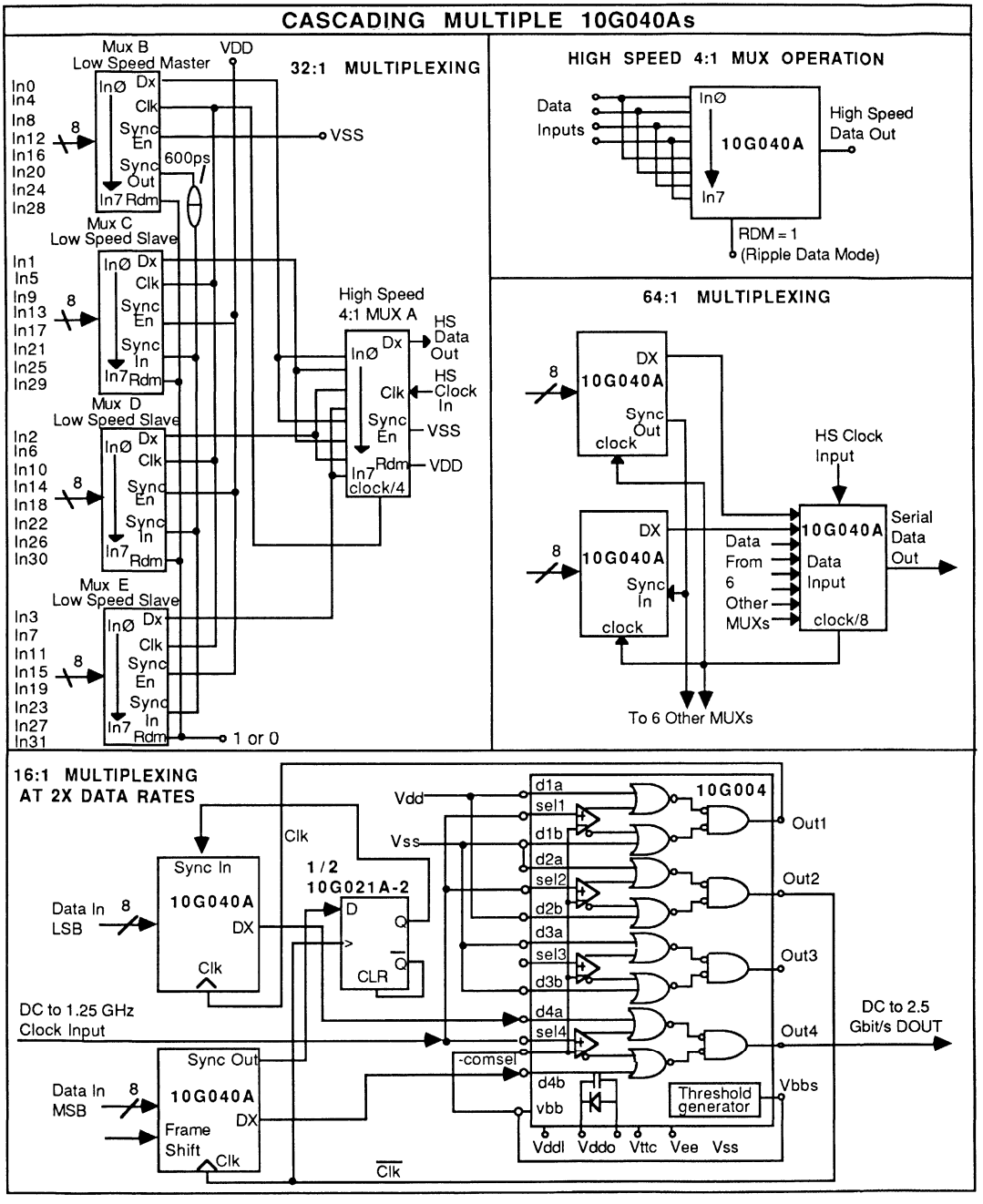
Since the clock delay internal to the slave exceeds the SYNC-IN delay by approximately 600 ps, it is necessary to delay the SYNC-OUT pulse from the master by approximately 600 ps before passing it to the SYNC-IN of the slave device. This is approximately the delay of most common combinatorial PicoLogic parts except for the NOR gates which have only a single stage. Hence, it is possible to achieve this delay by buffering the SYNC OUT pulse with devices such as the 10G002, 004, or 010. The10G010 fanout buffer might be used where several slave devices are required. When it is required to double the final output speed of the 10G040A, two devices are driven with clocks 180° out of phase to form a single stage, high speed16:1 mux.

The circuit drawings which follow show how the 10G040A is configured to create 4:1, 16:1 (double speed), 32:1 and 64:1 multiplexers. In order to assure the proper timing relationship between SYNC OUT and SYNC IN when cascading, the following circuit layout rules should be followed (the 32:1 drawing is used to illustrate these rules):

1. The CLOCK/4 (or CLOCK/8) output from the high speed MUX (MUX A) must be fed first to the CLOCK input of the low speed master (MUX B) and then distributed in daisy-chain fashion to the three low speed slaves (MUX's C, D, E). Similarly, SYNC OUT from the master must be delayed 600ps and then connected in a daisy chain to the slaves.

2. The length of the interconnect lines between the clock connection at the master and the clock connection to any slave must equal the length of interconnect between the master SYNC OUT connection and the SYNC IN connection at any slave.

3. The sum of:
   (a) the interconnect length between the clock output from the high speed MUX (MUX A) and the clock input to any low speed MUX, plus
   (b) the interconnect length between the data output of the same low speed MUX and the data input to high speed MUX A ---
must be the same for all cascaded (low speed) MUXs.


CASCADING MULTIPLE 10G040As
Mux B
Low Speed Master
VDD
32:1 MULTIPLEXING
In0
In4
In8
In12
In16
In20
In24
In28
8
InØ
Dx
Clk
Sync En
Sync Out
In7
Rdm
VSS
600ps
Mux C
Low Speed Slave
In1
In5
In9
In13
In17
In21
In25
In29
Sync In
High Speed 4:1 MUX A
HS Data Out
HS Clock In
VSS
VDD
clock/4
Mux D
Low Speed Slave
In2
In6
In10
In14
In18
In22
In26
In30
Mux E
Low Speed Slave
In3
In7
In11
In15
In19
In23
In27
In31
1 or 0
HIGH SPEED 4:1 MUX OPERATION
Data Inputs
High Speed Data Out
10G040A
RDM = 1
(Ripple Data Mode)
64:1 MULTIPLEXING
DX
Sync Out
clock
HS Clock Input
Sync In
Data From 6 Other MUXs
Data Input
clock/8
Serial Data Out
To 6 Other MUXs
16:1 MULTIPLEXING
AT 2X DATA RATES
Clk
Vdd
Vss
1/2
10G021A-2
D
Q
CLR
Data In LSB
DC to 1.25 GHz Clock Input
Data In MSB
Frame Shift
d1a
sel1
d1b
d2a
sel2
d2b
d3a
sel3
d3b
d4a
sel4
d4b
vbb
-comsel
10G004
Out1
Out2
Out3
Out4
DC to 2.5 Gbit/s DOUT
Vbbs
Threshold generator
Vddl
Vddo
Vttc
Vee
Vss

DC CHARACTERISTICS (Notes 1,2)

Tc = 0°C to 85°C, VSS = -3.5V to -3.3V, VEE = -5.5V to -5.1V, VDDL=VDDO = Gnd, unless otherwise indicated.

Symbol	Parameter	Min	Typ	Max	Units	Test Conditions	
VIH1	Input voltage high (IN0-IN7)	- 1.0		VDDL	V		
VIL1	Input voltage low (IN0-IN7)	VSS		- 1.6	V		
VIH2	Input voltage high (RECLK)	-0.6		VDDL	V		
VIL2	Input voltage low (RECLK)	VSS		-1.8	V		
VIH3	Input voltage high (all others)	-0.8		VDDL	V		
VIL3	Input voltage low (all others)	VSS		-1.8	V		
ISS	VSS power supply current		395	500	mA		
IEE	VEE power supply current		40	60	mA		
PD	Power dissipation		1.5	2.0	W		

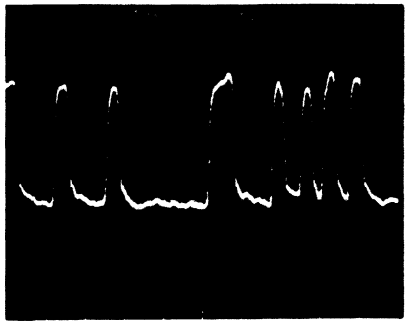
NOTES:

1. The remaining DC Characteristics are specified in the 10G PicoLogic Family Electrical Characteristics section. This table notes parameter deviations to Family Characteristics and provides device specific supplementary characteristics only.
2. Upon power up, the 10G040A's internal counter should be initialized to a known state through application of a pulse to the Frame Shift input.

10G040A TYPICAL OUTPUT WAVEFORMS

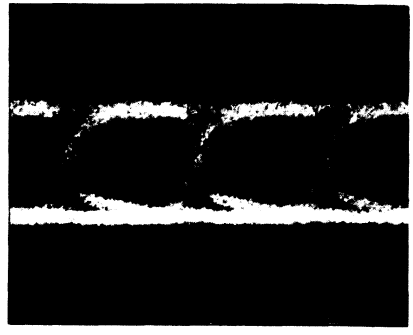
1.5 Gbit/s DATA RATE

DX Output (2^{15}-1 Pseudorandom Pattern)
Corrected Vert.=500 mV/div.



OUTPUT DATA EYE PATTERN

1.5 Gbit/s DATA RATE
DX Output (2^{15}-1 Pseudorandom Pattern)
Corrected Vert.= 500 mV/div.



AC CHARACTERISTICS (NOTES 1,2,3,4)

10G040A VSS = -3.5V to -3.3V, VEE = -5.5V to -5.1V, VDDL=VDDO = Gnd., unless otherwise indicated.

SYMBOL	PARAMETER	Tc = 0°C		Tc = +25°C			Tc = +85°C		UNITS
		MIN	MAX	MIN	TYP	MAX	MIN	MAX	
1/T	Clock Frequency	1.25		1.25	1.45		1.35		GHz
tsoh	CLK1 to sync out high	1250	1600		1350		1250	1600	ps
tsol	CLK2 to sync out low	1300	1700		1450		1300	1700	ps
tc4h	CLK2 to CLK/4 high	1300	1700		1450		1300	1650	ps
tc4l	CLK0 to CLK/4 low	1400	1900		1650		1400	1750	ps
tc8h	CLK0 to CLK/8 high	1500	1950		1550		1500	1950	ps
tc8l	CLK4 to CLK/8 low	1250	1600		1350		1250	1650	ps
tdo	CLK to data output	1700	2100	1700	1900	2100	1700	2100	ps
thse	SYNC EN high time	500		500			500		ps
tsd	Data to CLK0 setup time	-500		-600	-800		-500		ps
thd	CLK1 to data hold time	1400		1350	1000		1400		ps
trcko	$\overline{\text{RECLK}}$ to data output	500	1000	500	700	1000	500	1000	ps
tr,f	Output rise and fall times		200		150	200		200	ps

10G040A-3

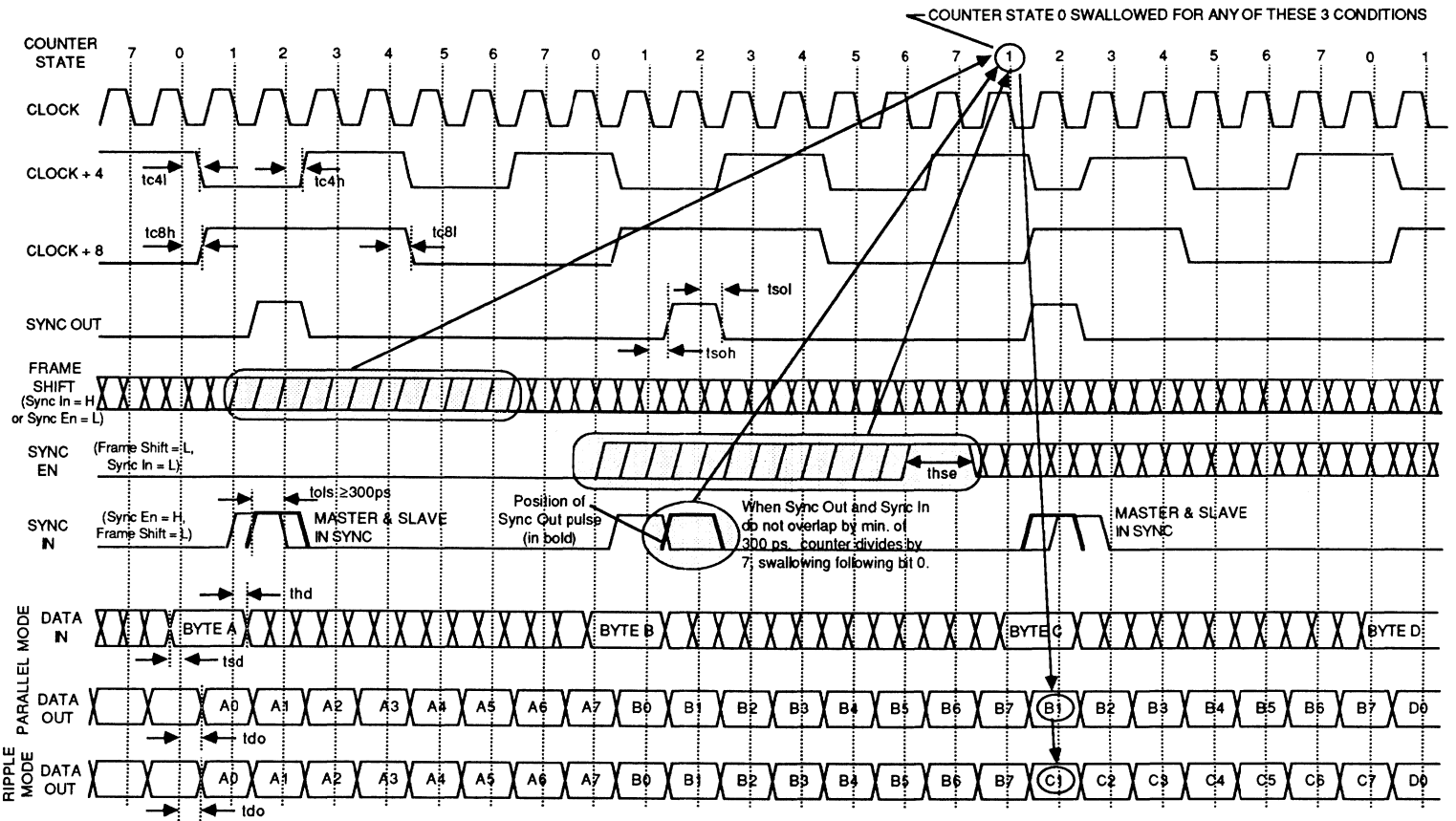
SYMBOL	PARAMETER	Tc = 0°C		Tc = +25°C			Tc = +85°C		UNITS
		MIN	MAX	MIN	TYP	MAX	MIN	MAX	
1/T	Clock Frequency	1.0		1.15	1.25		1.15		GHz
tsoh	CLK1 to sync out high	1450	1750		1450		1400	1650	ps
tsol	CLK2 to sync out low	1550	1850		1550		1450	1750	ps
tc4h	CLK2 to CLK/4 high	1450	1800		1450		1400	1650	ps
tc4l	CLK0 to CLK/4 low	1650	2000		1700		1600	1900	ps
tc8h	CLK0 to CLK/8 high	1750	2100		1750		1650	1950	ps
tc8l	CLK4 to CLK/8 low	1450	1800		1550		1400	1650	ps
tdo	CLK to data output	1900	2300	1900	2100	2300	1900	2300	ps
thse	SYNC EN high time	500		500			500		ps
tsd	Data to CLK0 setup time	-500		-600	-900		-500		ps
thd	CLK1 to data hold time	1500		1400	1000		1500		ps
trcko	$\overline{\text{RECLK}}$ to data output	500	1000	500	800	1000	500	1000	ps
tr,f	Output rise and fall times		200		150	200		200	ps

10G040A-4

SYMBOL	PARAMETER	Tc = 0°C		Tc = +25°C			Tc = +85°C		UNITS
		MIN	MAX	MIN	TYP	MAX	MIN	MAX	
1/T	Clock Frequency	.75		.75	1.00		.75		GHz
tsoh	CLK1 to sync out high	1400	1900		1500		1350	1800	ps
tsol	CLK2 to sync out low	1500	2000		1600		1400	1900	ps
tc4h	CLK2 to CLK/4 high	1400	1950		1500		1350	1800	ps
tc4l	CLK0 to CLK/4 low	1600	2150		1750		1550	2050	ps
tc8h	CLK0 to CLK/8 high	1700	2250		1800		1600	2100	ps
tc8l	CLK4 to CLK/8 low	1400	1950		1600		1350	1800	ps
tdo	CLK to data output	1850	2450	1900	2150	2300	1850	2450	ps
thse	SYNC EN high time	550		500			550		ps
tsd	Data to CLK0 setup time	-450		-600	-850		-450		ps
thd	CLK1 to data hold time	1550		1400	1050		1550		ps
trcko	$\overline{\text{RECLK}}$ to data output	450	1150	500	850	1000	450	1150	ps
tr,f	Output rise and fall times		250		200	250		250	ps

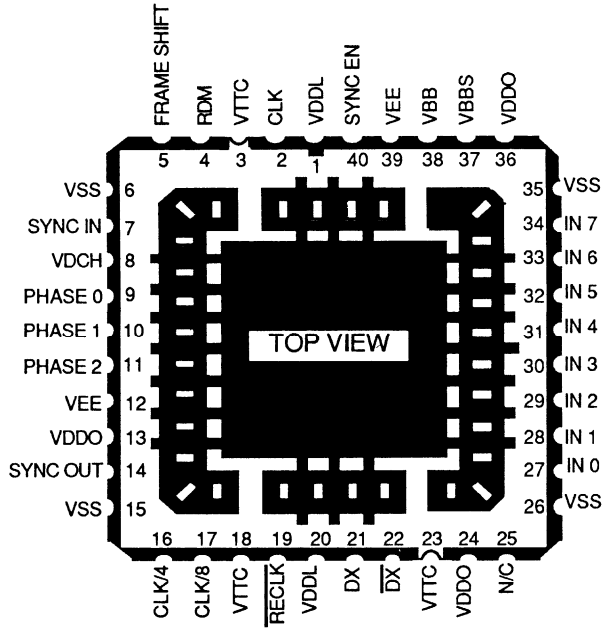
1. Test conditions (unless otherwise noted): Vbb = -1.3V, Vtt = -2.0V, Vttc = Vtt, Rload = 50Ω to Vtt, Vdch = Vddo, Data Inputs: Vih = -0.7V, Vil = -1.7V, Voh≥ -0.7V, Vol ≤ -1.7V. Input signal rise and fall times ≤ 200ps.
2. Output rise and fall times are measured at the 20% and 80% points of the transition from Vol max to Voh min.
3. This applies when phase 0 = Phase 1 = Phase 2 = low.
4. Clock input = 1.5Vp-p, -1.3V DC offset.

10G040A SWITCHING WAVEFORMS AND TIMING CHARACTERISTICS SUMMARY



NOTES:
1. CLOCK ÷ 8 IS SHOWN WITH PHASE 0 = PHASE 1 = PHASE 2 = LOW.
2. The falling edge of Clock0 causes the input data latch to become transparent, whereas the Clock1 falling edge causes the latch to hold data. Since data input IN0 bypasses the latch, data setup time is referenced to Clock0 and data hold time is referenced to Clock1.
3. Clock1 initiates the generation of the SYNC OUT pulse. Therefore, SYNC OUT delays are referenced to Clock1.

PIN FUNCTIONS - PACKAGE TYPES "C" AND "L"



NOTES: Pin 1 is marked for orientation. N/C = No Connection.

GBL GigaBit Logic

10G041A

1:8 Time Division Demultiplexer Serial to Parallel Converter • 1.45 Gbit/s NRZ Data Rate

10G PicoLogic™ Family

DISTINCTIVE CAPABILITIES

- Complete single chip demultiplexer system
- DC to 1.45 Gbit/s operation (Typ.)
- 1:8 and 1:4 operating modes
- On-chip frame synchronization circuitry
- Parallel or ripple data output modes
- Programmable input timing simplifies system interface
- 10G PicoLogic™ and ECL compatible
- Cascadable to 1:16, 1:32, 1:64, and beyond
- Fully compatible with companion 10G040A 8:1 multiplexer and 16G040 clock recovery circuit
- High speed differential input stage
- Available in "C" leaded or leadless chip carriers or in die form

APPLICATIONS

- High data rate fiber optic and microwave receivers/ transmitters and drop-and-insert systems
- High capacity local area networks
- Digital RF memory
- Board-to-board or computer-to-peripheral data communications
- High speed test equipment response vector deserialization

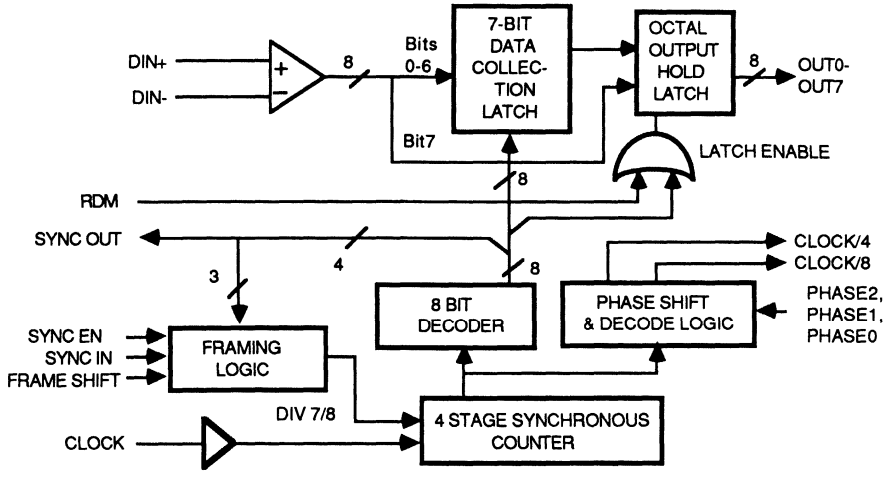
FUNCTIONAL DESCRIPTION

Together with its companion 10G040A 8:1 multiplexer, the 10G041A Time Division Demultiplexer extends fiber optic digital data transmission speeds to 1.45 Gbps NRZ. The device is capable of serial-to-parallel data deserialization at rates extending from DC to 1.45 Gbps, with maximum power dissipation of 1.9 W. The 10G041A is a complete, single-chip demultiplexing subsystem containing on-chip frame synchronization circuitry which simplifies fiber optic receiver design while minimizing high speed parts count. It features a CLOCK/8 output with digitally programmable phase which provides easy synchronization between the 10G041A and logic connected to its 8 outputs. It can be operated in a 1:4 mode and can be cascaded to higher order DEMUX ratios of 1:16, 1:32 or 1:64.

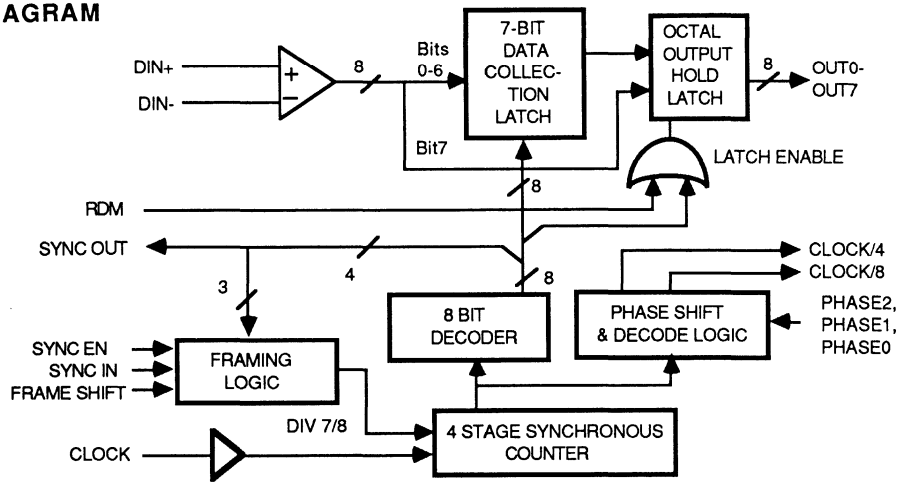
10G041A ORDERING INFORMATION

PACKAGE TYPE	SPEED (Min. 25°C)		
	1.25 GHz	1.0 GHz	750 MHz
Leadless CC	10G041A-L	10G041A-3L	10G041A-4L
C- Leaded CC	10G041A-C	10G041A-3C	10G041A-4C
Dice			10G041A-4X

10G041A BLOCK DIAGRAM



10G041A BLOCK DIAGRAM



PIN DESCRIPTIONS

Signal Pins

OUT0 through OUT7
Demultiplexer data output pins.

DIN+, DIN-
Complementary, high speed differential input pins. These inputs should either be driven from differential signals or the unused input must be tied to reference threshold from driving device (nominally -1.3 volts)

SYNC OUT
This output pin is used when cascading multiple 10G041As for higher order DEMUX ratios. In combination with the SYNC IN input pin, SYNC OUT is used to acheive automatic synchronization among a group of cascaded demultiplexers. SYNC OUT provides a positive sync pulse of one CLOCK period duration during the time that data on output pin OUT1 is valid.

SYNC IN
This input pin is used to receive the SYNC OUT pulse from another 10G041A when multiple demultiplexers are cascaded. Tie low (to VSS) when not used.

FRAME SHIFT
Each time a low-to-high transition is applied to FRAME SHIFT, the 10G041A's internal counter will divide by seven instead of eight for one clock period, effectively shifting frame timing by one bit. Tie low (to VSS) when not used.

CLOCK
This is the high speed external clock input pin. The clock signal on this pin drives the 10G041A's internal sequencing counter. The input sampling rate on the DIN+ and DIN- inputs is equal to the CLOCK frequency.

CLOCK/4
This output pin provides a clock output equal to one quarter of the master CLOCK frequency. CLOCK/4 is used when cascading 10G041A's to achieve higher order demultiplexing ratios.

CLOCK/8
CLOCK/8 is an output clock equal to one eighth of the master CLOCK frequency. CLOCK/8 will normally be used to clock external logic accepting data from the OUT0 to OUT7 output pins. The phase of CLOCK/8, with respect to output data timing, is digitally adjustable via the PHASE0,1,2 control pins.

Control Pins

RDM
The RDM (Ripple Data Mode) input pin selects whether the 10G041A provides output data on pins OUT0 through OUT7 in parallel or ripple data format. RDM = 0 (tied low to VSS) selects parallel mode; RDM = 1 (tied high to VDDL) selects ripple mode.

PHASE0, PHASE1, PHASE2
These three input pins are used to select one of 8 phases of the CLOCK/8 output.

SYNC EN
This input pin enables or disables the SYNC IN signal input. The SYNC IN pin is enabled when SYNC EN is tied high (to VDDL); SYNC IN is disabled when SYNC EN is tied low (to VSS). When not used, SYNC EN must be tied low or SYNC IN must be tied high. SYNC EN can also be used to shift frame timing in a manner similar to the FRAME SHIFT input (see text).

VBB
Reference input to the 10G041A's input threshold compensation circuit. Connect to the VBB supplied from ECL when driving the 10G041A from ECL. Connect to the VBBS pin when the 10G041A is driven from PicoLogic. This pin may not be left unconnected.

VBBS
PicoLogic threshold reference output voltage. Nominally equal to -1.3V with a 40Ω source impedance. Connect to VBB when driving from PicoLogic.
$\Delta VBBS/\Delta Temp = 0.6mV/°C$;
$\Delta VBBS/\Delta VSS = 0.2$ mV/mV.

Power Supply Pins

VDDO, VDDL
These pins are the ground (0V) connections for the output driver and internal logic circuitry, respectively.

VSS
-3.4V power supply.

VEE
-5.2V power supply.

VTTC
AC return lead for the package internal VDDO decoupling capacitor. Typically connect to VTT.

Functional Description, cont.

1.DATA INPUT (PINS DIN+, DIN-)
High speed serial data is sampled by the 10G041A on the differential input pins DIN+ and DIN-. The data is demultiplexed and output on the 8 output pins OUT0 through OUT7. Input data is sampled under control of an on-chip counter, which is incremented on each high-to-low transition of the CLOCK input. The rate at which data is output is therefore equal to one eighth of the CLOCK frequency. Data is always sampled and output in sequential order OUT0,OUT1, OUT2...OUT7, OUT0...
The DIN+ and DIN- inputs may be differentially driven, or if either is connected to -1.3V (or VBBS), the other may be driven from an ECL or PicoLogic compatible source.

2. DATA OUTPUT (PINS RDM and OUT0-OUT7)
Two output data modes, called parallel and ripple data modes, are supported by the 10G041A. Input pin RDM (Ripple Data Mode) selects the output mode. When RDM is tied high (to VDDL), ripple mode is enabled. For RDM tied low (to VSS), parallel mode is selected. In normal 1:8 operation, parallel mode is easiest to use since the outputs arrive simultaneously and remain stable for nearly seven bit times. The CLOCK/8 output of the DEMUX can be used to clock the interfacing ECL logic. Through adjustment of the CLOCK/8 phase using the control pins PHASE0, PHASE1 and PHASE2, it is possible to compensate for external logic and interconnect delays and guarantee maximum timing margin between the output data valid time of the DEMUX and the ECL input sample period. In some applications, ripple mode may be more appropriate such as when it is necessary to retain all demultiplexed bits except the bit being swallowed during a +7 "swallow" operation. Ripple mode is also required to achieve maximum data rate operation of a 1:4 demultiplexer.

In parallel mode, the 10G041A's counter and decode logic causes bits 0-6 to be loaded in successive positions of the seven bit data collection latch. When the counter reaches a count of seven, (the eighth count) indicating a full byte of data has been assembled in the data collection latch, the output hold latch is made transparent, and data from the data collection latch flows through the output hold latch to OUT0-OUT6. Simultaneously, the input data for bit 7 is being sampled by the demultiplexer and is passed around the data collection latch, and through the transparent hold latch, to OUT7 directly.

When the next high-to-low CLOCK edge is received, the output hold latch is made non-transparent, holding the data on all eight OUT pins constant until a new byte is assembled in the data collection latch. Because the output hold latch is updated during counter state 7 (bit time 7), output data should not be sampled during this time.

In ripple mode, the output hold latch is always in the transparent state. As bits received on the DIN pins are written into the data collection latch, the OUT pins are immediately updated. As a result, in ripple mode the outputs are staggered in time.

3. SUBMULTIPLE CLOCK OUTPUTS AND CONTROL PINS (CLOCK/8, CLOCK/4 AND PINS PHASE0,1,2)
The 10G041A provides CLOCK/4 and CLOCK/8 outputs to provide synchronous clocking to interfacing ECL output circuitry. In addition, they can be used in conjunction with a PLL to provide a stable, synthesized master CLOCK from an ECL clock. The output phase of the CLOCK/8 output is digitally programmable to any one of eight phases, each differing by one high speed CLOCK period in time. When the CLOCK/8 output is used to control interfacing data output logic, the user generally will program the CLOCK/8 phase necessary to achieve synchronization between the Demux and interfacing logic. This is accomplished by providing a 3-bit static code to input pins PHASE0, PHASE1 and PHASE2 and changing this code as necessary to achieve sync.

4. FRAME SYNCHRONIZATION AND TIMING
The 10G041A features a ÷7/÷8 counter controlled by on-chip synchronization logic with FRAME SHIFT, SYNC EN and SYNC IN control inputs. Any of these three inputs can put the dual modulus counter into the ÷7 mode causing the device to effectively "swallow" one counter state or clock pulse. The swallowed clock pulse always corresponds to bit time 7 (counter state 7) meaning that the data bit ordinarily sampled and output during bit time 7 will be swallowed, or ignored. Also, in parallel mode, bit time 7 is the time during which the command to update the output holding latch with the contents (bits 0-6) of the data collection latch, is generated. Therefore, not only will bit 7 be swallowed when the counter is in the ÷7 mode, but bits 0-6 will also be lost since the hold latch update command is also swallowed. The result is that, in parallel mode only, a complete byte of input data is swallowed (output data is not updated) and the last byte of data stored in the holding latch is replayed at the output. The data output will not be updated until the counter is returned to the ÷8 mode. Therefore, in parallel mode, if it is necessary to determine from the output whether or not frame timing (frame synchronization) is correct, then the control input causing the ÷7 counter mode must be alternately inhibited. In ripple data mode, when a ÷7 operation occurs, due to any of the three controlling inputs, bit time 7 is still swallowed but input bits 0-6 are updated at the output because the output holding latch is always transparent in this mode. There are timing differences between the manner in which FRAME SHIFT, SYNC EN and SYNC IN cause the counter to switch to the ÷7 mode. SYNC IN should be used when multiple 10G041As are cascaded to increase the width. In this case, the SYNC OUT pulse from device A (called the master) is driven into the SYNC IN input of cascaded device B (termed the slave). The timing between the received SYNC OUT pulse from the master and the internal SYNC OUT pulse of the slave is compared by the slave and used to determine whether or not a ÷7 counter mode should be initiated in the slave. In this manner, multiple cascaded devices are automatically synchronized (see section on Cascading and SYNC OUT/SYNC IN Timing for examples).

The FRAME SHIFT and SYNC EN controls are also used to shift frame timing or position. In particular, SYNC EN is quite useful in alternating ÷7 and ÷8 modes as a means of controlling the frame synchronization process. When the FRAME SHIFT pin is pulsed with a rising edge anytime between Clock0 to slightly after Clock 5 during the time in which Byte A data is input, Bit7 (Clock7) of the SECOND following output data byte will be swallowed or lost. In ripple mode, this means that Bit7 of output Byte C is lost. In parallel mode, Bit7 of a repeated Byte B is swallowed. Byte B is repeated during the time at which Byte C would normally appear at the output because the output latch does not capture Byte C (recall that the holding latch update command is also swallowed). Refer to the Switching Waveforms Summary drawing which makes this operation clear.

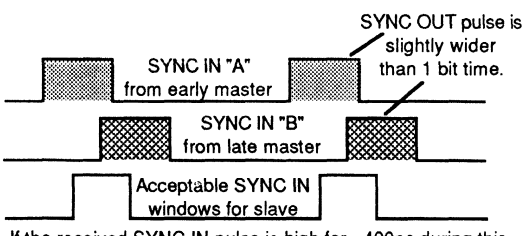
Compared with the FRAME SHIFT command, SYNC EN operates identically except that it is an active high level signal and its effect occurs on the IMMEDIATELY following data byte. When SYNC EN is brought high during the time interval when data Byte A is input, following the example above, data bytes will appear at the output in the order AACD and not ABBD as is the case for the FRAME SHIFT command example. In both cases, the last bit of the repeated byte (Bit7) is swallowed. Note that Byte A , not Byte B is repeated in response to SYNC EN, illustrating its more immediate affect on the output. SYNC EN, when used to shift frame timing, must meet minimum specified high time requirements and must go high anytime following Clock7 up to Clock5 in order for Bit7 of the IMMEDIATELY following byte to be swallowed.

5. SYNC OUT / SYNC IN TIMING; SYNCHRONIZATION OF CASCADED 10G041As

The 10G041A is designed to be cascaded to provide the ability to form wider word size demultiplexers and to achieve higher data rates than is possible with a single device. Cascaded devices are automatically synchronized via use of the SYNC OUT signal and SYNC IN input as explained in the previous section. Devices are configured for auto sync as follows:

1. Tie the SYNC EN pins of all slaves high (to VDDL) and that of the master low (to VSS);
2. Connect the SYNC OUT signal, delayed 600ps, of the master to the SYNC IN pins of all slaves.

Each slave now has its internal phase detection circuitry enabled to compare the amount of overlap between the received SYNC OUT pulse from the master and its own internally generated SYNC OUT pulse. There is, however a possible difficulty with this type of operation since the slave may potentially be sync'ed to either of two possible states of the master. This is due to the fact that the slave senses the level of the SYNC IN from the master during its internal sync time, and only requires this to be in the high state for 400ps. This results in the potential for redundant sync'ing as described below.



If the received SYNC IN pulse is high for >400ps during this window the master and slave will be in sync and the slave will count to 8; otherwise the slave will attempt to sync itself by dividing by 7 and swallowing a count.

In the sketch above, BOTH SYNC-IN "A" and "B" timing meet the requirement for the master and slave to be in sync; hence the slave will not swallow a count and will not resynchronize. To avoid this possible redundant sync state, the following scheme will assure that only the SYNC-IN "A" state will exist. The master device should be given a FRAME SHIFT after the parts have been turned on long enough to stabilize. If the slave was initially sync'ed to SYNC-IN A (early master) the FRAME SHIFT pulse will cause SYNC IN A to occur earlier in time and move in front of the acceptable window. As a result, the Slave will swallow a pulse and the SYNC-IN A condition will be re-established. If the slave is initially sync'ed to SYNC-IN B, the application of a FRAME SHIFT to the master will advance the master's SYNC OUT pulse to the SYNC-IN A condition, which is the desired in-sync state. It is also necessary to assure that the CLOCK and SYNC-OUT/SYNC-IN path delays match sufficiently such that >400 ps of overlap occur. Marginal overlap could result in initial syncing per the SYNC-IN A timing which might slip due to temperature, noise, etc. causing a slave to swallow a count and arrive at the SYNC-IN B condition.

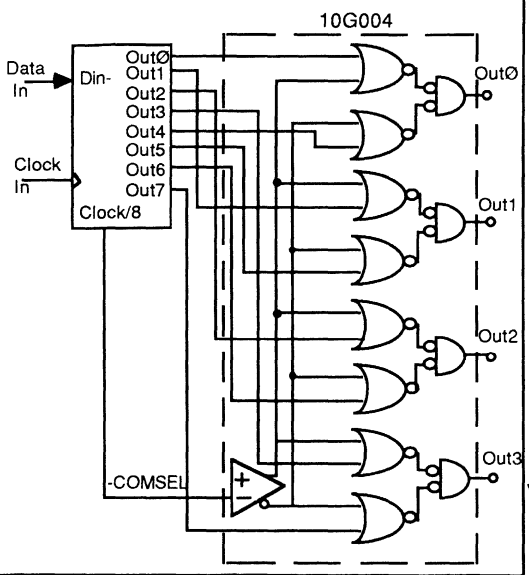
Since the clock delay internal to the slave exceeds the SYNC-IN delay by approximately 600 ps, it is necessary to delay the SYNC-OUT pulse from the master by approximately 600 ps before passing it to the SYNC-IN of the slave device. This is approximately the delay of most common combinatorial PicoLogic parts except for the NOR gates which have only a single stage. Hence, it is possible to achieve this delay by buffering the SYNC OUT pulse with devices such as the 10G002, 004, or 010. The10G010 fanout buffer might be used where several slave devices are required. When it is required to double the input speed of the 10G041A, two devices are driven with clocks 180° out of phase to form a single stage, high speed 1:16 demux.

The circuit drawings which follow show how the 10G041A is configured to create 1:4, 1:16 (double speed), and 1:64 demultiplexers. In order to assure the proper timing relationship between SYNC OUT and SYNC IN when cascading, the following circuit layout rules should be followed with the double speed 1:16 demultiplexer used for illustration:

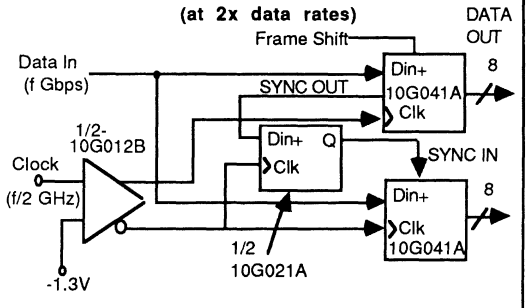
1. The incoming clock is converted to a bi-phase clock by the 10G012B, with the in-phase clock feeding the master and the out of phase clock feeding the slave. The inputs of the two multiplexers will therefore load their respective data collection latches on opposite phases of the clock permitting data to change during each half period of the clock.
2. SYNC OUT from the master must be delayed 600ps plus one half clock period before being sent to the SYNC IN input of the slave. The 10G021A is used to achieve this. Since the 10G021A clocks on the negative edge of the clock it is clocked from the non-inverted clock. For a fixed freq. of operation the flipflop could be eliminated and replaced with a delay line of a half period plus 600 ps.
3. The data input delays should be equalized for the two paths, otherwise additional clock delays and SYNC delays must be matched to the data delays.
4. Either CLK/8 output can be used as the handshake signal to the interfacing logic family since the output resister is stable during more than 6 of the possible 8 bit times. However it must be recognized that at a 2GBit/s data rate, all 16 outputs will be updated every 8ns.

CASCADING MULTIPLE 10G041A's (Note 2)

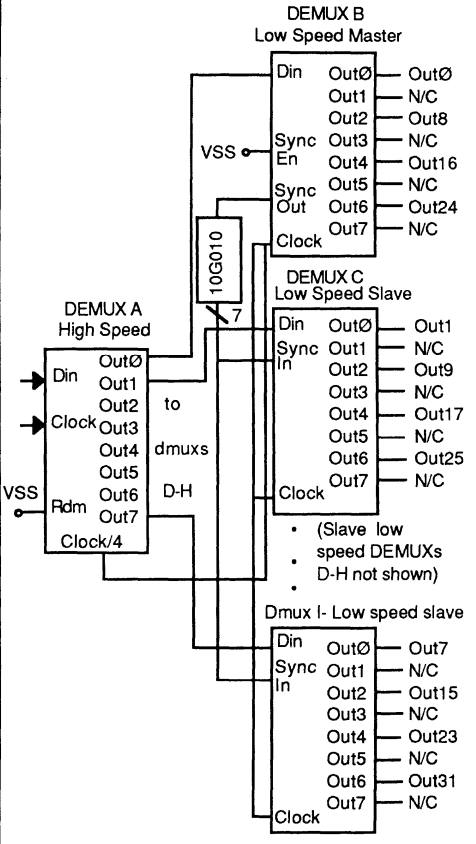
1:4 DEMULTIPLEXING



1:16 DEMULTIPLEXING (at 2x data rates)



1:32/1:64 DEMULTIPLEXING (Note 1)



NOTES

1. This block diagram shows the connections for 1:32 demultiplexing. Connections for 1:64 demultiplexing are identical, except that CLOCK/8 instead of CLOCK/4 is used and all 64 low speed outputs carry data.
2. In order to ensure the proper timing relationship between SYNC OUT and SYNC IN when cascading, the following circuit layout rules should be followed:

(a). The CLOCK/4 (or CLOCK/8) signal from the high speed DEMUX (DEMUX A above) must be fed first to the CLOCK input of the master (DEMUX B) and then daisy-chained from the master to the low speed slaves. Similarly, SYNC OUT from the master must be connected in a daisy chain to the slaves.

(b). The interconnect distance between the master's CLOCK connection and any slaves's CLOCK connection must equal the interconnect distance beteween the master's SYNC OUT connection and the SYNC IN connection to the same slave.

(c). The interconnect distance between each OUT pin of the high speed DEMUX (A) and the DIN pin of each low speed DEMUX must equal the interconnect length of the corresponding connection between DEMUX A's CLOCK output and the low speed DEMUX's CLOCK input.

DC CHARACTERISTICS

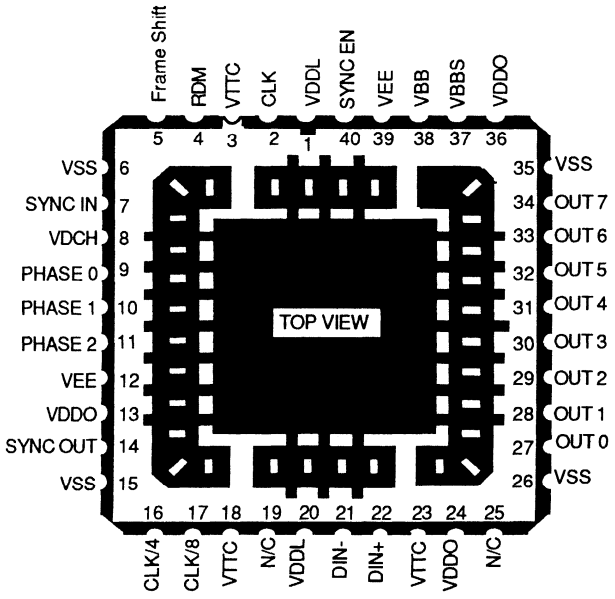
Tc = 25°C, VSS = -3.5V to -3.3V, VEE = -5.5V to -5.1V, VDDL=VDDO =Gnd, unless otherwise indicated.

Symbol	Parameter	Min	Typ	Max	Units	Test Conditions	Notes
ISS	VSS power supply current		300	450	mA		
IEE	VEE power supply current		40	60	mA		
PD	Power dissipation		1.2	1.9	W		

NOTE:

The remaining DC Characteristics are specified in the 10G PicoLogic Family Electrical Characteristics section. This table notes parameter deviations to Family Characteristics and provides device specific supplementary characteristics only.

PIN FUNCTIONS - 40 PIN PACKAGE TYPES "C" AND "L"



NOTES: Pin 1 is marked for orientation. N/C = No Connection.

AC CHARACTERISTICS (NOTES 1,2,3,4)

10G041A Tc = 25°C, Vss = -3.4V, Vee = -5.2V, Vddl =Vddo = Gnd., unless otherwise indicated.

SYMBOL	PARAMETER	Tc = 0°C		Tc = +25°C			Tc = +85°C		UNITS
		MIN	MAX	MIN	TYP	MAX	MIN	MAX	
1/T	Clock Frequency			1.25	1.45				GHz
tsoh	CLK0 to sync out high				1350				ps
tsol	CLK1 to sync out low				1450				ps
tc4h	CLK1 to CLK/4 high				1450				ps
tc4l	CLK7 to CLK/4 low				1650				ps
tc8h	CLK7 to CLK/8 high				1550				ps
tc8l	CLK3 to CLK/8 low				1350				ps
tdop	CLK7 to parallel data output			1700	1900	2100			ps
tdor	CLKn to ripple data output			1700	1900	2100			ps
thse	SYNC EN high time			500					ps
tsd	Data to CLK0 setup time				-800				ps
thd	CLK0 to data hold time				1000				ps
tr,f	Output rise and fall times				150	200			ps

10G041A-3

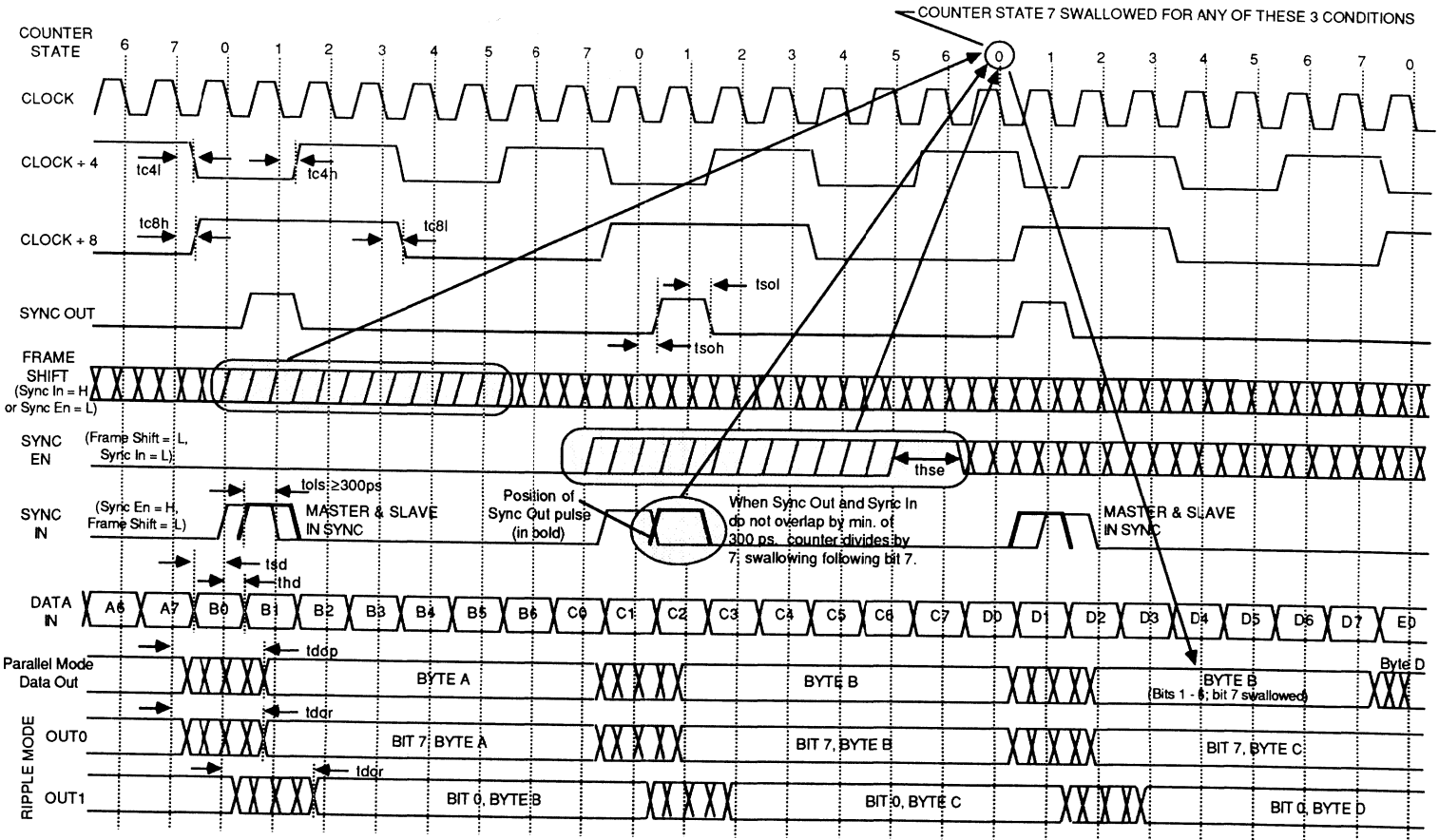
SYMBOL	PARAMETER	Tc = 0°C		Tc = +25°C			Tc = +85°C		UNITS
		MIN	MAX	MIN	TYP	MAX	MIN	MAX	
1/T	Clock Frequency			1.0	1.25				GHz
tsoh	CLK0 to sync out high				1450				ps
tsol	CLK1 to sync out low				1550				ps
tc4h	CLK1 to CLK/4 high				1450				ps
tc4l	CLK7 to CLK/4 low				1700				ps
tc8h	CLK7 to CLK/8 high				1750				ps
tc8l	CLK3 to CLK/8 low				1550				ps
tdop	CLK7 to parallel data output			1900	2100	2300			ps
tdor	CLKn to ripple data output			1900	2100	2300			ps
thse	SYNC EN high time			500					ps
tsd	Data to CLK0 setup time				-900				ps
thd	CLK0 to data hold time				1000				ps
tr,f	Output rise and fall times				150	200			ps

10G041A-4

SYMBOL	PARAMETER	Tc = 0°C		Tc = +25°C			Tc = +85°C		UNITS
		MIN	MAX	MIN	TYP	MAX	MIN	MAX	
1/T	Clock Frequency			.75	1.00				GHz
tsoh	CLK0 to sync out high				1500				ps
tsol	CLK1 to sync out low				1600				ps
tc4h	CLK1 to CLK/4 high				1500				ps
tc4l	CLK7 to CLK/4 low				1750				ps
tc8h	CLK7 to CLK/8 high				1800				ps
tc8l	CLK3 to CLK/8 low				1600				ps
tdop	CLK7 to parallel data output			1900	2150	2300			ps
tdor	CLKn to ripple data output			1900	2150	2300			ps
thse	SYNC EN high time			500					ps
tsd	Data to CLK0 setup time				-850				ps
thd	CLK0 to data hold time				1050				ps
tr,f	Output rise and fall times				200	250			ps

1. Test conditions (unless otherwise noted): Vbb = -1.3V, Vtt = -2.0V, Vttc = Vtt, Rload = 50Ω to Vtt, Vdch = Vddo, Vih = -0.5V, Vil = -1.9V, Voh≥ -0.7V, Vol ≤ -1.7V. Input signal rise and fall times ≤ 200ps.
2. Output rise and fall times are measured at the 20% and 80% points of the transition from Vol max to Voh min.
3. This applies when phase 0 = Phase 1 = Phase 2 = low.
4. Clock input = 1.5Vp-p, -1.3V DC offset.

10G041A SWITCHING WAVEFORMS AND TIMING CHARACTERISTICS SUMMARY



NOTES:
1. CLOCK ÷ 8 IS SHOWN WITH PHASE 0 = PHASE 1 = PHASE 2 = LOW.
2. The falling edge of Clock7 causes the output hold latch to become transparent; the Clock0 falling edge causes the output hold latch to hold data.
3. Clock0 initiates the generation of the SYNC OUT pulse. Therefore, SYNC OUT delays are referenced to Clock0.

3 to 8-Line or Dual 2 to 4-Line Decoder/Demux Boolean Function Generator • 650 ps Delay

10G PicoLogic™ Family

DISTINCTIVE CAPABILITIES

- Dual independent 2- to 4-line decoders
- Single 3- to 8-line decoder operation
- Dual 1:4 or single 1:8 demultiplexing capability
- Expandable to 1 of 24 with no external comps.
- Boolean function generation capability
- Active low mutually exclusive outputs
- Up to 1.6 GHz input freq. supported
- ECL and PicoLogic family compatible I/O
- Wired-OR output capability
- Temperature and voltage compensated design using VBB threshold reference input
- Available in leadless or C-leaded chip carriers or in unpackaged die form
- Packages contain internal decoupling capacitors for optimum high frequency performance
- 0°C to 85°C operating temperature range

APPLICATIONS

- High speed memory decoding
- Data transmission systems
- Demultiplexers
- Function generation

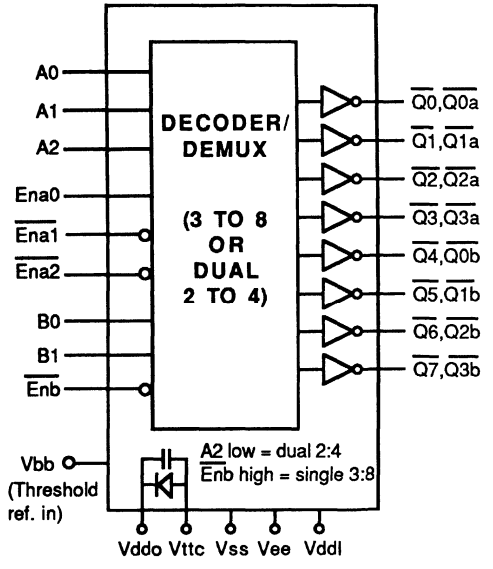
FUNCTIONAL DESCRIPTION

The 10G044 is an ECL and PicoLogic family compatible ultra-fast GaAs digital integrated circuit that is designed to perform the work of five separate devices. The 10G044 can be operated as a : 1) dual 2-to-4 line decoder; 2) single 3-to-8 line decoder; 3) dual 1:4 addressable demultiplexer; 4) single1:8 addressable demultiplexer; 5) Boolean function generator. When A2 is low, the 10G044 functions as a dual 2- to 4-line decoder or dual 1:4 Demux; when $\overline{Enb}$ is held high, the device operates as a single 3- to 8-line decoder or single 1:8 Demux. For compatibility with any ECL or GaAs logic family, the 10G044 incorporates the PicoLogic standard input threshold compensation circuit driven by the VBB input.

Typical address to output propagation delay is 500 ps. Typical output delays from the Enable inputs are 750 ps (Ena0) and 650 ps ($\overline{Enx}$). The 10G044 can support an input frequency of 1.6 GHz while dissipating less than 1.4W at room temperature. Output rise and fall times are typically 150 ps.

The 10G044 is a member of GigaBit Logic's 10G PicoLogic family of gallium arsenide integrated circuits and is fabricated using GigaBit's high volume, GaAs MESFET process technology.

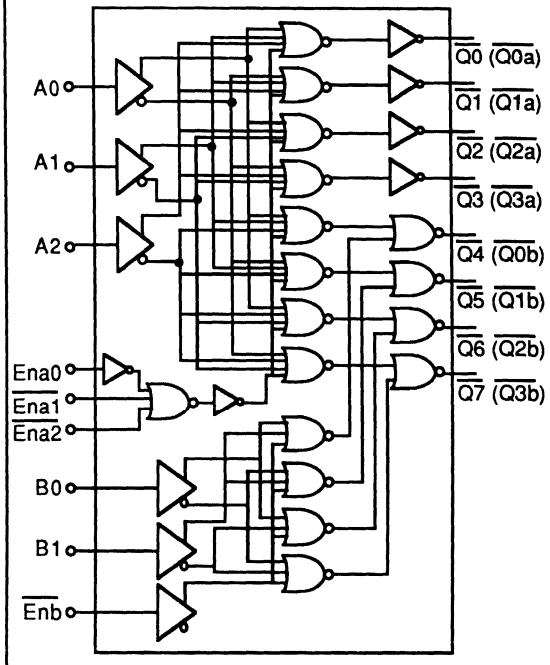
BLOCK DIAGRAM



10G044 ORDERING INFORMATION

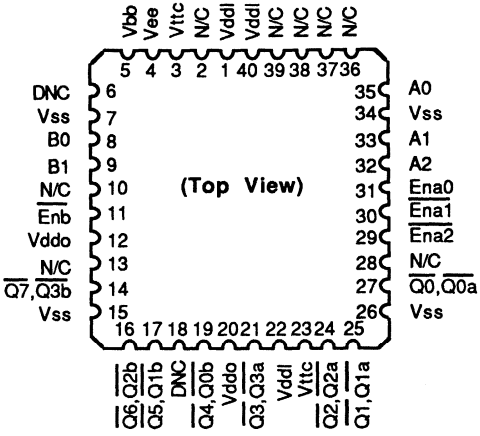
PACKAGE TYPE	DELAY (25°C max, An - Qn)
	650 ps
Leadless CC	10G044-2L
C-Leaded CC	10G044-2C
Dice	10G044-2X

10G044 LOGIC DIAGRAM



PACKAGE PIN FUNCTION DIAGRAM

PACKAGE TYPES "L" AND "C"



NOTES: Pin 1 is marked for orientation. N/C = No Connection. DNC = Do Not Connect.

DUAL 2-TO-4 LINE DECODING & DUAL 1:4 DEMULTIPLEXING*

A Side

Ena0	$\overline{Ena1}$	$\overline{Ena2}$	A1	A0	$\overline{Q0a}$	$\overline{Q1a}$	$\overline{Q2a}$	$\overline{Q3a}$
L	X	X	X	X	H	H	H	H
X	H	X	X	X	H	H	H	H
X	X	H	X	X	H	H	H	H
H	L	L	L	L	L	H	H	H
H	L	L	L	H	H	L	H	H
H	L	L	H	L	H	H	L	H
H	L	L	H	H	H	H	H	L

A2 = L

*Ena0, $\overline{Ena1}$ or $\overline{Ena2}$ used as DEMUX data input.

B Side

$\overline{Enb}$	B1	B0	$\overline{Q0b}$	$\overline{Q1b}$	$\overline{Q2b}$	$\overline{Q3b}$
H	X	X	H	H	H	H
L	L	L	Q	H	H	H
L	L	H	H	Q	H	H
L	H	L	H	H	Q	H
L	H	H	H	H	H	Q

A2 = L

*Q = L for 2- to 4-line decoding.
Q = $\overline{Enb}$ for 1:4 demultiplexing

The 10G044 functions as either two independent 2-to-4 line decoders or as a single 3-to-8 line decoder. In the dual 2-to-4 mode, the address inputs are A0, A1 and B0, B1 with A2 unused and held low. Each of the two independent decoders accepts their respective A and B address inputs and provides four mutually exclusive active low outputs: $\overline{Q0a}$-$\overline{Q3a}$ and $\overline{Q0b}$-$\overline{Q3b}$ respectively. The A side has one active high and two active low enables; Ena0, $\overline{Ena1}$ and $\overline{Ena2}$. The B side has one active low enable, $\overline{Enb}$.

When disabled, all outputs are forced high. The B enable input and any one of the two active low A side enables (or Ena0 if data inversion is desired) can be used as the data inputs when the 10G044 is operated as a dual 1:4 demultiplexer. In this case, the A2 input must also be held low to enable the B outputs. The remaining two A side enables can be used as data input strobes for the A side demultiplexer. A0, A1 and B0, B1 provide the A side and B side demultiplexer address inputs respectively.

3-TO-8 LINE DECODING & 1:8 DEMULTIPLEXING

Ena0	$\overline{Ena1}$	$\overline{Ena2}$	A2	A1	A0	$\overline{Q0}$	$\overline{Q1}$	$\overline{Q2}$	$\overline{Q3}$	$\overline{Q4}$	$\overline{Q5}$	$\overline{Q6}$	$\overline{Q7}$	FUNCTION
L	X	X	X	X	X	H	H	H	H	H	H	H	H	Output disable
X	H	X	X	X	X	H	H	H	H	H	H	H	H	
X	X	H	X	X	X	H	H	H	H	H	H	H	H	
H	L	L	L	L	L	Q	H	H	H	H	H	H	H	3-to-8 decoding or 1:8 demultiplexing
H	L	L	L	L	H	H	Q	H	H	H	H	H	H	
H	L	L	L	H	L	H	H	Q	H	H	H	H	H	
H	L	L	L	H	H	H	H	H	Q	H	H	H	H	
H	L	L	H	L	L	H	H	H	H	Q	H	H	H	
H	L	L	H	L	H	H	H	H	H	H	Q	H	H	
H	L	L	H	H	L	H	H	H	H	H	H	Q	H	
H	L	L	H	H	H	H	H	H	H	H	H	H	Q	

Enb = H Q = L for 3-to-8 decoding; Q = Ena0 inverse, $\overline{Ena1}$ or $\overline{Ena2}$ for 1:8 demultiplexing.

In the 3-to-8 line decoder mode, the 10G044 accepts three binary weighted inputs - A0, A1 and A2 - and when enabled, provides eight mutually exclusive active low outputs, $\overline{Q0}$ through $\overline{Q7}$. The $\overline{Enb}$ pin must be tied high in this mode. To configure an eight output addressable demultiplexer, the address inputs are provided on A0, A1 and A2 and either Ena1 or $\overline{Ena2}$ is used as the data input pin (or Ena0 if data inversion is desired). The remaining two unused A side enables can be used as data input strobes. Enb must be held high in this case as well.

BOOLEAN FUNCTION GENERATION

When A2 is held low, the 10G044 can simultaneously generate the four minterms of the input variables A0 and A1 and the four minterms of inputs B0 and B1. Additionally, when A2 is held high, the 10G044 will generate the minterms of the A inputs (A0, A1) NORed with the minterms of the B inputs in corresponding pairs. In both cases, the generation of A and B input minterms can be controlled by the respective A and B input enables. These operations are shown in the following three truth tables.

Minterm generation of the variables A0 and A1 and associated enables

Ena0	$\overline{Ena1}$	$\overline{Ena2}$	A1	A0	$\overline{Q0a}$	$\overline{Q1a}$	$\overline{Q2a}$	$\overline{Q3a}$	FUNCTION	
L	X	X	X	X	H	H	H	H	Output disable	
X	H	X	X	X	H	H	H	H		
X	X	H	X	X	H	H	H	H		
H	L	L	L	L	L	H	H	H	A minterms	$\overline{Q0a} = \overline{(A0 \cdot A1)}$
H	L	L	L	H	H	L	H	H		$\overline{Q1a} = \overline{(A0 \cdot \overline{A1})}$
H	L	L	H	L	H	H	L	H		$\overline{Q2a} = \overline{(\overline{A0} \cdot A1)}$
H	L	L	H	H	H	H	H	L		$\overline{Q3a} = \overline{(\overline{A0} \cdot \overline{A1})}$

A2 = L

Minterm generation of the variables B0 and B1 & associated enables

$\overline{Enb}$	B1	B0	$\overline{Q0b}$	$\overline{Q1b}$	$\overline{Q2b}$	$\overline{Q3b}$	FUNCTION
H	X	X	H	H	H	H	Output disable
L	L	L	L	H	H	H	B Minterms $\overline{Q0b} = \overline{(\overline{B0} \cdot \overline{B1})}$
L	L	H	H	L	H	H	$\overline{Q1b} = \overline{(\overline{B0} \cdot B1)}$
L	H	L	H	H	L	H	$\overline{Q2b} = \overline{(B0 \cdot \overline{B1})}$
L	H	H	H	H	H	L	$\overline{Q3b} = \overline{(B0 \cdot B1)}$

A2 = L

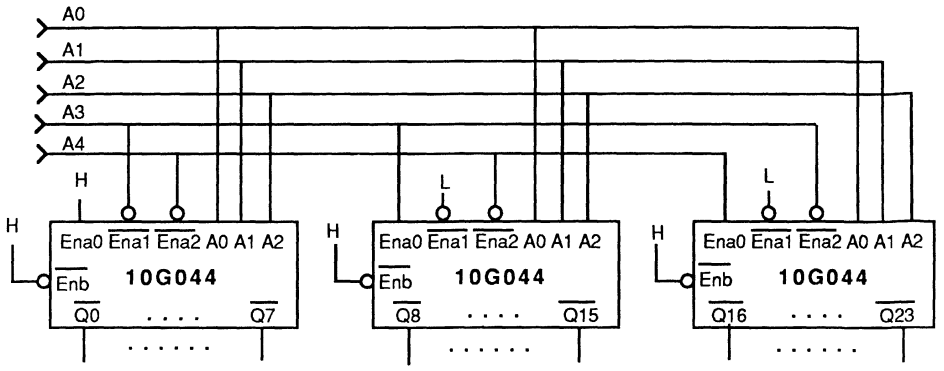
Again, the operations expressed in these previous two tables can occur simultaneously. When A2 is held high, the eight individual minterms described above are functionally NORed together in corresponding pairs and are made available on the four $\overline{Qb}$ output pins. In addition, by controlling the $\overline{Ena2}$ and $\overline{Enb}$ pins, the minterms of the A0, A1 inputs or the B0, B1 inputs can be generated and directed to the same $\overline{Qb}$ output pins. These operations are shown in the following table.

Selecting B output minterms and sum of products minterm generation

Ena0	$\overline{Ena1}$	$\overline{Ena2}$	$\overline{Enb}$	A1	A0	B1	B0	$\overline{Q0b}$	$\overline{Q1b}$	$\overline{Q2b}$	$\overline{Q3b}$	FUNCTION
L	X	X	H	X	X	X	X	H	H	H	H	
X	H	X	H	X	X	X	X	H	H	H	H	Output disable
X	X	H	H	X	X	X	X	H	H	H	H	
H	L	L	H	0	0	X	X	L	H	H	H	$\overline{Q0b} = \overline{(\overline{A0} \cdot \overline{A1})}$
H	L	L	H	0	1	X	X	H	L	H	H	$\overline{Q1b} = \overline{(A0 \cdot \overline{A1})}$
H	L	L	H	1	0	X	X	H	H	L	H	$\overline{Q2b} = \overline{(\overline{A0} \cdot A1)}$
H	L	L	H	1	1	X	X	H	H	H	L	$\overline{Q3b} = \overline{(A0 \cdot A1)}$
X	X	H	L	X	X	0	0	L	H	H	H	$\overline{Q0b} = \overline{(\overline{B0} \cdot \overline{B1})}$
X	X	H	L	X	X	0	1	H	L	H	H	$\overline{Q1b} = \overline{(B0 \cdot \overline{B1})}$
X	X	H	L	X	X	1	0	H	H	L	H	$\overline{Q2b} = \overline{(\overline{B0} \cdot B1)}$
X	X	H	L	X	X	1	1	H	H	H	L	$\overline{Q3b} = \overline{(B0 \cdot B1)}$
H	L	L	L	0	0	0	0	L	H	H	H	
H	L	L	L	0	0	0	1	L	L	H	H	
H	L	L	L	0	0	1	0	L	H	L	H	
H	L	L	L	0	0	1	1	L	H	H	L	
H	L	L	L	0	1	0	0	L	L	H	H	$\overline{Q0b} = \overline{(\overline{A0} \cdot \overline{A1}) + (\overline{B0} \cdot \overline{B1})}$
H	L	L	L	0	1	0	1	H	L	H	H	
H	L	L	L	0	1	1	0	H	L	L	H	$\overline{Q1b} = \overline{(A0 \cdot \overline{A1}) + (B0 \cdot \overline{B1})}$
H	L	L	L	0	1	1	1	H	L	H	L	
H	L	L	L	1	0	0	0	L	H	L	H	$\overline{Q2b} = \overline{(\overline{A0} \cdot A1) + (\overline{B0} \cdot B1)}$
H	L	L	L	1	0	0	1	H	L	L	H	
H	L	L	L	1	0	1	0	H	H	L	H	$\overline{Q3b} = \overline{(A0 \cdot A1) + (B0 \cdot B1)}$
H	L	L	L	1	0	1	1	H	H	L	L	
H	L	L	L	1	1	0	0	L	H	H	L	
H	L	L	L	1	1	0	1	H	L	H	L	
H	L	L	L	1	1	1	0	H	H	L	L	
H	L	L	L	1	1	1	1	H	H	H	L	

A2 = H

EXPANSION TO 24 DECODED OUTPUTS



A4	A3	
0	0	Only Q0 to Q7 enabled
0	1	Only Q8 to Q15 enabled
1	0	Only Q16 to Q23 enabled
1	1	All outputs disabled (high)

H = Vddo or Vddl
L = Vtt or Vss

PIN DESCRIPTIONS

A0, A1,A2	3:8 decoder address inputs
A0, A1	2:4 decoder A address inputs
$\overline{Ena0}$, $\overline{Ena1}$, $\overline{Ena2}$	3:8 and 2:4 decoder A side enable inputs
B0, B1	2:4 decoder B address inputs
$\overline{Enb}$	2:4 decoder B enable input
$\overline{Q0}$ - $\overline{Q7}$	3:8 decoder outputs
$\overline{Q0a}$ - $\overline{Q3a}$	2:4 decoder A outputs
$\overline{Q0b}$ - $\overline{Q3b}$	2:4 decoder B outputs
VDDO	Ground connection for the output drivers
VDDL	Ground connection for internal switching logic
VSS	-3.4V power supply
VEE	-5.2V power supply
VTTC	Internal VDDO decoupling capacitor return pin. VTTC is brought into the 10G044 package as the AC return lead for the internal VDDO output driver decoupling capacitor. It is not brought onto the 10G044 die. VTTC is typically tied to VTT (nom. -2.0V).
VBB	Input to the 10G044's input threshold compensation circuit. Connect to Vbb supplied from ECL when driving from ECL; connect to the PicoLogic threshold reference voltage (VBBS) when driving from PicoLogic. (NOTE: the 10G044 does not provide a VBBS output).
DNC	Do Not Connect to this pin.
N/C	No connection.

DC CHARACTERISTICS

Tc = 0°C to 85°C, VSS = -3.5 V TO -3.3 V, VEE = -5.5 TO -5.1 V, VDDL = VDDO = Gnd., unless otherwise indicated

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
VIH	Input Voltage High					1
VIL	Input Voltage Low					1
ISS	Power Supply Current		280	370	mA	
IEE	Power Supply Current		75	100	mA	
PD	Power Dissipation		1.35	1.8	W	

NOTES:

The remaining DC Characteristics are specified in the 10G PicoLogic™ Family Electrical Characteristics Table at the beginning of this section. This table notes parameter deviations to Family Characteristics and provides specific supplementary characteristics only.

1. Ena1 and Ena2 are unbuffered inputs. Either one, but not both simultaneously, may be driven with ECL levels. The other must be driven with GaAs levels of VIH min = -0.8 V and VIL max = -1.8 V.

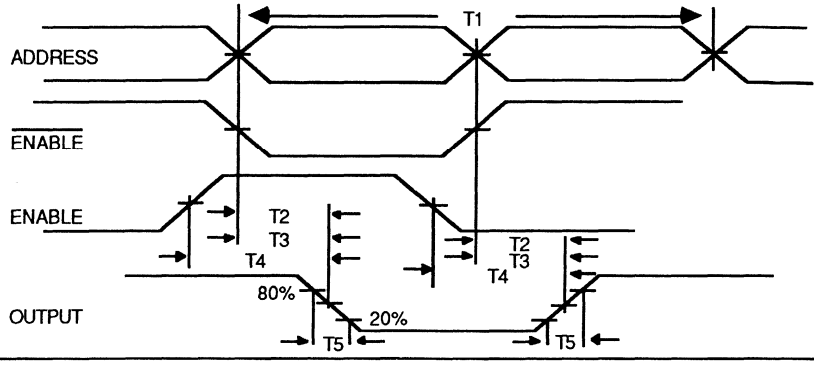
AC CHARACTERISTICS (Note 1)

10G044-2 VSS = -3.5V to -3.3V, VEE = -5.5V to -5.1V, VDDL=VDDO = 0V, unless otherwise indicated.

SYMBOL	PARAMETER	Tc = 0°C		Tc = +25°C			Tc = +85°C		UNITS	NOTES
		MIN	MAX	MIN	TYP	MAX	MIN	MAX		
1/T1	Input frequency	1.2		1.2	1.6		1.2		GHz	
T2	Address to output delay	400	700	325	500	650	425	750	ps	
T3	Enable to output delay	475	850	450	650	800	500	900	ps	
T4	Enable to output delay	525	950	500	750	900	550	1000	ps	
T5	Output rise and fall times		175		125	175		215	ps	2

Notes: 1. Test conditions (unless otherwise noted): Vbb = -1.2V; Vtt = -2.0V; Vttc = Vtt; Rload = 50Ω to Vtt; Vih = -0.7V; Vil = -1.7V; Voh≥ -0.7V; Vol ≤ -1.7V. Input signal rise and fall times ≤ 150 ps.
2. Rise & fall times are measured at the 20% and 80% points of the transition from VOL max to VOH min.

SWITCHING WAVEFORMS



Dual 9-Bit Parity Generator & Checker 8-Bit Word Comparator • 850 ps Delay

10G PicoLogic™ Family

DISTINCTIVE CAPABILITIES

- Generate or check even or odd parity for two sets of 8 data lines (1300 ps)
- Generates equivalence of two 8 bit words (850 ps)
- Check equivalence and parity of two 8 bit words simultaneously (1300 ps)
- Cascadable for N-bits parity
- Up to1.5 GHz input frequency
- ECL and Picologic family compatible I/O
- Wired-OR output capability
- On-chip threshold compensation circuit and reference voltage generator
- Available in leadless or C-leaded chip carriers or in unpackaged die form
- Packages contain internal decoupling capacitors for optimum high frequency performance
- 0° to 85° operating temperature range

APPLICATIONS

- Cache tag comparison
- Frame synchronization & code identification
- Correlation
- Parity generation and checking

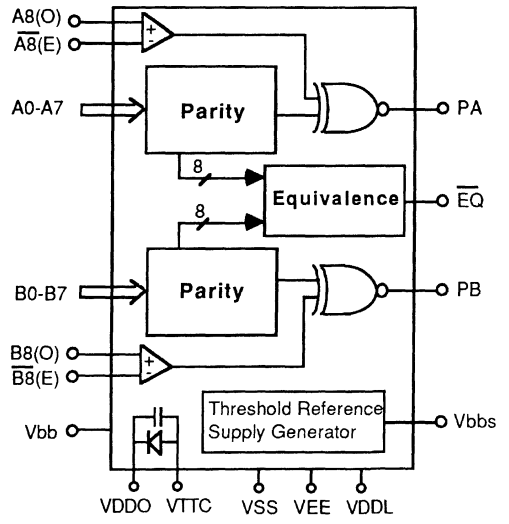
FUNCTIONAL DESCRIPTION

The 10G045 is an ECL and PicoLogic family compatible ultra-fast dual 9-bit parity checker, 8-bit parity generator and 8 bit word comparator. The device can be configured to generate even or odd parity and can be cascaded to provide N-bit parity. The equivalence and parity of two 8-bit words can be checked simultaneously. For compatibility with any ECL or GaAs logic family, the 10G045 incorporates the PicoLogic standard input threshold compensation circuit driven by the VBB input as well as an on-chip threshold reference generator which provides a nominal -1.3V reference voltage on the VBBS output pin.

Typical data to parity output propagation delay is 1000 ps; typical data input to equivalence output delay is 700 ps; typical parity input to parity output delay is 700 ps. Operation at 1.5 GHz can be sustained while dissipating less than 1.2 W at room temperature. Output rise and fall times are typically 150 ps.

The 10G045 is a member of GigaBit Logic's 10G PicoLogic family of gallium arsenide integrated circuits and is fabricated using Gigabit's high volume, GaAs MESFET process technology.

BLOCK DIAGRAM



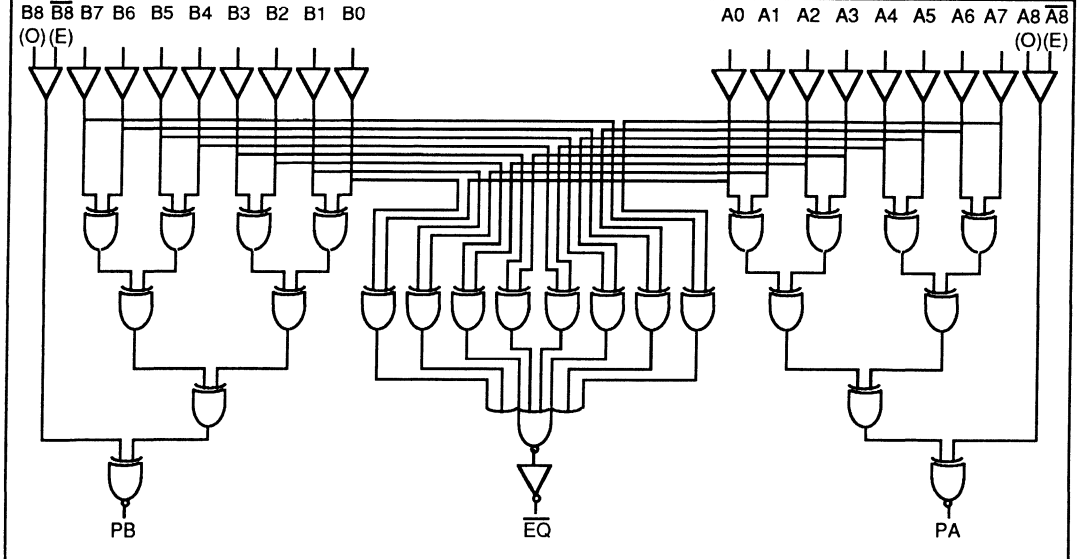
10G045 ORDERING INFORMATION

PACKAGE TYPE	DELAY (Max. @ 25°C)
	850 ps ($\overline{EQ}$ Output)
Leadless CC	10G045-2L
C-leaded CC	10G045-2C
Dice	10G045-2X

PIN DESCRIPTIONS

A0 - A7	Data inputs, A word.
B0 - B7	Data inputs, B word.
A8(O), B8(O)	Odd parity inputs.
$\overline{A8}$(E), $\overline{B8}$(E)	Even parity inputs.
$\overline{EQ}$	Equivalence output of words A and B.
PA, PB	Parity outputs of words A and B. Programmable for even or odd parity.
VDDO	Output driver ground (0V).
VDDL	Internal logic ground (0V).
VSS	- 3.4V power supply.
VEE	- 5.2V power supply.
VDCH	Output driver high level clamp voltage. When driving other GaAs devices, VDCH is generally left unconnected. When driving ECL, VDCH may be used to limit VOH. Consult App. Note 4 for details.
VTTC	Internal VDDO decoupling capacitor return pin. VTTC is brought into the 10G045 package as the AC return lead for the internal VDDO output driver decoupling capacitor. It is not brought onto the 10G045 die. VTTC is typically tied to VTT (nom. -2.0V).
VBB	Reference input to the 10G045's input threshold compensation circuit. Connect to the VBB supplied from ECL when driving the 10G045 from ECL. Connect to the VBBS pin when the 10G045 is driven from PicoLogic. This pin may not be left unconnected.
VBBS	PicoLogic threshold reference output voltage. Nominally equal to -1.3V with a 40Ω source impedance. Connect to VBB when driving from PicoLogic. ΔVBBS/ΔTemp. = 0.6mV/°C; ΔVBBS/ΔVSS = 0.2mV/mV.

10G045 LOGIC DIAGRAM



TRUTH TABLES

The 10G045 can be programmed for even or odd parity by appropriate connection of the even and odd parity inputs as shown below.

Generate EVEN parity of 8-bit word (A side shown)

Input A8(O)	Input $\overline{A8}$(E)	Sum of HIGH Inputs A0 - A7	Output PA
H	L or VBB(S)	EVEN	L
H	L or VBB(S)	ODD	H

Generate ODD parity of 8-bit word (A side shown)

Input A8(O)	Input $\overline{A8}$(E)	Sum of HIGH Inputs A0 - A7	Output PA
L	H or VBB(S)	EVEN	H
L	H or VBB(S)	ODD	L

Check EVEN parity of 9-bit word (A side shown)

Input A8(O)	Sum of HIGH Inputs A0 - A7, $\overline{A8}$(E)	Output PA
VBB(S)	EVEN	L
VBB(S)	ODD (Parity Error)	H

Check ODD parity of 9-bit word (A side shown)

Input $\overline{A8}$(E)	Sum of HIGH Inputs A0 - A7, A8(O)	Output PA
VBB(S)	ODD	L
VBB(S)	EVEN (Parity Error)	H

Equivalence of two 8-bit words:

$\overline{EQ} = (A0 \oplus B0) + (A1 \oplus B1) + (A2 \oplus B2) + (A3 \oplus B3) + (A4 \oplus B4) + (A5 \oplus B5) + (A6 \oplus B6) + (A7 \oplus B7)$

DC CHARACTERISTICS

Tc = 0°C to 85°C, VSS = -3.5 V TO -3.3 V, VEE = -5.5 TO -5.1 V, VDDL = VDDO = Gnd, unless otherwise indicated

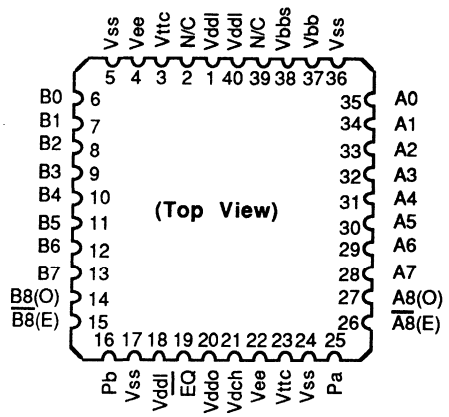
SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
ISS	Power Supply Current		175	240	mA
IEE	Power Supply Current		115	150	mA
PD	Power Dissipation		1.2	1.6	W

NOTE:

The remaining DC Characteristics are specified in the 10G PicoLogic™ Family Electrical Characteristics Table at the beginning of this section. This table notes parameter deviations to Family Characteristics and provides specific supplementary characteristics only.

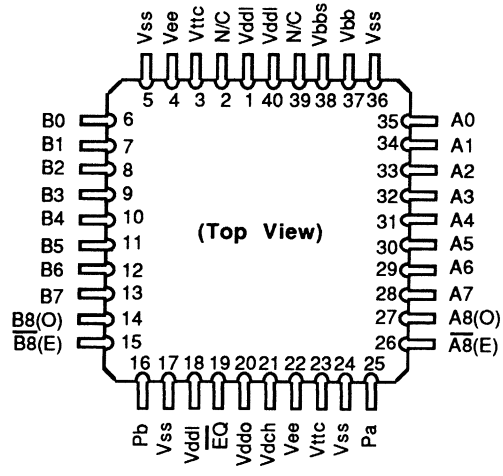
PACKAGE PINOUT DIAGRAMS

PACKAGE TYPE "L"



NOTES: Pin 1 is marked for orientation. N/C = No Connection.

PACKAGE TYPE "C"



NOTES: Pin 1 is marked for orientation. N/C = No Connection.

AC CHARACTERISTICS (Note 1)

10G045-2 VSS = -3.5V to -3.3V, VEE = -5.5V to -5.1V, VDDL=VDDO = Gnd, unless otherwise indicated.

SYMBOL	PARAMETER	Tc = 0°C		Tc = +25°C			Tc=+85°C		UNITS	NOTES
		MIN	MAX	MIN	TYP	MAX	MIN	MAX		
1/(2T1)	Operating frequency	1.0		1.1	1.5		1.0		GHz	
T2	Data to parity output high delay	800	1300	800	1000	1300	800	1300	ps	
T3	Data to parity output low delay	800	1300	800	1000	1300	800	1300	ps	
T4	Parity input to parity output high delay	550	900	550	700	900	550	900	ps	
T5	Parity input to parity output low delay	550	900	550	700	900	550	900	ps	
T6	Data input to EQ output high delay	550	950	550	700	850	550	900	ps	
T7	Data input to EQ output low delay	550	950	550	700	850	550	900	ps	
T8	Output rise time		200		150	200		200	ps	2
T9	Output fall time		150		150	200		150	ps	2

Notes: 1. Test conditions (unless otherwise indicated) :

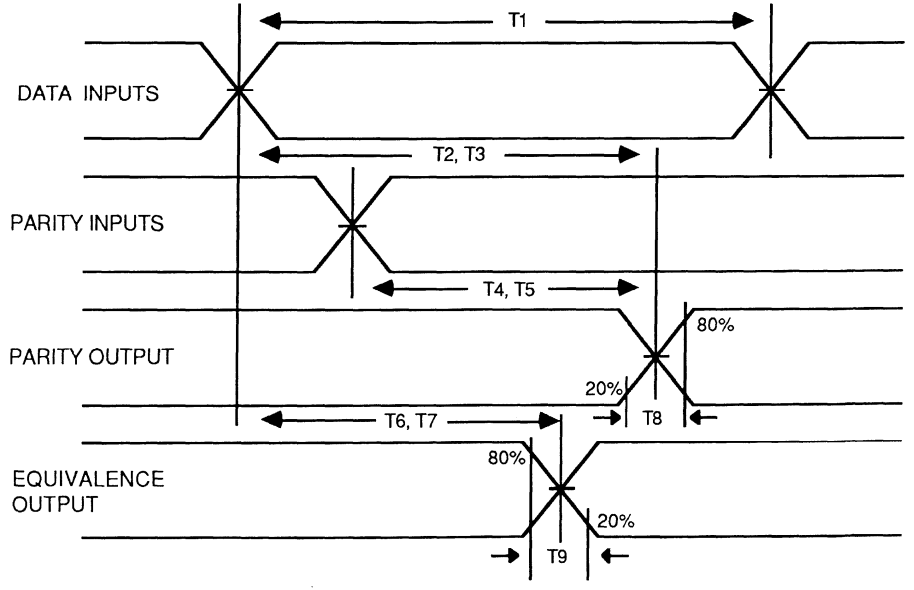
VBB = -1.2V
VTT = -2.0V
VTTC = VTT
RLOAD = 50Ω to -2.0V
Input signal rise and fall time ≤ 150 ps

VIH = -0.7V
VIL = -1.7V
VOH ≥ -0.7V
VOL ≤ -1.7V

VDCH = VDDO

2. Rise and fall times are measured at the 20% and 80% points of the transition from Vol max to Voh min.

SWITCHING WAVEFORMS



Quad 4:1 or Dual 8:1 Data Multiplexer
1.5 GHz /600 ps Propagation Delay
10G PicoLogic™ Family

DISTINCTIVE CAPABILITIES

- Dual 8:1 or quad 4:1 configurations controlled by Mode input
- Data paths controlled by 3 common select lines
- Common output enable control
- 150 ps typical output rise, fall times
- ECL and PicoLogic compatible I/O
- Temperature and voltage compensated using VBB threshold reference input
- On-chip VBBS (-1.2V) reference voltage supply
- Output wire - OR capability for expansion to 16:1 MUX
- Available in C - leaded or leadless chip carrier or dice form

APPLICATIONS

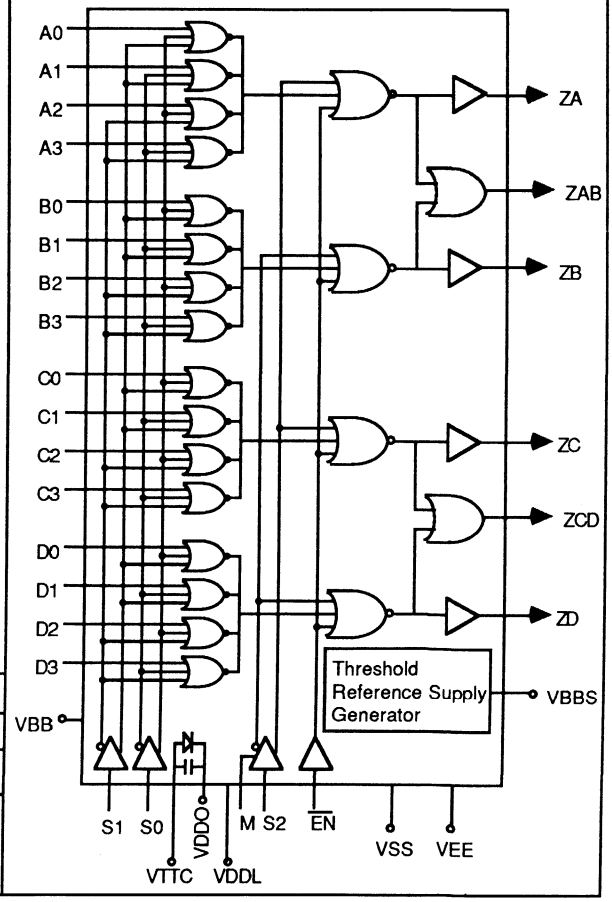
- High speed test equipment
- General purpose multiplexing
- High speed word generation

FUNCTIONAL DESCRIPTION

The 10G046 is a high speed dual 8:1 or quad 4:1 data multiplexer with three common select lines and a common output enable. A dc mode control (M), strapable to VDDL or VSS, is provided to select between 8:1 or 4:1 operating modes. The 10G046 has16 data inputs, A0...A3, B0...B3, C0...C3 and D0...D3. When M is high (=VDDL), S0 and S1 provide a common 4:1 data selection to ZA, ZB, ZC and ZD. When M is low (=VSS), S0, S1 and S2 are used to provide a common 8:1 data selection to the ZAB and ZCD outputs. A common enable ($\overline{EN}$) enables all outputs when low. Note that M must be strapped to VDDL or VSS and not driven by logic.

The 10G046 is designed to provide general purpose logical multiplexing for bus structures, data and address multiplexing and fan-in of data channels or interrupt signals. Two devices can be easily interconnected to form a dual 16:1 MUX by wire-OR tying their respective 8:1 outputs and driving the $\overline{EN}$ inputs with an S3 select line (see drawing pg. 2). The 10G046 is a member of GigaBit's PicoLogic family of GaAs digital integrated circuits, and is fabricated using GigaBit's high volume GaAs MESFET process technology.

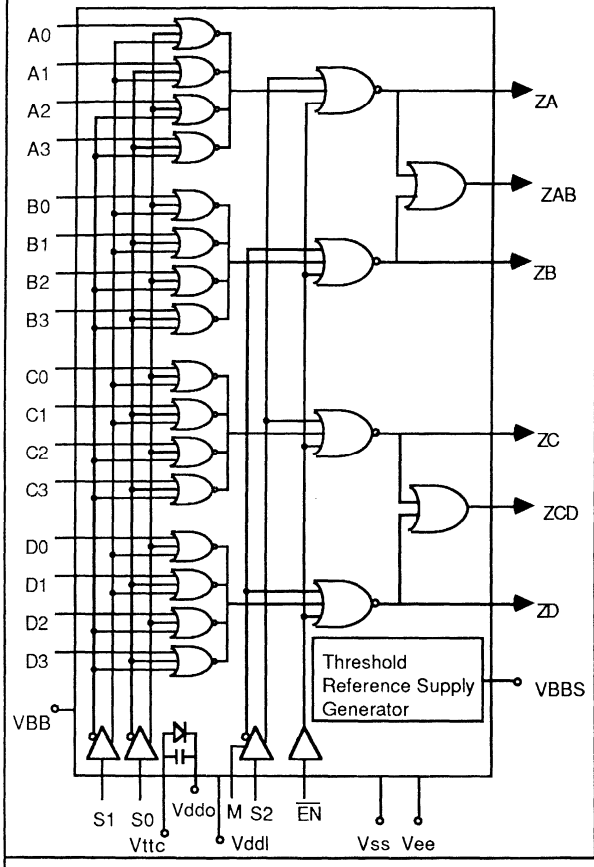
LOGIC DIAGRAM



10G046 ORDERING INFORMATION

PACKAGE TYPE	SPEED (Min. 0°C to 85°C)	
	1.5 GHz	1.25 GHz
C-Leaded CC Leadless CC Dice	10G046-2C 10G046-2L	10G046-3C 10G046-3L 10G046-3X

LOGIC DIAGRAM



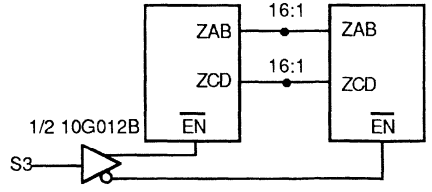
Truth Table 2 X 8:1

Mode M	Enable $\overline{EN}$	Select Inputs S0	S1	S2	Outputs ZAB	ZCD
L	L	L	L	L	A0	C0
L	L	H	L	L	A1	C1
L	L	L	H	L	A2	C2
L	L	H	H	L	A3	C3
L	L	L	L	H	B0	D0
L	L	H	L	H	B1	D1
L	L	L	H	H	B2	D2
L	L	H	H	H	B3	D3
X	H	X	X	X	L	L

Truth Table 4 X 4:1

Mode M	Enable $\overline{EN}$	Select Inputs S0	S1	S2	Outputs ZA	ZB	ZC	ZD
H	L	L	L	X	A0	B0	C0	D0
H	L	H	L	X	A1	B1	C1	D1
H	L	L	H	X	A2	B2	C2	D2
H	L	H	H	X	A3	B3	C3	D3
X	H	X	X	X	L	L	L	L

DUAL 16:1 MUX



PIN DESCRIPTIONS

A0 - A3	Data inputs, A group
B0 - B3	Data inputs, B group
C1 - C3	Data inputs, C group
D0 - D3	Data inputs, D group
S0, S1, S2	Data select inputs
M	Mode control input (selects 8:1 or 4:1 operating mode; tie to Vddl or Vss)
$\overline{EN}$	Active low output enable control (GaAs level compatible only)
ZA	4:1 output of group A inputs
ZAB	8:1 output of group A and B inputs
ZB	4:1 output of group B inputs
ZC	4:1 output of group C inputs
ZCD	8:1 output of group C and D inputs
ZD	4:1 output of group D inputs
VDDO	Output driver ground pin
VDDL	Internal logic ground pin
VSS	-3.4 volt power supply
VEE	- 5.2 volt power supply
VTTC	AC return lead for the package internal VDDO decoupling capacitor. Typically connect to VTT.
VBB	Threshold reference level input. Provides temperature and voltage compensation of the input threshold. Connect to VBBS when driving from PicoLogic. When driving from ECL or other GaAs families, connect to that families' threshold voltage. This pin may not be left unconnected.
VBBS	PicoLogic threshold reference voltage output. Nominally equal to - 1.2V with a 40Ω source impedance. Connect to VBB when interfacing to PicoLogic. $\Delta VBBS/\Delta Temp$ = 0.6mV/°C, $\Delta VBBS/\Delta VSS$ = 0.2mV/mV.

DC CHARACTERISTICS

Tc = 0°C to 85°C, VSS = -3.5 V TO -3.3 V, VEE = -5.5 TO -5.1 V, VDDL = VDDO = Gnd, unless otherwise indicated

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
VIHEn	VIH for $\overline{EN}$ input	-0.8		VDDL	V
VILEn	VIL for $\overline{EN}$ input	VSS		-1.8	V
VBBS	Threshold Reference Voltage		-1.2		V
ISS	Power Supply Current		290	400	mA
IEE	Power Supply Current		120	160	mA
PD	Power Dissipation		1610	2190	mW

NOTE:

The remaining DC Characteristics are specified in the 10G PicoLogic™ Family Electrical Characteristics Table at the beginning of this section. This table notes parameter deviations to Family Characteristics and provides specific supplementary characteristics only.

AC CHARACTERISTICS (Note 1)

10G046-2

VSS = -3.5V to -3.3V, VEE = -5.5V to -5.1V, VDDL=VDDO = 0V, unless otherwise indicated.

SYMBOL	PARAMETER	Tc = 0°C		Tc = +25°C			Tc = +85°C		UNITS	NOTES
		MIN	MAX	MIN	TYP	MAX	MIN	MAX		
F	Operating frequency	1.5		1.5	1.7		1.5		GHz	2
T1	Data inputs to output delay	300	600	300	450	600	300	600	ps	
T2	Enable input to output delay	350	750	350	575	750	350	750	ps	
T3	S0 or S1 input to output delay	400	800	400	650	800	400	800	ps	
T4	S2 input to output delay	375	700	375	500	700	375	700	ps	
T5	Output rise and fall times		175		125	175		200	ps	3

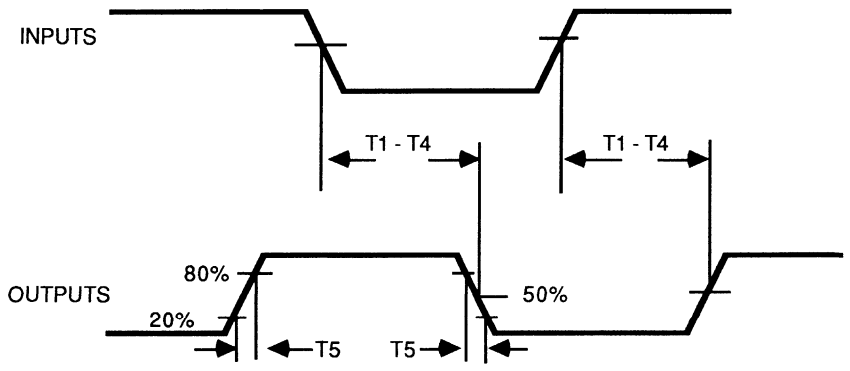
10G046-3

SYMBOL	PARAMETER	Tc = 0°C		Tc = +25°C			Tc = +85°C		UNITS	NOTES
		MIN	MAX	MIN	TYP	MAX	MIN	MAX		
F	Operating frequency	1.25		1.25	1.5		1.25		GHz	2
T1	Data inputs to output delay	350	600	350	525	600	350	600	ps	
T2	Enable input to output delay	400	800	400	650	800	400	800	ps	
T3	S0 or S1 input to output delay	450	825	450	700	825	450	825	ps	
T4	S2 input to output delay	425	800	425	550	800	425	800	ps	
T5	Output rise and fall times		175		150	175		200	ps	3

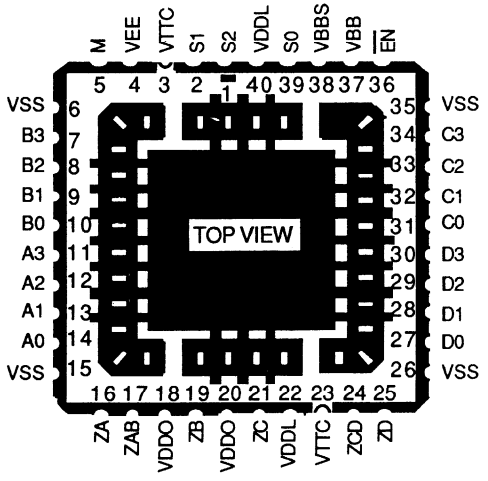
NOTES:

1. Test conditions (unless otherwise noted): VBB = -1.2V, VTT = -2.0V, VTTC = VTT, Rload = 50Ω to VTT, VIH = -0.7V, VIL = -1.7V, VOH ≥ -0.7V, VOL ≤ -1.7V. Input signal rise and fall times <150ps.
2. Operating frequency is limited by output pull down level (VOL). Providing a 300Ω resistor on the output pin to VSS will increase performance by several hundred MHz while maintaining VOL ≤ -1.7V.
3. Output rise and fall times are measured at the 20% and 80% points of the transition from VOL max to VOH min.

SWITCHING WAVEFORMS



PIN FUNCTIONS - PACKAGE TYPES "L" AND "C"



NOTES:
Pin 1 is marked for orientation. N/C = no connection.

GigaBit Logic

10G050
ADVANCE

8x8x1 Expandable Crosspoint Switch
2 Gbit/s Data Rate / 1 ns Reconfiguration Time
10G PicoLogic™ Family

DISTINCTIVE CAPABILITIES

- Full broadcast switching capability (any output can select any input)
- Expandable to 8Px8QxR crosspoint switch with no external components
- Flow-through or registered data input mode
- 500 MHz destination control update rate
- 25Ω output drive capability
- ECL and PicoLogic I/O compatible
- Temperature and voltage compensated using Vbb threshold reference input
- On-chip Vbbs threshold reference supply
- Available in 68 pin leaded chip carrier or unpackaged die form

APPLICATIONS

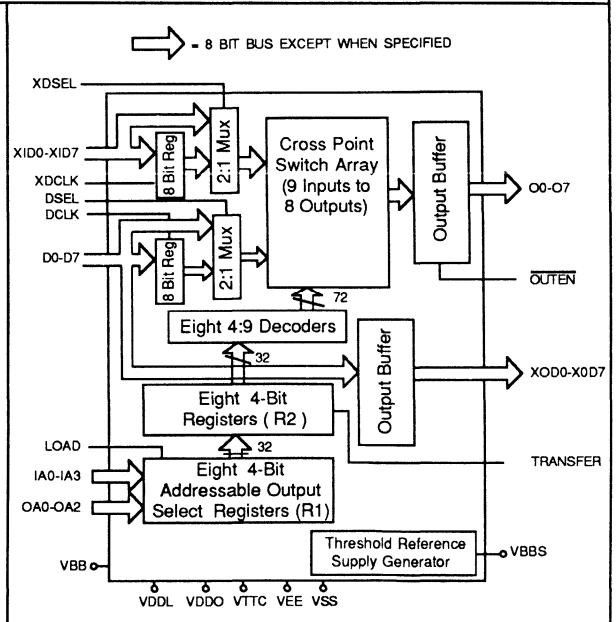
- Fiber optic or microwave data distribution
- Digital video switching equipment
- High speed test equipment
- Digital demultiplexing

FUNCTIONAL DESCRIPTION

The 10G050 is a high speed 8x8x1 crosspoint switch capable of passing up to 1 GHz signals (2 Gbit/s NRZ data rate). The switch can be completely reconfigured in just 1 ns. The 10G050 features full broadcast capability. Each output (Oi) can independently select any of the 8 inputs (D0-D7) including an input chosen by another output, or the correspondingly indexed expanded input (XIDi). An output is connected to a given input by loading the address of the desired input (IA0-IA3) into one of 8 internal 4-bit output select registers which are addressed by inputs OA0-OA2. In order to minimize the time to completely reconfigure the switch, the 10G050 features a double row of output select registers, R1 and R2. While the switch is active and prior to the time at which it will be reconfigured, R1 can be serially loaded at a 1.5 ns rate with a new set of input addresses. Therefore, a complete update of the output select registers requires 12 ns. When all required input addresses have been updated, the content of R1 is parallel transfered to R2 (using the "Transfer" control), resulting in complete switch reconfiguration in just 1 ns. Individual path changes require 2.5 ns to complete.

The 10G050 is expanded via use of the expand data outputs (XOD0-XOD7) and expand data inputs (XID0-XID7).

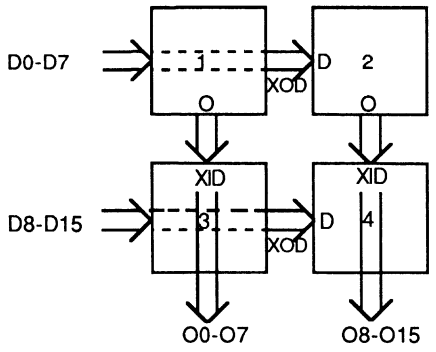
The 10G050 is fabricated using GigaBit's high volume GaAs MESFET process technology.



10G050 ORDERING INFORMATION

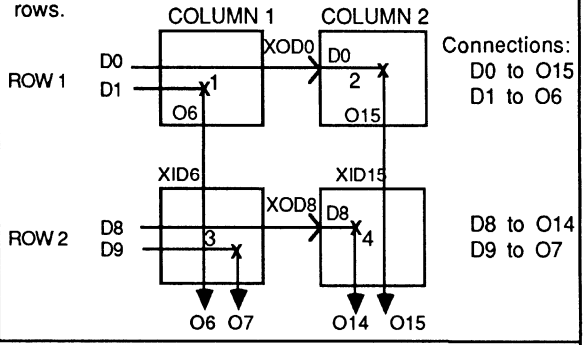
PACKAGE TYPE	10G050-2 2.0 Gbit/s	
C-Leaded CC Leadless CC Die	10G050-2C 10G050-2L 10G050-2X	

EXPANSION TO A 16X16X1 CROSS POINT SWITCH



Crosspoint 1:Switches D0-D7 to O0-O7.
Crosspoint 2:Switches D0-D7 to O8-O15.
Crosspoint 3:Switches D8-D15 to O0-O7 and/or reproduces outputs of crosspoint 1 via XD.
Crosspoint 4:Switches D8-D15 to O8-O15 and/or repoduces outputs of crosspoint2 via XD.

Example: connecting D0, D1, D8, D9 to O6, O7, O14, O15 respectively.
The switching operation is realized by the 10G050 at the intersection of the input and output connected together (shown by "Xs" in the diagram).
Expanded outputs (XODi) are buffered inputs flowed through to subsequent columns (in our ex. , column 2).
Expanded inputs (XIDi) are used when the switching operation has been realized in a previous row (in our ex. row 1) and only a flow through is necessary in subsequent rows.



Connections:
D0 to O15
D1 to O6
D8 to O14
D9 to O7

PIN DESCRIPTIONS

D0-D7	Input Data.
O0-O7	Output Data.
XID0-XID7	Expansion Input Data.
XOD0-XOD7	Expansion Output Data: buffered input data enabling expansion with no external components.
DSEL	Data Select; selects registered data when low and flowthrough data when high.
XDSEL	Expansion Data Select; selects registered expansion data when low and flowthrough expansion data when high.
DCLK	Input data register clock.
XDCLK	Expansion input data register clock.
OUTEN	Active low Output data enable.
IA0-IA3	Input data addresses.
OA0-OA2	Output select register addresses: decoded to match an input pin to the selected output pin.
LOAD	Loads IA0-IA3 into the register addressed by OA0-OA2 at the rising edge of the signal.
TRANSFER	The content of R1 is parallel loaded in R2 at the rising edge of the Transfer signal, resulting in complete switch reconfiguration .
VDDO	Output driver ground pin (0V)
VDDL	Internal logic ground connection (0V)
VSS	-3.4 V power supply
VEE	-5.2 V power supply
VDCH	Output driver high level clamp voltage. When driving other GaAs devices, VDCH is generally left unconnected. When driving ECL, VDCH may be used to limit VOH. Consult Application Note 4 for detail.
VBB	Reference input to the 10G050's input threshold tracking circuit. Connect to the VBB supplied from ECL when driving the 10G050 from ECL. Must be strapped to the VBBS pin when the 10G050 is driven from PicoLogic. This pin may not be left unconnected.
VBBS	PicoLogic threshold reference output voltage. Connect to VBB when driving from PicoLogic. $\Delta VBBS/\Delta Temp$ = 0.6mV/°C; $\Delta VBBS/\Delta VSS$ = 0.2 mV/mV.

DC CHARACTERISTICS (Notes 1,2)

TC = 0°C to 85 °C, VSS = -3.5V to -3.3V, VEE = -5.5V to -5.1V, VDDL=VDDO = 0V, unless otherwise indicated.

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	TEST CONDITIONS	NOTES
VOH	Output Voltage High	- 0.8	-0.4	- 0.3	V		
VOL	Output Voltage Low	- 2.0	-1.9	- 1.8	V		
IOH	Output Current High		-70	- 60	mA	VOH = - 0.8V	3
VIH	Input Voltage High	- 1.0		VDDL	V		
VIL	Input Voltage Low	VSS		- 1.6	V		
IIN	Input Current	-500	150	500	uA	VIN = -0.8V to -1.8V	
VBBS	Threshold Reference Voltage		-1.2		V		5
ISS	Power Supply Current		750		mA		
IEE	Power Supply Current		250		mA		
PD	Power Dissipation		3.85		W		4

Notes: 1. These characteristics are applicable from DC to 500 MHz.
2. Test conditions (unless otherwise indicated) :
VBB = -1.2V VDCH = VDDO
VTT = -2.0V
VTTC = VTT
RLOAD = 50Ω to VTT
3. IOH is the available output current at VOH = -0.8V.
4. At nominal supply voltages and 50% duty cycle. Exclusive of VDDO output source follower power (typically 15 mW per loaded output) and VDCH power, if any.
5. Nominally equal to -1.2V with a 40Ω source impedance. The range of VBBS at 25°C is -1.05 to -1.3V. ΔVBBS/ΔTemp. = +0.6mV/°C; ΔVBBS/ΔVSS = +0.2mV/mV.

AC CHARACTERISTICS (Note 1)

10G050-2

VSS = -3.5V to -3.3V, VEE = -5.5V to -5.1V, VDDL=VDDO = 0V, unless otherwise indicated.

SYMBOL	PARAMETER	Tc = 0°C		Tc = +25°C			Tc=+85°C		UNITS	NOTES
		MIN	MAX	MIN	TYP	MAX	MIN	MAX		
Fd	Input NRZ data rate				2.0				Gb/s	
Fc	Clock Frequency				1.0				GHz	
Td1	Data in (Di or XIDi) to data out (Oi) (registers bypassed)				500				ps	
Td2	Data in(Di) to expanded data out(XODi)				350				ps	
Td3	Clock (CLK) to data out (Oi)				900				ps	
Td4	Output Enable(OUTEN) to data out(Oi)				1300				ps	
Td5	Transfer to data out (Oi)				1000				ps	
Td6	LOAD to addresses in (IAi)				1500				ps	
TsD	Set up time on data registers(Di or XDi)				100				ps	
ThD	Hold time on data registers (Di or XDi)				150				ps	
TsA	Set up time on addresses in (IAi)				0				ps	
ThA	Hold time on addresses in (IAi)				250				ps	
Tr,f	Output rise or fall time				150				ps	2

Notes:
1. Test conditions (unless otherwise indicated) :
VBB = -1.2V; VTT=-2.0V; VTTC=VTT; VIH=-0.7V; VIL=-1.7V; VOH≥-0.7V; VOL≤-1.7V; VDCH=VDDO; RLOAD = 50Ω to VTT. Input signal rise and fall time ≤ 150 ps
2. Rise and fall times are measured at the 20% and 80%points of the transition from Vol max to Voh min.

GigaBit Logic

10G060
10G060K

2 Stage Ripple Counter/Divider
3.0 GHz Clock Rate
10G PicoLogic™ Family

DISTINCTIVE CAPABILITIES

- 3.0 GHz (25°C min.) low power operation
- 0°C to 85°C commercial temperature range, 10G060
- -40°C to 100°C extended temp. range, 10G060K
- Ripple counting prescaler, divide by 2 and 4 outputs
- 10G PicoLogic I/O compatible
- Wire-OR output capability
- Available in flatpack, leadless chip carrier (LCC) or dice form
- Packages contain internal decoupling capacitors for optimum high frequency performance

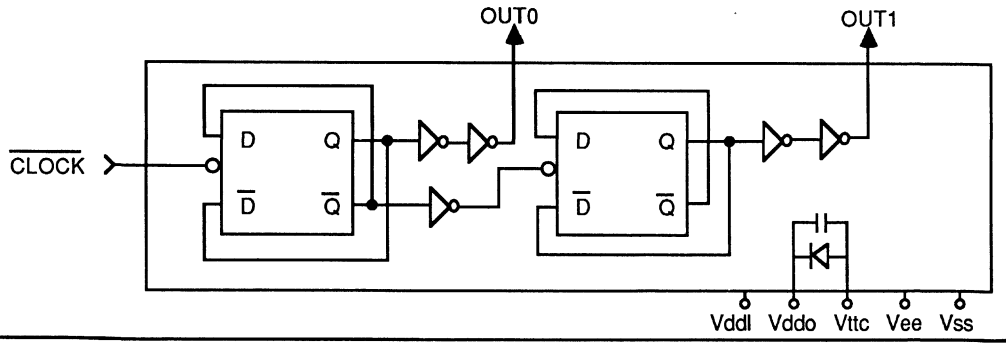
APPLICATIONS

- Frequency Synthesizer Prescaler
- Phased Locked Loops

FUNCTIONAL DESCRIPTION

The 10G060 is an ultra- fast 3.0 GHz performance two stage ripple up-counter for frequency synthesis, phased locked loop, and other applications requiring a fast, low power prescaler. The 10G060 provides both ÷2 and ÷4 outputs. The clock input is 10G PicoLogic compatible meaning that the input signal must be centered around the -1.1V input threshold level. Output levels are ECL and 10G PicoLogic compatible. The 10G060 is capable of 3 GHz operation at 25°C and typical propagation delay to the ÷2 output is 1.1 ns. The 10G060 is fabricated using GigaBit's high volume Gallium Arsenide MESFET process technology.

BLOCK DIAGRAM



10G060, 10G060K ORDERING INFORMATION

PACKAGE TYPE	SPEED				
	10G060 (0°C to 85°C)			10G060K (-40°C to 100°C)	
	2.3 GHz	2.0 GHz	1.5 GHz	2.0 GHz	1.5 GHz
36 I/O Leadless carrier	10G060-2L36	10G060-L36	10G060-3L36	10G060K-2L36	10G060K-L36
36 I/O Flatpack	10G060-2F	10G060-F	10G060-3F	10G060K-2F	10G060K-F
40 I/O Leadless carrier	10G060-2L	10G060-L	10G060-3L	10G060K-2L	10G060K-L
40I/O C- Leaded carrier	10G060-2C	10G060-C	10G060-3C	10G060K-2C	10G060K-C
Unpackaged Dice			10G060-3X		10G060K-X

FUNCTIONAL DESCRIPTION (cont.)

The counter counts up on each high-to-low transition of $\overline{\text{CLOCK}}$. The 10G060 has optional clamp inputs to provide flexibility when interfacing to other components. When connected to a supply voltage at the input threshold of -1.1V, input clamps VICH and VICL allow the 10G060 to be driven with input signals greater than 2.0Vp-p without damage to internal gates. This is particularly useful when the clock input is driven directly from a voltage controlled oscillator (VCO). When not used, input clamp VICH should be connected to VDDL (GND) and VICL to VSS (-3.4V). Logic clamps VLCH and VLCL provide a means of limiting the voltage swing of internal gates, thus increasing the performance of the divider. The recommended voltages for VLCH and VLCL are indicated with the notes for the AC characteristics. When not used the VLCH and VLCL pins may be left open.

PIN DESCRIPTIONS

$\overline{\text{CLOCK}}$	High speed clock input. Drives both stages. The falling edge of $\overline{\text{CLOCK}}$ causes the outputs to change.
OUT0-OUT1	Divide by 2, 4 outputs, respectively.
VDDO	Output driver ground (0V).
VDDL	Internal logic ground (0V).
VSS	-3.4V power supply.
VEE	-5.2V power supply.
VTTC	The AC return pin for the internal VDDO decoupling capacitor. VTTC is not brought on to the 10G060 die. VTTC is typically tied to VTT (nominally -2.0V).
VDCH	Output driver high level clamp voltage. May be used to limit VOH when driving ECL. See App. Note 4 for details. When driving other GaAs devices, VDCH should be disabled by connecting it to VDDO.
VICH, VICL	Input protection clamp voltages. When connected to -1.3V, these allow an overdriven sine wave input signal to be truncated to a square wave.
VLCH, VLCL	Logic clamp voltages. When connected as specified in the AC Characteristic Notes these pins clamp the internal logic voltage swing of the device, thus enhancing the AC performance of the part. When not used these pins may be left open.
VTRIM	Input threshold adjustment voltage. Values of VTRIM more or less negative than VEE will adjust all input thresholds around their nominal value of -1.1V. Connect to VEE when not used.

RECOMMENDED OPERATING CONDITIONS (note 3)

SYMBOL	PARAMETER	MIN	NOM	MAX	UNITS	NOTES
TC1	Case Operating Temp. (10G060)	0	25	85	°C	1
TC2	Case Operating Temp. (10G060K)	-40	25	100	°C	1
VDDL	Logic Supply Voltage		GND		V	
VDDO	Output Driver Supply Voltage	-0.8	GND	1.0	V	
VSS	Supply Voltage	-3.5	-3.4	-3.3	V	
VEE	Supply Voltage	-5.5	-5.2	-5.1	V	
VTTC	VDDO Internal Decoupling Return	VSS	VTT	VDDO	V	
VTT	Load Termination Supply Voltage	VSS	-2.0	-2.0	V	2
RLOAD	Output Termination Load Resistance	25	50	100	Ω	2
VICH	Input Clamp High Voltage	-1.8	VDDL	VDDL	V	
VICL	Input Clamp Low Voltage	VSS	VSS	-0.8	V	
VLCH	Logic Clamp High Voltage	-1.8	VDDL	VDDL	V	
VLCL	Logic Clamp Low Voltage	VSS	VSS	-0.8	V	
VDCH	Output Driver Clamp High Voltage	-2.5	VDDO	VDDO	V	4
VTRIM	Input Threshold Adjustment Voltage	VEE-1	VEE	VEE+1	V	

RECOMMENDED OPERATING CONDITIONS, cont.

NOTES

1. Tcase measured at case bottom. User attention to device thermal management is recommended. See GigaBit Application Note 3 for a complete discussion of all aspects of device thermal management.
2. The RLOAD and VTT combination used is subject to maximum output current and power restrictions.
3. See GigaBit Application Note 4 for a discussion of interfacing requirements to and from PicoLogic devices.
4. VDCH is not used when driving GaAs logic. To limit VOH when driving ECL logic, consult Application Note 4.

ABSOLUTE MAXIMUM RATINGS

(Beyond which useful life may be impaired) (Note 1)

SYMBOL	PARAMETER	ABSOLUTE MAXIMUM RATINGS	NOTES
TSTOR	Storage Temperature	- 65 °C to + 150 °C	
TJ	Junction Temperature	- 55 °C to + 150 °C	
TC	Case Temperature Under Bias	- 55 °C to + 125 °C	2
VDDO	Output Driver Supply Voltage	-0.8V to + 1.0 V	
VSS	Supply Voltage	- 4.0 V to + 0.5 V	
VEE	Supply Voltage	- 7.0 V to VSS + 0.5 V	
VIN	Voltage Applied to Any Input; Continuous VSS = - 3.4 V, VEE = - 5.2 V	- 4.0 V to + 0.5 V	
I IN	Current Into Any Input; Continuous	- 0.5 mA to 1.0 mA	
VOUT	Voltage Applied to Any Output	-4.0V to + 7.0 V	3
IOUT	Current From Any Output; Continuous	-70 mA	
PD	Power Dissipation Per Output POUT = (VDDO-VOUT) x IOUT	100 mW	3
VTTC	VDDO Internal Decoupling Cap. Return	-6.0 V to VDDO	
VTT	Load Termination Supply	-6.0 V to VDDO + 6.0 V	
VDCH	Output Driver Clamp Voltage	VSS to VDDO	4
IDCH	Output Driver Clamp Current	-20 mA	
VICH	Input Clamp High Voltage	-2.0V to VDDL	5
IICH	Input Clamp High Current	-20mA	
VICL	Input Clamp Low Voltage	VSS to - 0.4V	5
IICL	Input Clamp Low Current	20 mA	
VLCH	Logic Clamp High Voltage	-2.0V to VDDL	5
ILCH	Logic Clamp High Current	-40mA	
VLCL	Logic Clamp Low Voltage	VSS TO 0.4V	5
ILCL	Logic Clamp Low Current	-40 mA	

NOTES:
1. All voltages specified with VDDL defined as 0 V. Positive current is defined as current into the device.
2. TC is measured at case bottom.
3. Subject to IOUT and power dissipation limitations.
4. Subject to IDCH and power dissipation limitations.
5. Subject to clamp current and power dissipation limitations

USER NOTES

Unlike most PicoLogic circuits, the input threshold level of the 10G060 is not stabilized with a VBB feedback circuit. Therefore, the clock input threshold voltage will vary from its nominal -1.1V room temperature level with variation in VSS and temperature. VTRIM may be used to compensate for threshold drift. This approach is detailed in App. Note 4. Alternatively, it is necessary to drive the clock input with a large peak-to-peak signal as shown for VIH and VIL in the DC characteristics table. Under high speed conditions, the clock input should be ≥2Vp-p to achieve maximum speed as described in the notes to the AC Characteristics tables. Other PicoLogic devices can be used as a driver to provide these levels by terminating the output to VSS instead of VTT.

10G060/K DC CHARACTERISTICS (Notes1,2)

TC = -40°C to +100°C, VSS = -3.5V to -3.3V, VEE = -5.5V to -5.1V, VDDL=VDDO = 0V, unless otherwise indicated.

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	TEST CONDITIONS	NOTES
VOH	Output Voltage High	- 0.8	-0.6	-0.3	V		
VOL	Output Voltage Low	- 2.0	-1.9	- 1.8	V		
IOH	Output Current High		-70	-60	mA	VOH = -0.8V	
VIH1	Input Voltage High (60)	- 0.6		VDDL	V		4,5
VIL1	Input Voltage Low (60)	VSS		- 1.9	V		4,5
VIH2	Input Voltage High (60K)	-0.6		VDDL	V		4,5
VIL2	Input Voltage Low (60K)	VSS		-2.1	V		4,5
IIN	Input Current		200	500	uA	VIN = -0.6V to -2.1V	
ISS	Power Supply Current		60	100	mA		
IEE	Power Supply Current		6	10	mA		
PD	Power Dissipation		250	400	mW		3

Notes: 1. These characteristics are applicable from DC to 500MHz.
2. Test conditions (unless otherwise indicated) :
VTT = -2.0V VICH = VDDL VLCH = VDDL VDCH = VDDO VTRIM = VEE
VTTC = VTT VICL = VSS VLCL = VSS IOH is the available output current at VOH = -0.8V.
3. At nominal supply voltages and 50% duty cycle. Exclusive of VDDO output source follower power (typically 15 mW per output) and clamp power if any.
4. CLOCK0 input rise and fall times ≤ 2ns (measured from the 20% and 80% points).
5. Input levels are 10G PicoLogic compatible.

10G060-2 AC CHARACTERISTICS (Note 1)

VSS = -3.5V to -3.3V, VEE = -5.5V to -5.1V, VDDL=VDDO = 0V, unless otherwise indicated.

SYM-BOL	PARAMETER	Tc= 0°C		Tc = +25°C			Tc= +85°C		UNITS	NOTES
		MIN	MAX	MIN	TYP	MAX	MIN	MAX		
T1	$\overline{\text{CLOCK}}$ Max Toggle Freq.	2.3		3.0			2.3		GHz	2
T2	$\overline{\text{CLOCK}}$ Low Time	185		165			215		ps	
T3	$\overline{\text{CLOCK}}$ High Time	185		165			215		ps	
T4	$\overline{\text{CLOCK}}$ Low to OUT0		1.7		1.1	1.5		2.0	ns	
T5	$\overline{\text{CLOCK}}$ Low to OUT1		2.8		1.9	2.5		3.3	ns	
Tr	Output Rise Time				250				ps	
Tf	Output Fall Time				250				ps	

10G060 AC CHARACTERISTICS (Note 1)

VSS = -3.5V to -3.3V, VEE = -5.5V to -5.1V, VDDL=VDDO = 0V, unless otherwise indicated.

SYM-BOL	PARAMETER	Tc= 0°C		Tc = +25°C			Tc= +85°C		UNITS	NOTES
		MIN	MAX	MIN	TYP	MAX	MIN	MAX		
T1	$\overline{\text{CLOCK}}$ Max Toggle Freq.	2.0		2.5			2.0		GHz	2
T2	$\overline{\text{CLOCK}}$ Low Time	250		200			250		ps	
T3	$\overline{\text{CLOCK}}$ High Time	250		200			250		ps	
T4	$\overline{\text{CLOCK}}$ Low to OUT0		2.4		1.3	1.8		2.4	ns	
T5	$\overline{\text{CLOCK}}$ Low to OUT1		3.9		2.3	3.0		3.9	ns	

10G060 AC CHARACTERISTICS (Note 1)

VSS = -3.5V to -3.3V, VEE = -5.5V to -5.1V, VDDL=VDDO = 0V, unless otherwise indicated.

SYMBOL	PARAMETER	Tc= 0°C		Tc = +25°C			Tc= +85°C		UNITS	NOTES
		MIN	MAX	MIN	TYP	MAX	MIN	MAX		
Tr	Output Rise Time				250				ps	
Tf	Output Fall Time				250				ps	

10G060-3 AC CHARACTERISTICS (Note 1)

VSS = -3.5V to -3.3V, VEE = -5.5V to -5.1V, VDDL=VDDO = 0V, unless otherwise indicated.

SYMBOL	PARAMETER	Tc= 0°C		Tc = +25°C			Tc= +85°C		UNITS	NOTES
		MIN	MAX	MIN	TYP	MAX	MIN	MAX		
T1	$\overline{\text{CLOCK}}$ Max Toggle Freq.	1.5		2.0			1.5		GHz	2
T2	$\overline{\text{CLOCK}}$ Low Time	330		250			330		ps	
T3	$\overline{\text{CLOCK}}$ High Time	330		250			330		ps	
T4	$\overline{\text{CLOCK}}$ Low to OUT0		2.9		1.9	2.4		2.9	ns	
T5	$\overline{\text{CLOCK}}$ Low to OUT1		4.9		2.9	3.9		4.9	ns	
Tr	Output Rise Time				250				ps	
Tf	Output Fall Time				250				ps	

10G060K-2 AC CHARACTERISTICS (Note 1)

VSS = -3.5V to -3.3V, VEE = -5.5V to -5.1V, VDDL=VDDO = 0V, unless otherwise indicated.

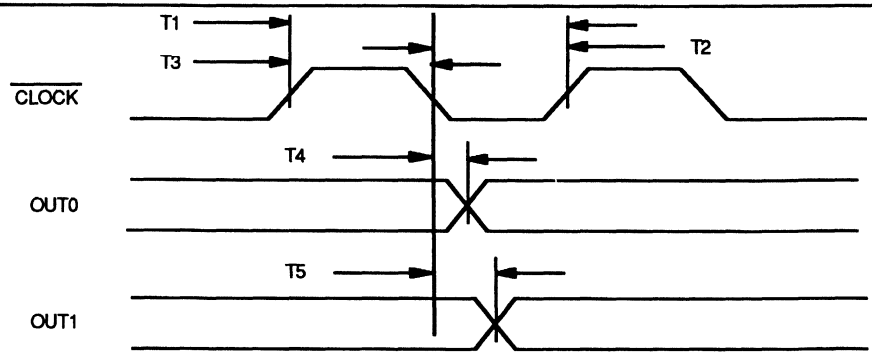
SYMBOL	PARAMETER	Tc= -40°C		Tc = +25°C			Tc= +100°C		UNITS	NOTES
		MIN	MAX	MIN	TYP	MAX	MIN	MAX		
T1	$\overline{\text{CLOCK}}$ Max Toggle Freq.	2.0		3.0			2.0		GHz	2
T2	$\overline{\text{CLOCK}}$ Low Time	250		165			250		ps	
T3	$\overline{\text{CLOCK}}$ High Time	250		165			250		ps	
T4	$\overline{\text{CLOCK}}$ Low to OUT0		2.4		1.1	1.5		2.4	ns	
T5	$\overline{\text{CLOCK}}$ Low to OUT1		3.9		1.9	2.5		3.9	ns	
Tr	Output Rise Time				250				ps	
Tf	Output Fall Time				250				ps	

10G060K AC CHARACTERISTICS (Note 1)

VSS = -3.5V to -3.3V, VEE = -5.5V to -5.1V, VDDL=VDDO = 0V, unless otherwise indicated.

SYMBOL	PARAMETER	Tc= -40°C		Tc = +25°C			Tc= +100°C		UNITS	NOTES
		MIN	MAX	MIN	TYP	MAX	MIN	MAX		
T1	$\overline{\text{CLOCK}}$ Max Toggle Freq.	1.5		2.5			1.5		GHz	2
T2	$\overline{\text{CLOCK}}$ Low Time	330		200			330		ps	
T3	$\overline{\text{CLOCK}}$ High Time	330		200			330		ps	
T4	$\overline{\text{CLOCK}}$ Low to OUT0		2.9		1.3	1.8		2.9	ns	
T5	$\overline{\text{CLOCK}}$ Low to OUT1		4.9		2.3	3.0		4.9	ns	
Tr	Output Rise Time				250				ps	
Tf	Output Fall Time				250				ps	

SWITCHING WAVEFORMS



AC CHARACTERISTICS

NOTES: 1. Test Conditions, unless otherwise stated.

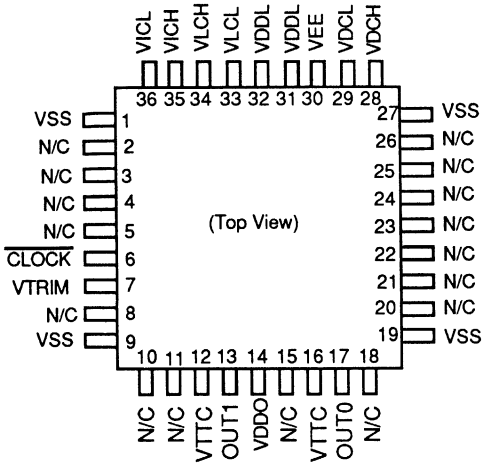
TA = 25°C
VDDL = VDDO = 0V
VEE = -5.2V
VSS = -3.4V
VICH = 0V
VICL = VSS
VLCH = -1.50V
VLCL = -1.25V
VDCH = 0V
VDCL = VSS
VTRIM = VEE
VOH ≥ -0.8V
VOL ≤ -1.8V
RLOAD = 50Ω to -2.0V

Rise and fall times are measured between 20% and 80% points.

2. Test conditions: Clock input = 2V peak -to- peak sine wave, -1.1V offset.

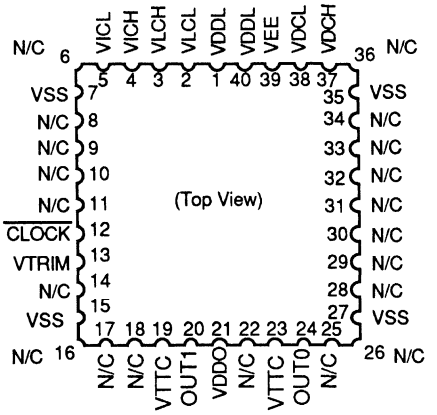
PACKAGE PINOUT DIAGRAM

36 LEAD FLATPACK
PACKAGE TYPE "F"



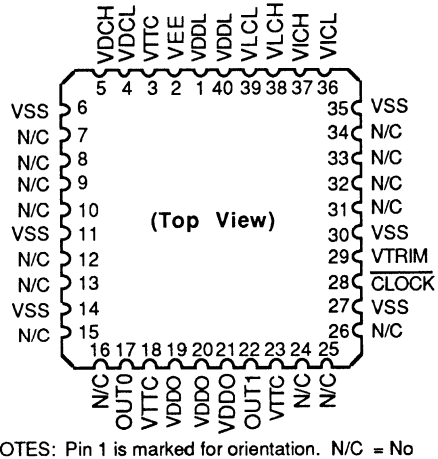
NOTES: Pin 1 is marked for orientation. N/C = No Connection. The package bottom surface is at VSS potential.

36 I/O LEADLESS CHIP CARRIER
PACKAGE TYPE "L36"



NOTES: Pin 1 is marked for orientation. N/C = No Connection. The package lid, bottom heat vias, and 4 N/C corner pins (6,16,26,36) are at Vss potential.

PIN FUNCTIONS - 40 PIN TYPE "C" AND "L" PACKAGES



NOTES: Pin 1 is marked for orientation. N/C = No connection.

4-Stage Synchronous Programmable Counter
1.3 GHz Clock Rate
10G PicoLogic™ Family

DISTINCTIVE CAPABILITIES

- Advanced carry look-ahead controls permit cascaded counting and N-bit programmable division near the maximum speed of a single counter
- Terminal Count Load Enable control automatically reloads counter after terminal count for ultra-high speed programmable division
- Synchronous Reset and parallel Load controls
- Carry Out (terminal count) complement output for easy design of self-stopping counters and
- 850 ps typical clock to output delay
- Fully synchronous rising edge-triggered operation
- ECL and PicoLogic compatible I/O
- VBB threshold reference input and on-chip VBBS threshold reference voltage output
- Available in 40 I/O C-leaded or leadless chip carriers or in dice form
- Packages contain power supply decoupling capacitors for optimum high frequency performance

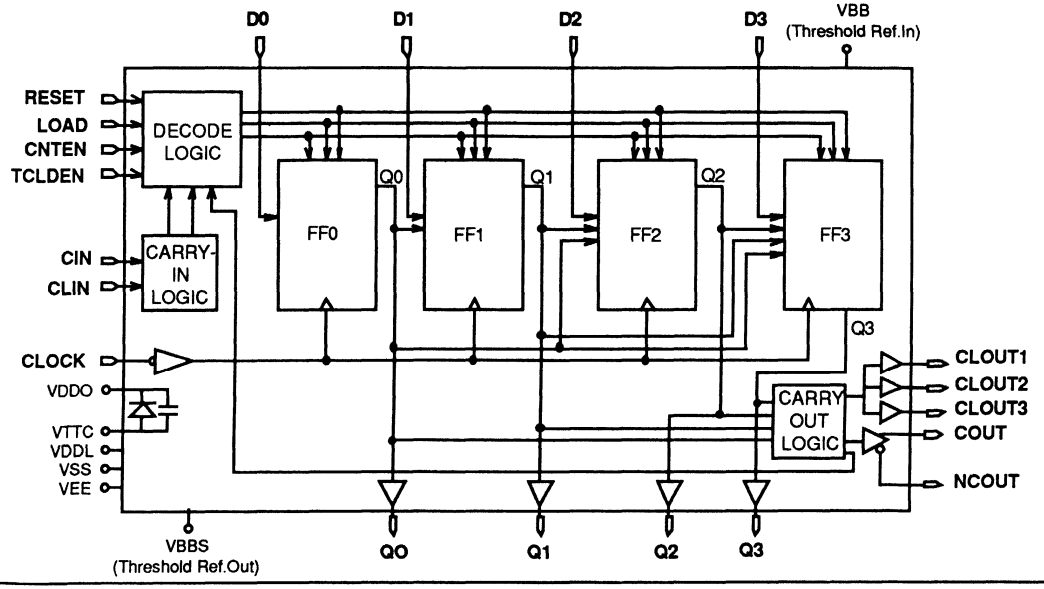
APPLICATIONS

- Ultra-high frequency N-bit programmable dividers
- Self-stopping counters
- Synthesizer prescalers
- High resolution time delay measurement
- Sequential memory address generation
- High speed synthesizer swallow counters (in combination with 10G070 Variable Modulus Divider)
- High speed state machines

10G061 ORDERING INFORMATION

PACKAGE TYPE	SPEED (MIN. 0°C to 85°C)	
	1.3 GHz	1.0 GHz
C-leaded CC	10G061-2C	10G061-3C
Leadless CC	10G061-2L	10G061-3L
Dice		10G061-3X

10G061 BLOCK DIAGRAM



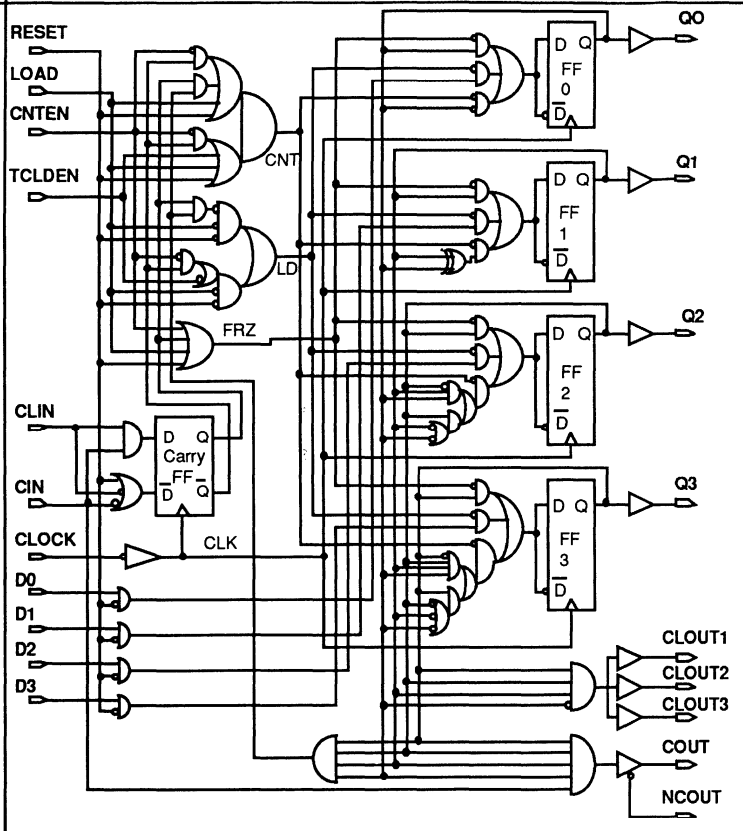
FUNCTIONAL DESCRIPTION

The 10G061 is a modulo-16 synchronous binary up-counter that can be loaded with external data for programmable counter applications. Advanced carry look-ahead and terminal count load enable features, not found on other high speed counters, have been incorporated. These features allow the user to cascade multiple 10G061s to realize N-stage counters or programmable dividers at clock frequencies in excess of a gigaHertz. Using the counter's active low terminal count output, high speed self-stopping counters and prime number dividers can be easily designed.

The 10G061 is fully synchronous, changing states on the rising edge of the clock input. Synchronous reset and load controls are provided. The device features clock to output delay of typically 850 ps and is capable of a 1.6 GHz clock rate operating as a free running counter. For compatibility with other high speed logic families, the 10G061 features the PicoLogic family standard VBB input which allows the device's input logic threshold to be controlled by the driving logic family. This way, mismatches in threshold level due to temperature and power supply variation can be tracked out, providing high system noise immunity. An on-chip -1.3V threshold voltage output (pin VBBS) is also provided. *VBBS must be strapped to the VBB input when PicoLogic is used to drive the 10G061.* See GigaBit Application Note 4, "Interfacing PicoLogic and NanoRam ICs to Other Logic Families" for more detail.

The 10G061 is a member of GigaBit's PicoLogic family of GaAs digital integrated circuits, and is fabricated using GigaBit's high volume, production proven GaAs MESFET process technology.

SIMPLIFIED LOGIC DIAGRAM



PIN DESCRIPTIONS

D0-D3	Parallel data inputs.
CLOCK	High speed buffered clock input. The rising edge of CLOCK causes the outputs to change.
CNTEN	Count enable input. When high, the counter is enabled to count up synchronously.
LOAD	The LOAD input enables parallel external data on pins D0-D3 to be synchronously loaded into the counter. LOAD has second highest priority after RESET.
TCLDEN	Terminal Count Load Enable input. When high, the external data on pins D0-D3 are synchronously loaded into the counter on the rising edge of the clock following terminal count.
RESET	When high, RESET forces all outputs (except NCOUT) low by synchronously loading all zero data. RESET overrides all other control inputs.
CIN	Carry In input. CIN is generally driven from the COUT output of a previous (less significant) counter in cascade. CIN also gates

PIN DESCRIPTIONS cont.

(AND) the COUT output. When CNTEN is low (not overriding), and if both CIN and CLIN are high, the 10G061 will be enabled to count beginning on the second clock cycle following the time at which both CIN and CLIN go high.

CLIN Carry Look-Ahead Input. CLIN is generally driven by the CLOUT output of the least significant counter in cascade.

Q0-Q3 True count outputs from counter stages 0-3 respectively.

COUT Carry Out output. COUT pulses high for one clock period when the counter reaches binary state 15 to indicate that terminal count has been reached.

NCOUT Not Carry Out output. NCOUT is the complement of COUT.

CLOUT1, CLOUT2, CLOUT3 Carry Look-Ahead Outputs 1, 2 and 3. These identical outputs, which facilitate cascading, pulse high for one clock period when the counter reaches count 14. CLOUT normally drives the CLIN input of all successively more significant counters in cascade.

VDDO Output driver ground pin (0V).

VDDL Internal logic ground connection (0V).

VSS -3.4V power supply.

VEE -5.2V power supply.

VTTC The AC return pin for the internal VDDO decoupling capacitor. VTTC is not brought onto the 10G061 circuit, and is typically tied to VTT (nominally -2.0V).

VDCH Output driver high level clamp voltage. May be used to limit VOH when driving ECL. See App. Note 4. When driving GaAs logic, VDCH should be disabled by connecting it to VDDO.

VBB Reference input to the 10G061's input threshold tracking circuit. Connect to the VBB supplied from ECL when driving the 10G061 from ECL. **Connect to the VBBS pin when the 10G061 is driven from PicoLogic.**

VBBS Threshold reference output voltage. Nominally equal to -1.3V with a 40Ω source impedance.

10G061 OPERATION

The operation of the 10G061 is described by the following function select table. Each operating mode defined in this table is discussed in detail in the paragraphs following.

10G061 FUNCTION SELECT TABLE

FUNCTION	INPUTS							OUTPUTS		
	RESET	CNTEN	Cin	Clin	TCLDEN	Load	CLK	CLOUT	COUT	Q0 - Q3
RESET After the rising edge of the clock, all outputs are low.	1	X	X	X	X	X	↓	0	0	[Q0,Q1,Q2,Q3] = Lo
LOAD After rising clock edge, data on pins D0-D3 are loaded and appear at the outputs.	0	X	X	0	X	1	↓	$\overline{Q0}$•Q1•Q2•Q3	CIN•Q0•Q1•Q2•Q3	$[Q0,Q1,Q2,Q3]_{n+1}$ = [D0,D1,D2,D3]
FREE COUNTING/÷16 Ouputs advance their binary state on each rising clock edge.	0	1	X	X	0	0	↓	$\overline{Q0}$•Q1•Q2•Q3	CIN•Q0•Q1•Q2•Q3	$[Q0,Q1,Q2,Q3]_{n+1}$ = Next binary state
CASCADED COUNTING On 2nd rising clock edge,outputs start to advance their state.	0	0	1	⎍	0	0	↓	$\overline{Q0}$•Q1•Q2•Q3	CIN•Q0•Q1•Q2•Q3	$[Q0,Q1,Q2,Q3]_{n+2}$ = Next binary state
MODULO-2/16 DIVISION Counter repetitively cycles from ext. data binary state to 1111.	0	1	1	1	1	0	↓	$\overline{Q0}$•Q1•Q2•Q3	CIN•Q0•Q1•Q2•Q3	$[Q0,Q1,Q2,Q3]_{n+1}$ = Next binary state
MODULO-N PROG. DIV. The counter begins count at 2nd clock edge and cycles from ext. data binary state to TC (1111).	0	0	1	⎍	1	0	↓	$\overline{Q0}$•Q1•Q2•Q3	CIN•Q0•Q1•Q2•Q3	$[Q0,Q1,Q2,Q3]_{n+2}$ = Next binary state
COUNT DISABLE Counter is disabled. Outputs held at previous state.	0	0	0 X	X 0	X	0	↓	$\overline{Q0}$•Q1•Q2•Q3	CIN•Q0•Q1•Q2•Q3	$[Q0,Q1,Q2,Q3]_{n+1}$ =

RESET, LOAD and Disable Functions

Regardless of the state of any other input, RESET will force all outputs low (except NCOUT), including CLOUT and COUT, at the rising edge of the clock after it is asserted high. The clock edge following the assertion of LOAD high will cause the data present on pins D0 - D3 to be parallel loaded into the counter and immediately appear at the outputs. Counting from this preloaded state will start on the next clock edge, assuming the counter is enabled to count. Among the four control inputs, the order of execution precedence is RESET, LOAD, CNTEN and TCLDEN.

The 10G061 is disabled from counting when CNTEN is low and either CIN or CLIN is also low. CIN and CLIN cannot both be high together since this condition generates an internal count enable even when CNTEN is low. This state is utilized when counters are cascaded. When disabled, the device's internal flip flop outputs are recirculated back to their inputs and the counter's outputs are maintained at their state prior to the disable action.

Free and Cascaded Counting Operation

These operating modes do not use the terminal count load enable feature (TCLDEN).

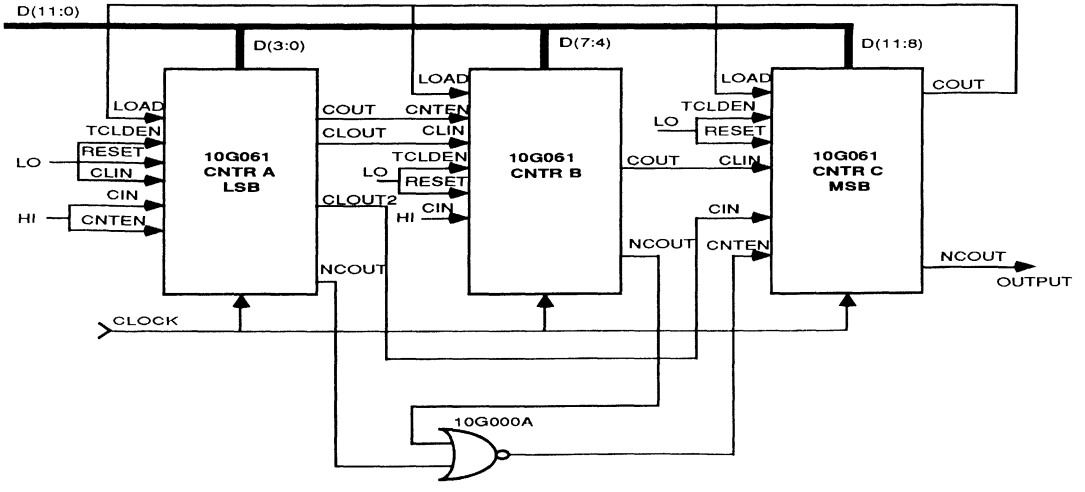
As a stand alone free-running ÷16 counter, the 10G061 operates at its fastest. In this mode, CNTEN is held high and TCLDEN is held low. The counter advances its binary state on each rising clock edge.

There are two distinct ways to cascade 10G061s to form N-bit counter chains. The first method is termed ripple carry; the second, look-ahead carry where the 10G061's advanced carry look-ahead circuitry is utilized. Counter chains which utilize look-ahead carry operate approximately twice as fast as they would if wired for ripple carry operation.

Ripple carry operation obtains its name from the fact that the terminal count signal (COUT) must ripple propagate from one stage to the next as it is generated. The clock rate capability of this arrangement is limited by the time required for the COUT pulse from the first (least significant) stage to ripple through to the CIN input of the last (most significant) stage.

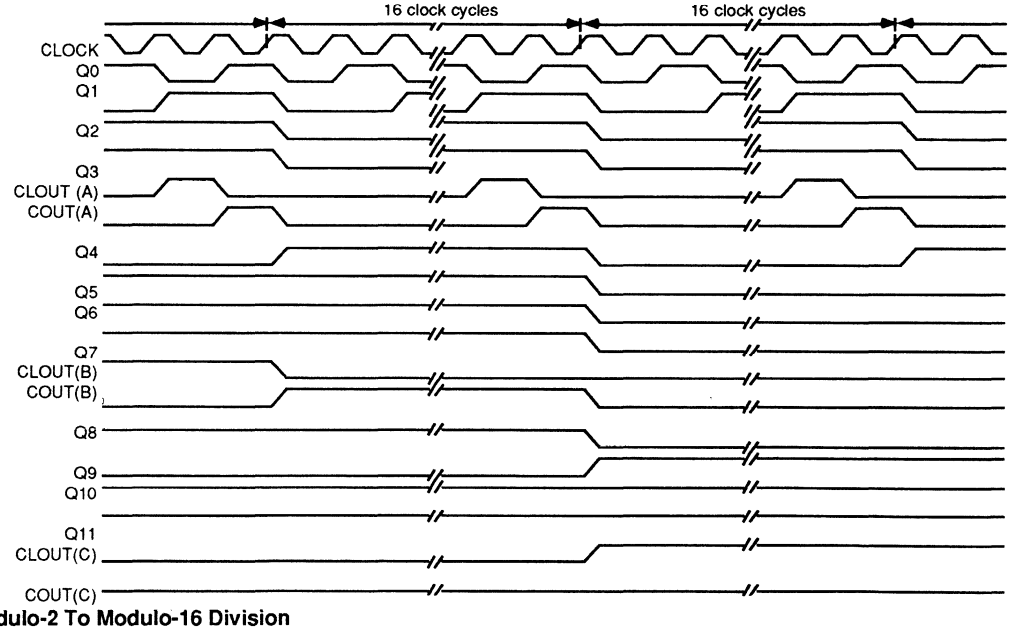
All applications should cascade 10G061's using the carry look-ahead controls, even at low operating speeds. The connection diagram for look-ahead carry operation of a 12-bit counter chain is shown below. Timing waveforms that describe this operation are given on the following page.

12-Bit Programmable Divider Using Look-ahead Carry Operation



In this mode, CLOUT1,2,3 outputs of the least significant stage drive the CLIN inputs of the second stage. CLOUT1 is a pulse equal to one clock period in width and is generated at count 14, one period prior to terminal count. At the next clock edge, which now corresponds to terminal count, the trailing edge of CLIN is ANDed with CIN and if both are high, the resulting signal is clocked through an internal flip flop and used to generate an internal count enable (see logic diagram, pg. 2). Only those stages that have already reached terminal count will enable the next stage to gate the CLIN pulse to set the flip flop output via the connection of COUT (high at terminal count only) to CIN of the next stage. At the next rising clock edge, the count enable resulting from the assertion of both CIN and CLIN high together advances the state of affected counters by one count. In this way, the terminal count from less significant counters is generated simultaneously inside the higher order counters thus eliminating the need to ripple propagate critical terminal counts from stage to stage. Using carry look-ahead, the maximum counting rate of an N-bit cascaded counter chain is nearly as fast as it is for a single counter. If a 16-bit counter is built, CLOUT3 should be used to drive the CLIN input of the added fourth stage. This stage is connected the same way as stage 3 in the drawing above. Wider counter chains should daisy-chain connect from the nearest CLOUT line to the added counter's CLIN input with the provision that the loading on each of the three CLOUT outputs be matched as much as possible. The clock and CLOUT to CLIN board delays from the least significant counter to each of the higher order counters should be designed to be approximately equal to one another.

Look-ahead Carry Waveforms

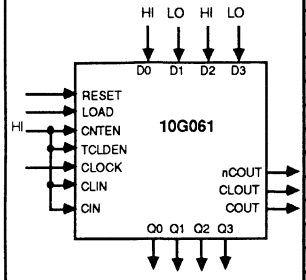


Modulo-2 To Modulo-16 Division

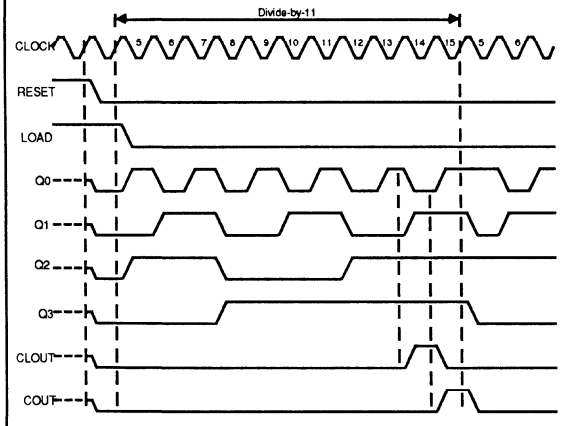
The 10G061's terminal count load enable control (TCLDEN) is utilized to configure the counter as a very high speed programmable divider. When TCLDEN, CNTEN, CIN and CLIN are all high, the 10G061 is enabled to count up and the outputs advance their binary state. When the counter reaches terminal count (1111), the data on pins D0...D3 are parallel loaded on the next rising clock edge and the counting cycle repeats. Unlike other counters, the 10G061's TCLDEN feature internally senses terminal count and generates a load enable. Keeping this feedback path on the circuit itself helps to account for the device's very high operating speed in this mode.

A single 10G061 can divide by any number between 2 and 16 inclusive. The connection diagram, timing waveforms and programming table for an example modulo-11 counter are shown on the next page. Input pins D0...D3 are set to the binary equivalent of (16 - N), i.e. the 2's complement, where N is the desired division ratio.

Mod2 - Mod16 Divider Operation & Programming



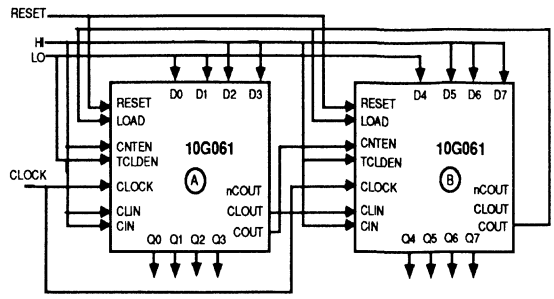
Divide Ratio	External Data Input D3	D2	D1	D0
2	H	H	H	L
3	H	H	L	H
4	H	H	L	L
5	H	L	H	H
6	H	L	H	L
7	H	L	L	H
8	H	L	L	L
9	L	H	H	H
10	L	H	H	L
11	L	H	L	H
12	L	H	L	L
13	L	L	H	H
14	L	L	H	L
15	L	L	L	H
16	L	L	L	L



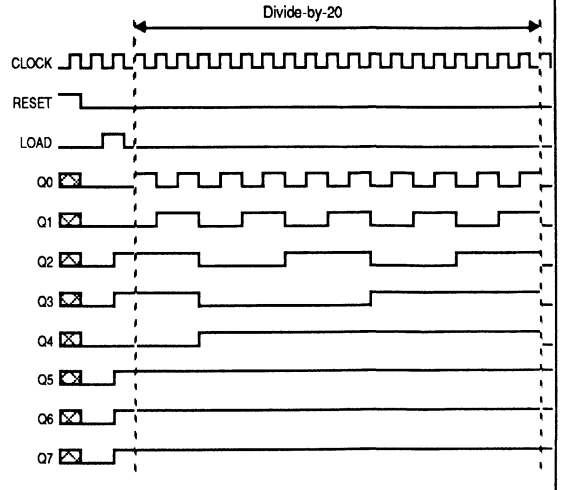
Modulo-N Programmable Division

With CLOUT(A) driving CLIN(B) and COUT(A) driving CNTEN(B) N-Bit programmable dividers capable of very high speed operation can be designed. This mode of operation is similar to that described previously for N-BIT counting except that TCLDEN of the most significant stage is wired high and the lower stages are loaded with the COUT of the most significant stage driving the LOAD inputs. Any division ratio may be formed for numbers that require programming a count (factor) greater than 16. The connection diagram, timing waveforms and programming table for an example Modulo-20 counter are shown. The counters are programmed with the binary equivalent of (256-N) where N is the desired count or factor. See App. Note 6 for more details on the design and operation of Modulo-N programmable dividers.

Modulo-N Operation & Programming



Divide Ratio	External Data Input D7	D6	D5	D4	D3	D2	D1	D0
17	H	H	H	L	H	H	H	H
18	H	H	H	L	H	H	H	L
19	H	H	H	L	H	H	L	H
20	H	H	H	L	H	H	L	L
• • •					• • •			
256	L	L	L	L	L	L	L	L

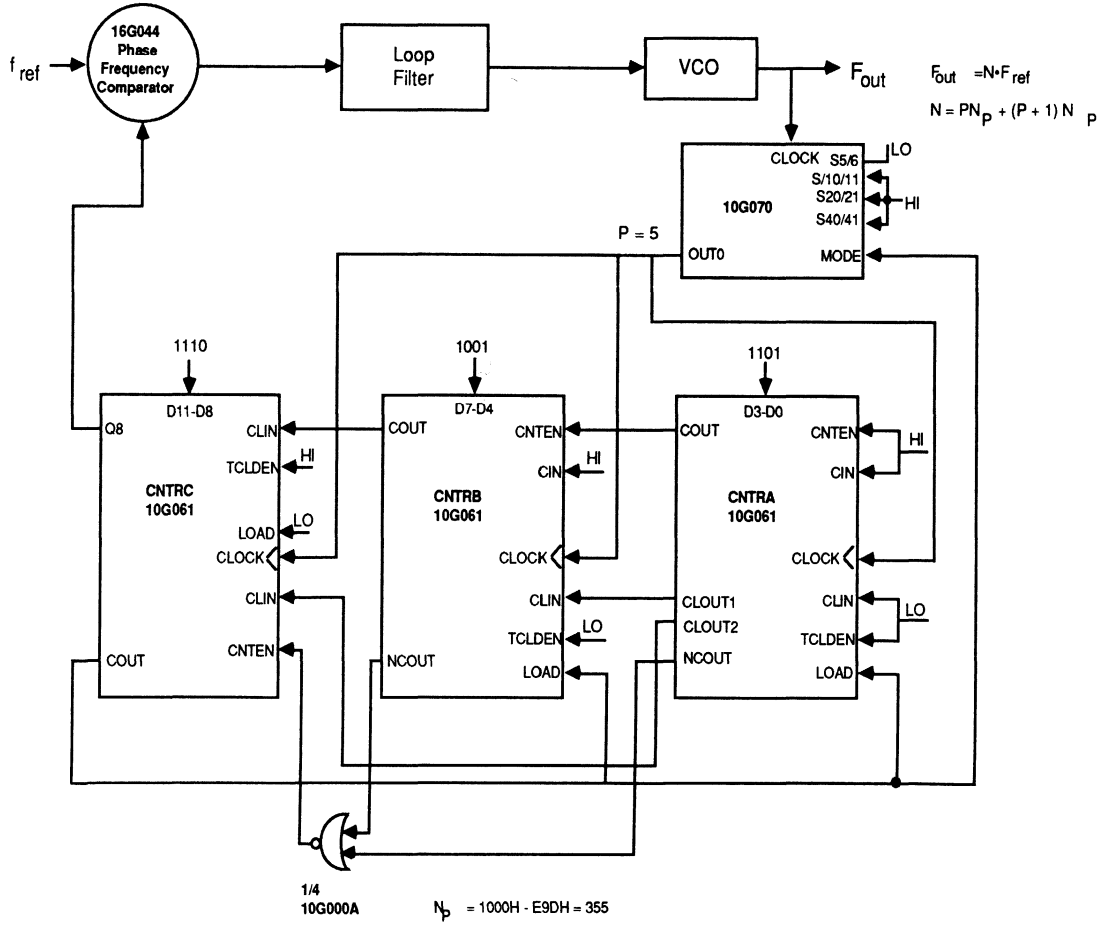


Application in Frequency Synthesizers

The 10G061, in combination with GigaBit's 10G070 Variable Modulus Divider, provides the components necessary to design very high speed (2 GHz) programmable counters for application in synthesizer phase locked loops using the pulse swallowing, or swallow counter technique. This technique uses programmable counters to toggle the mode control of the 10G070 between modulus A and A+1 to allow switching among a large number of synthesizer output frequencies. In the example below, three 10G061's are cascaded to form a 12 bit synchronous ÷355 counter. The 10G070 Variable Modulus Divider is set up to divide by 5 or 6 resulting in an overall divide ratio of 3905.

The counter loop starts out with the 10G070 dividing by 6. After 6 X 355 clock cycles, the 12 bit synchronous counter reaches terminal count and its NOR gate output triggers two actions: 1) Loads the synchronous counters with the data present on the D11 to D0 pins; 2) Changes the 10G070 mode to divide by 5. After 5 X 355 clock cycles the process repeats.

Frequency Synthesizer Swallow Counter Design Using 10G061, 10G070 and 16G044



DC CHARACTERISTICS

Tc = 0°C to 85 °C, VSS = -3.5V to -3.3V, VEE = -5.5V to -5.1V, VDDL=VDDO = Gnd, unless otherwise indicated.

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	TEST CONDITIONS	NOTES
ISS	Power Supply Current		390	500	mA		
IEE	Power Supply Current		65	105	mA		
PD	Power Dissipation		1.7	2.3	W		

NOTE:

The remaining DC Characteristics are specified in the 10G PicoLogic Family Electrical Characteristics section. This table notes parameter deviations to Family Characteristics and provides device specific supplementary characteristics only.

AC CHARACTERISTICS (Note 1)

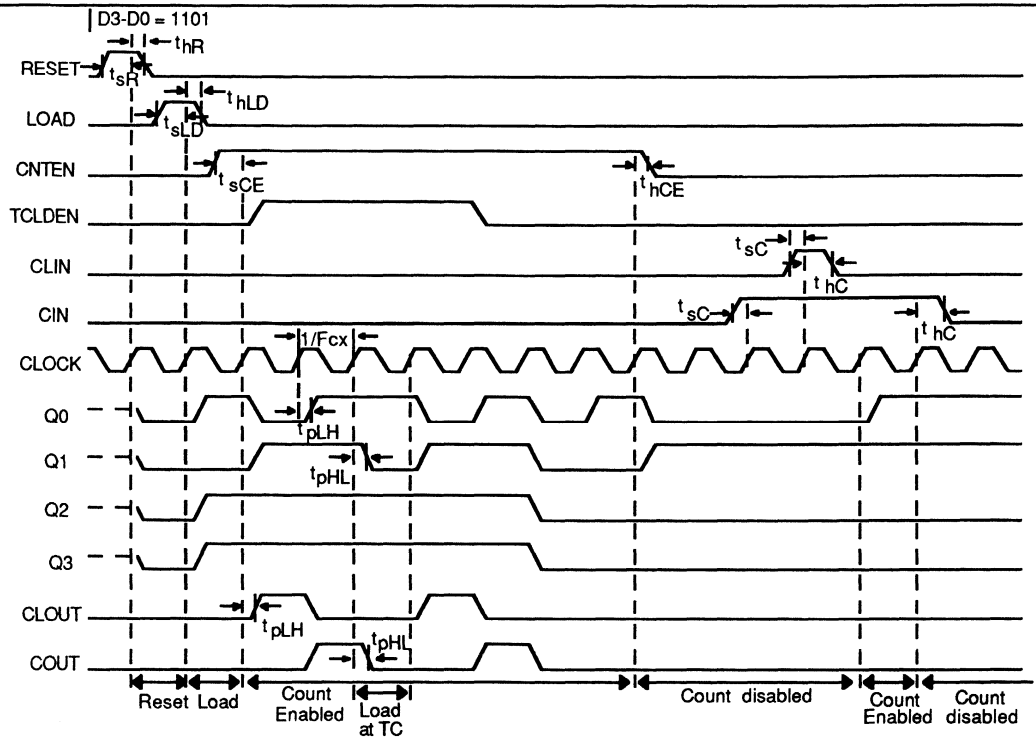
VSS = -3.5V to -3.3V, VEE = -5.5V to -5.1V, VDDL=VDDO = 0V, unless otherwise indicated.

Symbol	PARAMETER	10G061-2							10G061-3							Unit
		Tc = 0°C		Tc = 25°C			Tc = 85°C		Tc = 0°C		Tc = 25°C			Tc=85°C		
		Min	Max	Min	Typ	Max	Min	Max	Min	Max	Min	Typ	Max	Min	Max	
Fc1	Clock freq., unit counter	1.3		1.3	1.6		1.3		1.0		1.0	1.2		1.0		GHz
Fc2	Clock freq., unit divider	1.0		1.0	1.2		1.0		1.0		1.0	1.1		1.0		GHz
Fc3	Clock freq., cascaded counter				1.1							1.1				GHz
Fc4	Clock freq., cascaded divider				1.1							1.1				GHz
TsD	Setup time, data inputs	250			150		250		250			150		250		ps
ThD	Hold time, data inputs	150			100		150		150			100		150		ps
TsR	Setup time, RESET input	150			50		150		150			50		150		ps
ThR	Hold time, RESET input	100			0		100		100			0		100		ps
TsLD	Setup time, LOAD input	200			100		200		200			100		200		ps
ThLD	Hold time, LOAD input	100			0		100		100			0		100		ps
TsCE	Setup time, CNTEN input	300			200		300		300			200		300		ps
ThCE	Hold time, CNTEN input	100			0		100		100			0		100		ps
TsC	Setup time, CIN, CLIN inputs	350			250		350		350			250		350		ps
ThC	Hold time, CIN, CLIN inputs	100			0		100		100			0		100		ps
TpLH	Prop. delay, clock to output L-H	700	1200	700	850	1100	700	1200	700	1300	700	1000	1200	700	1300	ps
TpHL	Prop. delay, clock to output H-L	700	1200	700	850	1100	700	1200	700	1300	700	1000	1200	700	1300	ps
Tr	Output rise time (note 2)		200		200			200		200		200			200	ps
Tf	Output fall time (note 2)		150		150			150		150		150			150	ps
Tdc	Prop. delay, Cin to Cout	300	550				300	600	300	600				300	600	ps

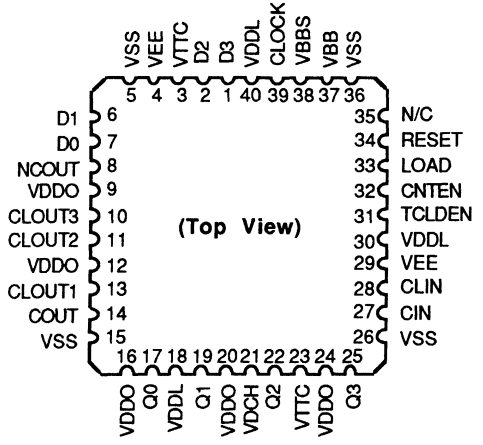
Notes: 1. Test conditions unless otherwise noted: VBB = -1.2V, VTT = -2.0V, VTTC = VTT, RLOAD = 50Ω to -2.0V, VDCH = VDDO, VIH = -0.7V, VIL = -1.7V, VOH ≥ -0.7V, VOL ≤ -1.7V. Input signal rise and fall times ≤ 200 ps.

2. Rise and fall times are measured at the 20% and 80% points of the transition from VOL max. to VOH min.

SWITCHING WAVEFORMS SUMMARY



PIN FUNCTIONS - TYPE "C" AND "L" PACKAGES



NOTES: Pin 1 is marked for orientation. N/C = No connection.

7 Stage Ripple Counter/Divider
3.0 GHz Clock Rate
10G PicoLogic™ Family

DISTINCTIVE CAPABILITIES

- 3.0 GHz operation (25°C min.)
- 0°C to 85°C commercial temperature range, 10G065
- -40°C to 100°C extended temp. range, 10G065K
- Ripple counting prescaler, divide by 2, 4, 8, 16, 32, 64, and 128
- Ripple up counter with asynchronous clear and clock enable on last six stages
- 10G PicoLogic I/O compatible
- Wire-OR output capability
- Available in flatpack, leadless chip carrier (LCC) or dice form
- Packages contain internal decoupling capacitors for optimum high frequency performance

APPLICATIONS

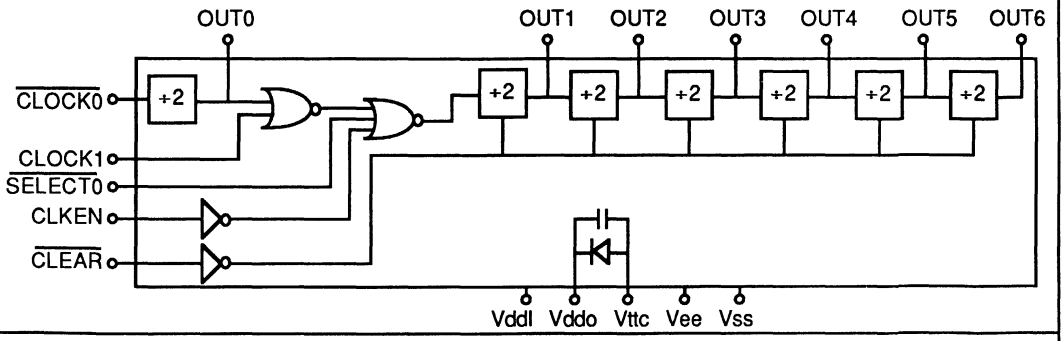
- Frequency Synthesis
- Phased Locked Loops
- Time Interval and Event Counting
- Up Counting

FUNCTIONAL DESCRIPTION

The 10G065 is an ultra- fast 3.0 GHz performance seven stage ripple up counter for frequency synthesis, phased locked loop, counting and time interval measurement applications.The device has two modes of operation; one with all seven stages driven from $\overline{\text{CLOCK0}}$, and another with the last six stages driven from a gated CLOCK1.

For seven stage operation, the $\overline{\text{SELECT0}}$ pin is strapped to VEE (-5.2V), selecting $\overline{\text{CLOCK0}}$ as the clock source. The counter counts up on each high-to-low transition of CLOCK0. This mode permits the fastest clocking rate. For six stage operation, the $\overline{\text{SELECT0}}$ pin is strapped to VSS (-3.4V), selecting CLOCK1 as the clock source.

BLOCK DIAGRAM



10G065, 10G065K ORDERING INFORMATION

PACKAGE TYPE	SPEED				
	10G065 (0°C to 85°C)			10G065K (-40°C to 100°C)	
	2.3 GHz	2.0 GHz	1.5 GHz	2.0 GHz	1.5 GHz
36 I/O Leadless carrier	10G065-2L36	10G065-L36	10G065-3L36	10G065K-2L36	10G065K-L36
36 I/O Flatpack	10G065-2F	10G065-F	10G065-3F	10G065K-2F	10G065K-F
40 I/O Leadless carrier	10G065-2L	10G065-L	10G065-3L	10G065K-2L	10G065K-L
40 I/O C - Leaded carrier	10G065-2C	10G065-C	10G065-3C	10G065K-2C	10G065K-C
Unpackaged Dice			10G065-3X		10G065K-X

FUNCTIONAL DESCRIPTION (cont.)

The counter counts up on each low-to-high transition of CLOCK1. A synchronous clock enable, CLKEN, allows CLOCK1 to be gated for counting applications. When CLKEN is high the device will count. When CLKEN is low the device will be inhibited from counting.

In both modes of operation, the asynchronous $\overline{\text{CLEAR}}$ input can be driven low to reset the last six stages of the counter. Because the first stage of the counter is optimized for speed in the seven stage operating mode it does not have a reset capability.

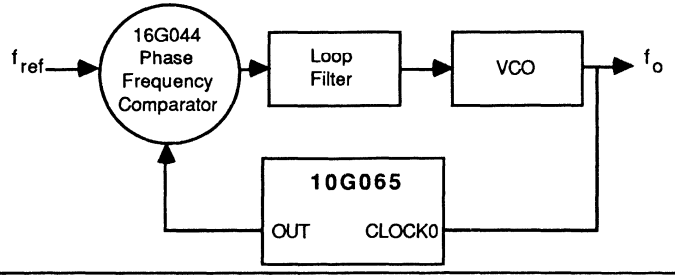
The 10G065 has optional clamp inputs to provide flexibility when interfacing to other components. When connected to a supply voltage at the input threshold of -1.3V, input clamps VICH and VICL allow the 10G065 to be driven with input signals greater than 2.0V p-p without damage to internal gates. This is particularly useful when either 10G065 clock input is driven directly from a voltage controlled oscillator (VCO). When not used, input clamp VICH should be connected to VDDL (GND) and VICL to VSS (-3.4V). Logic clamps VLCH and VLCL provide a means of limiting the voltage swing of internal gates, thus increasing the performance of the divider. The recommended voltages for VLCH and VLCL are indicated with the notes for the AC characteristics specifications. When not used the VLCH and VLCL pins may be left open. The output driver high level clamp, VDCH, may be used to limit VOH when driving ECL. See App. Note 4 for details. When driving GaAs devices, VDCH is typically connected to VDDO.

PIN DESCRIPTIONS

$\overline{\text{CLOCK0}}$	High speed clock input. Drives all seven stages. The falling edge of $\overline{\text{CLOCK0}}$ causes the outputs to change.
CLOCK1	High speed clock input. Drives last six stages. The rising edge of CLOCK1 causes the outputs to change.
$\overline{\text{SELECT0}}$	Selects the mode of operation. For seven stage operation $\overline{\text{SELECT0}}$ is tied to VEE (-5.2V). For six stage operation $\overline{\text{SELECT0}}$ is tied to VSS (-3.4V).
CLKEN	Synchronous clock enable gates the CLOCK1 input to the last six stages. When CLKEN is high the device will count. When CLKEN is low the device will be inhibited from counting.
$\overline{\text{CLEAR}}$	$\overline{\text{CLEAR}}$ is an asynchronous clear function for the last six stages. When driven low it resets the last six stages of the counter to zero.
OUT0-OUT6	Divide by 2, 4, 8, 16, 32, 64, and 128 outputs, respectively.
VDDO	Output driver ground (0V).
VDDL	Internal logic ground (0V).
VSS	-3.4V power supply.
VEE	-5.2V power supply.
VTRIM	Input threshold adjustment voltage. Values of VTRIM more or less negative than VEE will adjust all input thresholds around their nominal value of -1.3V. Connect to VEE when not used.
VTTC	The AC return pin for the internal VDDO decoupling capacitor. VTTC is not brought into the 10G065 die. VTTC is typically tied to VTT (nominally -2.0V).
VDCH	Output driver high level clamp voltage. When driving other GaAs devices, VDCH should be disabled by connecting it to VDDO.
VICH, VICL	Input protection clamp voltages. When connected to -1.3V, these allow an overdriven sine wave input signal to be truncated to a square wave, thus providing faster rise and fall times at either clock input.
VLCH, VLCL	Logic clamp voltages. When connected as specified in the AC Characteristic Notes these pins clamp the internal logic voltage swing of the device, thus enhancing the AC performance of the part. When not used these pins may be left open.

Frequency Synthesis Applications

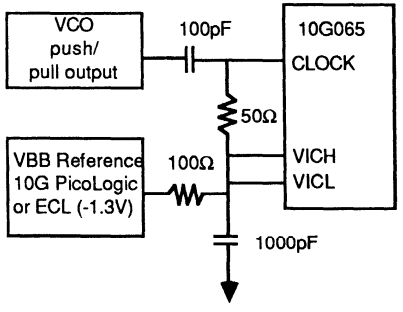
The 10G065 provides the necessary prescaler divider function for phase locked loop frequency synthesis applications. A typical frequency synthesizer block diagram including the 10G065 is shown below.



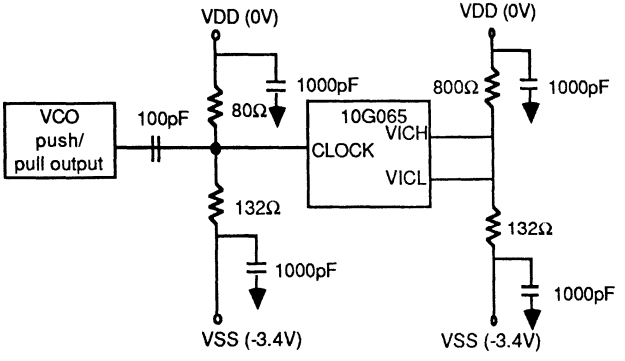
VOLTAGE CONTROLLED OSCILLATOR (VCO) INTERFACE

The CLOCK pin of the 10G065 has an input threshold of -1.3V. To interface the device to a general purpose VCO an AC coupling network is recommended. There are two common cases; one in which the threshold reference voltage (PicoLogic VBBS or ECL VBB output) is available, and another when this voltage is not availble.

VCO Interface to 10G065 With VBB Reference



VCO Interface to 10G065 Without VBB Reference



Unlike most PicoLogic circuits, the input threshold of the 10G065 is not stabilized with a VBB feedback circuit. Therefore, the threshold of all inputs will vary from their nominal -1.3V room temperature level with variations in VSS and temperature. VTRIM may be used to compensate for threshold drift. This approach is detailed in App. Note 4. Alternatively, it is necessary to drive each used input with a large peak-to-peak level signals as shown for VIH and VIL in the DC Characteristics table. Under high speed conditions, the clock input should be ≥2Vp-p to achieve maximum speed as decribed in the notes to the AC Characteristics tables. Other PicoLogic devices can be used as drivers to provide these levels by terminating driver outputs to VSS instead of VTT.

DESIGN HINTS - TTL OUTPUT LEVELS

The VDDO supply, normally at ground, is the current source for all seven 10G065 output source- follower driver FETs. APP. Note 4, Fig. 5A recommends that VDDO be biased to -0.5V, when driving a small (100Ω) pull -up load for fast rise time TTL/CMOS output levels, with a 200Ω current limiting resistor between VDDO and ground. For best performance, this 200Ω resistor must be changed to 18Ω.

ABSOLUTE MAXIMUM RATINGS

(Beyond which useful life may be impaired) (Note 1)

SYMBOL	PARAMETER	ABSOLUTE MAXIMUM RATINGS	NOTES
TSTOR	Storage Temperature	- 65 °C to + 150 °C	
TJ	Junction Temperature	- 55 °C to + 150 °C	
TC	Case Temperature Under Bias	- 55 °C to + 125 °C	2
VDDO	Output Driver Supply Voltage	-0.8V to + 1.0 V	
VSS	Supply Voltage	- 4.0 V to + 0.5 V	
VEE	Supply Voltage	- 7.0 V to VSS + 0.5 V	
VIN	Voltage Applied to Any Input; Continuous VSS = - 3.4 V, VEE = - 5.2 V	- 4.0 V to + 0.5 V	
I IN	Current Into Any Input; Continuous	- 0.5 mA to 1.0 mA	
VOUT	Voltage Applied to Any Output	-4.0V to + 7.0 V	3
IOUT	Current From Any Output; Continuous	-70 mA	
PD	Power Dissipation Per Output POUT = (VDDO-VOUT) x IOUT	100 mW	3
VTTC	VDDO Internal Decoupling Cap. Return	-6.0 V to VDDO	
VTT	Load Termination Supply	-6.0 V to VDDO + 6.0 V	
VDCH	Output Driver Clamp Voltage	VSS to VDDO	4
IDCH	Output Driver Clamp Current	-20 mA	
VICH	Input Clamp High Voltage	-2.0V to VDDL	5
IICH	Input Clamp High Current	-20mA	
VICL	Input Clamp Low Voltage	VSS to -0.4V	5
IICL	Input Clamp Low Current	20 mA	
VLCH	Logic Clamp High Voltage	-2.0V to VDDL	5
ILCH	Logic Clamp High Current	-40mA	
VLCL	Logic Clamp Low Voltage	VSS TO 0.4V	5
ILCL	Logic Clamp Low Current	-40 mA	

Notes:
1. All voltages specified with VDDL defined as 0 V. Positive current is defined as current into the device.
2. TC is measured at case bottom.
3. Subject to IOUT and power dissipation limitations.
4. Subject to IDCH and power dissipation limitations.
5. Subject to clamp current and power dissipation limitations

RECOMMENDED OPERATING CONDITIONS (note 3)

SYMBOL	PARAMETER	MIN	NOM	MAX	UNITS	NOTES
TC1	Case Operating Temp. (10G065)	0	25	85	℃	1
TC2	Case Operating Temp. (10G065K)	-40	25	100	℃	1
VDDL	Logic Supply Voltage		GND		V	
VDDO	Output Driver Supply Voltage	-0.8	GND	1.0	V	
VSS	Supply Voltage	- 3.5	- 3.4	- 3.3	V	
VEE	Supply Voltage	- 5.5	- 5.2	- 5.1	V	
VTTC	VDDO Internal Decoupling Return	VSS	VTT	VDDO	V	
VTT	Load Termination Supply Voltage	VSS	- 2.0	- 2.0	V	2
RLOAD	Output Termination Load Resistance	25	50	100	Ω	2
VICH	Input Clamp High Voltage	-1.8	VDDL	VDDL	V	
VICL	Input Clamp Low Voltage	VSS	VSS	-0.8	V	
VLCH	Logic Clamp High Voltage	-1.8	VDDL	VDDL	V	
VLCL	Logic Clamp Low Voltage	VSS	VSS	-0.8	V	
VDCH	Output Driver Clamp High Voltage	-2.5	VDDO	VDDO	V	4
VTRIM	Input Threshold Adjust Voltage	VEE-1	VEE	VEE+1	V	

RECOMMENDED OPERATING CONDITIONS, cont.

NOTES

1. Tcase measured at case bottom. User attention to device thermal management is recommended. See GigaBit Application Note 3 for a complete discussion of all aspects of device thermal management.
2. The RLOAD and VTT combination used is subject to maximum output current and power restrictions.
3. See GigaBit Application Note 4 for a discussion of interfacing requirements to and from PicoLogic devices.
4. VDCH is not used when driving GaAs logic. To limit VOH when driving ECL logic, consult Application Note 4.

10G065/K DC CHARACTERISTICS (Notes1,2)

TC = -40°C to +100°C,VSS = -3.5V to -3.3V, VEE = -5.5V to -5.1V, VDDL=VDDO = 0V, unless otherwise indicated.

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	TEST CONDITIONS	NOTES
VOH	Output Voltage High	- 0.8	-0.6	-0.3	V		
VOL	Output Voltage Low	- 2.0	-1.9	- 1.8	V		
IOH	Output Current High		-70	-60	mA	VOH = -0.8V	
VIH1	Input Voltage High (65)	- 0.6		VDDL	V		4,5
VIL1	Input Voltage Low (65)	VSS		- 1.9	V		4,5
VIH2	Input Voltage High (65K)	-0.6		VDDL	V		4,5
VIL2	Input Voltage Low (65K)	VSS		-2.1	V		4,5
IIN	Input Current		200	500	uA	VIN = -0.7V to -1.9V	
ISS	Power Supply Current		110	200	mA		
IEE	Power Supply Current		18	25	mA		
PD	Power Dissipation		500	850	mW		3

Notes: 1. These characteristics are applicable from DC to 500MHz.

2.Test conditions (unless otherwise indicated) :

VTT = -2.0V VICH = VDDL VLCH = VDDL VDCH = VDDO VTRIM = VEE

VTTC = VTT VICL = VSS VLCL = VSS IOH is the available output current at VOH = -0.8V.

3. At nominal supply voltages and 50% duty cycle. Exclusive of VDDO output source follower power (typically 15 mW per output) and clamp power if any.
4. CLOCK0 and CLOCK1 input rise and fall times ≤ 2ns (measured from the 20% and 80% points).
5. Input levels are 10G PicoLogic level compatible.

PHASE NOISE

	OFFSET (Hz)	RAW L(f)	CORRECTED dBc/Hz
OUT1 (÷4)	1K	-111.0	-99.0
	2.5K	-118.3	-106.3
	5.0K	-124.4	-112.4
	7.5K	-127.6	-115.6
	10.0K	-129.5	-117.5
	15.0K	-135.0	-123.0
	20.0K	-136.0	-124.0
	25.0K	-137.8	-125.0

NOTES:

1. Fin = 800MHz.
2. Noise Floor = -160dBc/Hz.
3. Correction is 12dBc/Hz to reference to input.

10G065-2 AC CHARACTERISTICS (Note 1)

VSS = -3.5V to -3.3V, VEE = -5.5V to -5.1V, VDDL=VDDO = 0V, unless otherwise indicated.

SYMBOL	PARAMETER	Tc= 0°C		Tc = +25°C			Tc= +85°C		UNITS	NOTES
		MIN	MAX	MIN	TYP	MAX	MIN	MAX		
T1	$\overline{\text{CLOCK0}}$ Max Toggle Freq.	2.3		3.0			2.3		GHz	2, 3
T2	$\overline{\text{CLOCK0}}$ Low Time	185		165			215		ps	2, 3
T3	$\overline{\text{CLOCK0}}$ High Time	185		165			215		ps	2,3
T4	$\overline{\text{CLOCK0}}$ Low to OUT0		1.7		1.1	1.5		2.0	ns	
T5	$\overline{\text{CLOCK0}}$ Low to OUT1		2.8		1.9	2.5		3.3	ns	
T6	$\overline{\text{CLOCK0}}$ Low to OUT2		3.9		2.6	3.5		4.6	ns	
T7	$\overline{\text{CLOCK0}}$ Low to OUT3		4.8		3.2	4.3		5.6	ns	
T8	$\overline{\text{CLOCK0}}$ Low to OUT4		5.7		3.8	5.1		6.6	ns	
T9	$\overline{\text{CLOCK0}}$ Low to OUT5		6.6		4.4	5.9		7.7	ns	
T10	$\overline{\text{CLOCK0}}$ Low to OUT6		7.5		5.0	6.7		8.7	ns	
T11	CLOCK1 Max Toggle Freq.	2.1		2.4			1.8		GHz	2, 3
T12	CLOCK1 Low Time	225		200			260		ps	2, 3
T13	CLOCK1 High Time	225		200			260		ps	2, 3
T14	CLOCK1 High to OUT1		1.7		1.1	1.5		2.0	ns	
T15	CLOCK1 High to OUT2		2.8		1.9	2.5		3.3	ns	
T16	CLOCK1 High to OUT3		3.9		2.6	3.5		4.6	ns	
T17	CLOCK1 High to OUT4		4.8		3.2	4.3		5.6	ns	
T18	CLOCK1 High to OUT5		5.7		3.8	5.1		6.6	ns	
T19	CLOCK1 High to OUT6		6.6		4.4	5.9		7.7	ns	
T20	$\overline{\text{CLEAR}}$ Setup Time				160				ps	
T21	$\overline{\text{CLEAR}}$ Hold Time				160				ps	
T22	$\overline{\text{CLEAR}}$ Pulse Width				550				ps	
T23	$\overline{\text{CLEAR}}$ High to OUT1-6 Low				700				ps	
T24	CLKEN Setup Time				110				ps	
T25	CLKEN Hold Time				110				ps	
Tr	Output Rise Time				500				ps	4
Tf	Output Fall Time				250				ps	4

10G065 AC CHARACTERISTICS (Note 1)

VSS = -3.5V to -3.3V, VEE = -5.5V to -5.1V, VDDL=VDDO = 0V, unless otherwise indicated.

SYMBOL	PARAMETER	Tc= 0°C		Tc = +25°C			Tc= +85°C		UNITS	NOTES
		MIN	MAX	MIN	TYP	MAX	MIN	MAX		
T1	$\overline{\text{CLOCK0}}$ Max Toggle Freq.	2.0		2.5			2.0		GHz	2, 3
T2	$\overline{\text{CLOCK0}}$ Low Time	250		200			250		ps	2, 3
T3	$\overline{\text{CLOCK0}}$ High Time	250		200			250		ps	2, 3
T4	$\overline{\text{CLOCK0}}$ Low to OUT0		2.4		1.3	1.8		2.4	ns	
T5	$\overline{\text{CLOCK0}}$ Low to OUT1		3.9		2.3	3.0		3.9	ns	
T6	$\overline{\text{CLOCK0}}$ Low to OUT2		5.4		3.1	4.2		5.4	ns	
T7	$\overline{\text{CLOCK0}}$ Low to OUT3		6.4		3.8	5.1		6.4	ns	
T8	$\overline{\text{CLOCK0}}$ Low to OUT4		7.6		4.5	6.1		7.6	ns	
T9	$\overline{\text{CLOCK0}}$ Low to OUT5		8.8		5.3	7.1		8.8	ns	
T10	$\overline{\text{CLOCK0}}$ Low to OUT6		10.0		6.0	8.1		10.0	ns	
T11	CLOCK1 Max Toggle Freq.	1.6		1.7			1.6		GHz	2, 3

10G065 AC CHARACTERISTICS (Note 1)

VSS = -3.5V to -3.3V, VEE = -5.5V to -5.1V, VDDL=VDDO = 0V, unless otherwise indicated.

SYM-BOL	PARAMETER	Tc= 0°C		Tc = +25°C			Tc= +85°C		UNITS	NOTES
		MIN	MAX	MIN	TYP	MAX	MIN	MAX		
T12	CLOCK1 Low Time	310		290			310		ps	2, 3
T13	CLOCK1 High Time	310		290			310		ps	2, 3
T14	CLOCK1 High to OUT1		2.3		1.3	1.8		2.3	ns	
T15	CLOCK1 High to OUT2		3.8		2.3	3.0		3.8	ns	
T16	CLOCK1 High to OUT3		5.2		3.1	4.2		5.2	ns	
T17	CLOCK1 High to OUT4		6.4		3.8	5.1		6.4	ns	
T18	CLOCK1 High to OUT5		7.6		4.5	6.1		7.6	ns	
T19	CLOCK1 High to OUT6		8.8		5.3	7.1		8.8	ns	
T20	CLEAR Setup Time				190				ps	
T21	CLEAR Hold Time				190				ps	
T22	CLEAR Pulse Width				650				ps	
T23	CLEAR High to OUT1-6 Low				800				ps	
T24	CLKEN Setup Time				110				ps	
T25	CLKEN Hold Time				110				ps	
Tr	Output Rise Time				500				ps	4
Tf	Output Fall Time				250				ps	4

10G065-3 AC CHARACTERISTICS (Note 1)

VSS = -3.5V to -3.3V, VEE = -5.5V to -5.1V, VDDL=VDDO = 0V, unless otherwise indicated.

SYM-BOL	PARAMETER	Tc= 0°C		Tc = +25°C			Tc= +85°C		UNITS	NOTES
		MIN	MAX	MIN	TYP	MAX	MIN	MAX		
T1	CLOCK0 Max Toggle Freq.	1.5		2.0			1.5		GHz	2, 3
T2	CLOCK0 Low Time	330		250			330		ps	2, 3
T3	CLOCK0 High Time	330		250			330		ps	2,3
T4	CLOCK0 Low to OUT0		2.9		1.9	2.4		2.9	ns	
T5	CLOCK0 Low to OUT1		4.9		2.9	3.9		4.9	ns	
T6	CLOCK0 Low to OUT2		6.9		3.9	5.4		6.9	ns	
T7	CLOCK0 Low to OUT3		8.5		4.8	6.4		8.5	ns	
T8	CLOCK0 Low to OUT4		11.0		5.7	7.6		11.0	ns	
T9	CLOCK0 Low to OUT5		12.0		6.6	8.8		12.0	ns	
T10	CLOCK0 Low to OUT6		14.0		7.5	10.0		14.0	ns	
T11	CLOCK1 Max Toggle Freq.	1.4		1.6			1.4		GHz	2, 3
T12	CLOCK1 Low Time	350		310			350		ps	2, 3
T13	CLOCK1 High Time	350		310			350		ps	2, 3
T14	CLOCK1 High to OUT1		2.9		1.7	2.4		2.9	ns	
T15	CLOCK1 High to OUT2		4.9		2.9	3.9		4.9	ns	
T16	CLOCK1 High to OUT3		6.9		3.9	5.4		6.9	ns	
T17	CLOCK1 High to OUT4		8.5		4.8	6.4		8.5	ns	
T18	CLOCK1 High to OUT5		11.0		5.7	7.6		11.0	ns	
T19	CLOCK1 High to OUT6		12.0		6.6	8.8		12.0	ns	
T20	CLEAR Setup Time				260				ps	
T21	CLEAR Hold Time				260				ps	
T22	CLEAR Pulse Width				1100				ps	

10G065-3 AC CHARACTERISTICS (Note 1)

VSS = -3.5V to -3.3V, VEE = -5.5V to -5.1V, VDDL=VDDO = 0V, unless otherwise indicated.

SYMBOL	PARAMETER	Tc= 0°C		Tc = +25°C			Tc= +85°C		UNITS	NOTES
		MIN	MAX	MIN	TYP	MAX	MIN	MAX		
T23	$\overline{\text{CLEAR}}$ High to OUT1-6 Low				1200				ps	
T24	CLKEN Setup Time				140				ps	
T25	CLKEN Hold Time				140				ps	
Tr	Output Rise Time				500				ps	4
Tf	Output Fall Time				250				ps	4

10G065K-2 AC CHARACTERISTICS (Note 1)

VSS = -3.5V to -3.3V, VEE = -5.5V to -5.1V, VDDL=VDDO = 0V, unless otherwise indicated.

SYMBOL	PARAMETER	Tc= -40°C		Tc = +25°C			Tc= +100°C		UNITS	NOTES
		MIN	MAX	MIN	TYP	MAX	MIN	MAX		
T1	$\overline{\text{CLOCK0}}$ Max Toggle Freq.	2.0		3.0			2.0		GHz	2, 3
T2	$\overline{\text{CLOCK0}}$ Low Time	250		165			250		ps	2, 3
T3	$\overline{\text{CLOCK0}}$ High Time	250		165			250		ps	2,3
T4	$\overline{\text{CLOCK0}}$ Low to OUT0		2.4		1.1	1.5		2.4	ns	
T5	$\overline{\text{CLOCK0}}$ Low to OUT1		3.9		1.9	2.5		3.9	ns	
T6	$\overline{\text{CLOCK0}}$ Low to OUT2		5.4		2.6	3.5		5.4	ns	
T7	$\overline{\text{CLOCK0}}$ Low to OUT3		6.4		3.2	4.3		6.4	ns	
T8	$\overline{\text{CLOCK0}}$ Low to OUT4		7.6		3.8	5.1		7.6	ns	
T9	$\overline{\text{CLOCK0}}$ Low to OUT5		8.8		4.4	5.9		8.8	ns	
T10	$\overline{\text{CLOCK0}}$ Low to OUT6		10.0		5.0	6.7		10.0	ns	
T11	CLOCK1 Max Toggle Freq.	1.6		2.4			1.6		GHz	2, 3
T12	CLOCK1 Low Time	200		200			310		ps	2, 3
T13	CLOCK1 High Time	200		200			310		ps	2, 3
T14	CLOCK1 High to OUT1		2.3		1.1	1.5		2.3	ns	
T15	CLOCK1 High to OUT2		3.8		1.9	2.5		3.8	ns	
T16	CLOCK1 High to OUT3		5.2		2.6	3.5		5.2	ns	
T17	CLOCK1 High to OUT4		6.4		3.2	4.3		6.4	ns	
T18	CLOCK1 High to OUT5		7.6		3.8	5.1		7.6	ns	
T19	CLOCK1 High to OUT6		8.8		4.4	5.9		8.8	ns	
T20	$\overline{\text{CLEAR}}$ Setup Time				160				ps	
T21	$\overline{\text{CLEAR}}$ Hold Time				160				ps	
T22	$\overline{\text{CLEAR}}$ Pulse Width				550				ps	
T23	$\overline{\text{CLEAR}}$ High to OUT1-6 Low				700				ps	
T24	CLKEN Setup Time				110				ps	
T25	CLKEN Hold Time				110				ps	
Tr	Output Rise Time				500				ps	4
Tf	Output Fall Time				250				ps	4

10G065K AC CHARACTERISTICS (Note 1)

VSS = -3.5V to -3.3V, VEE = -5.5V to -5.1V, VDDL=VDDO = 0V, unless otherwise indicated.

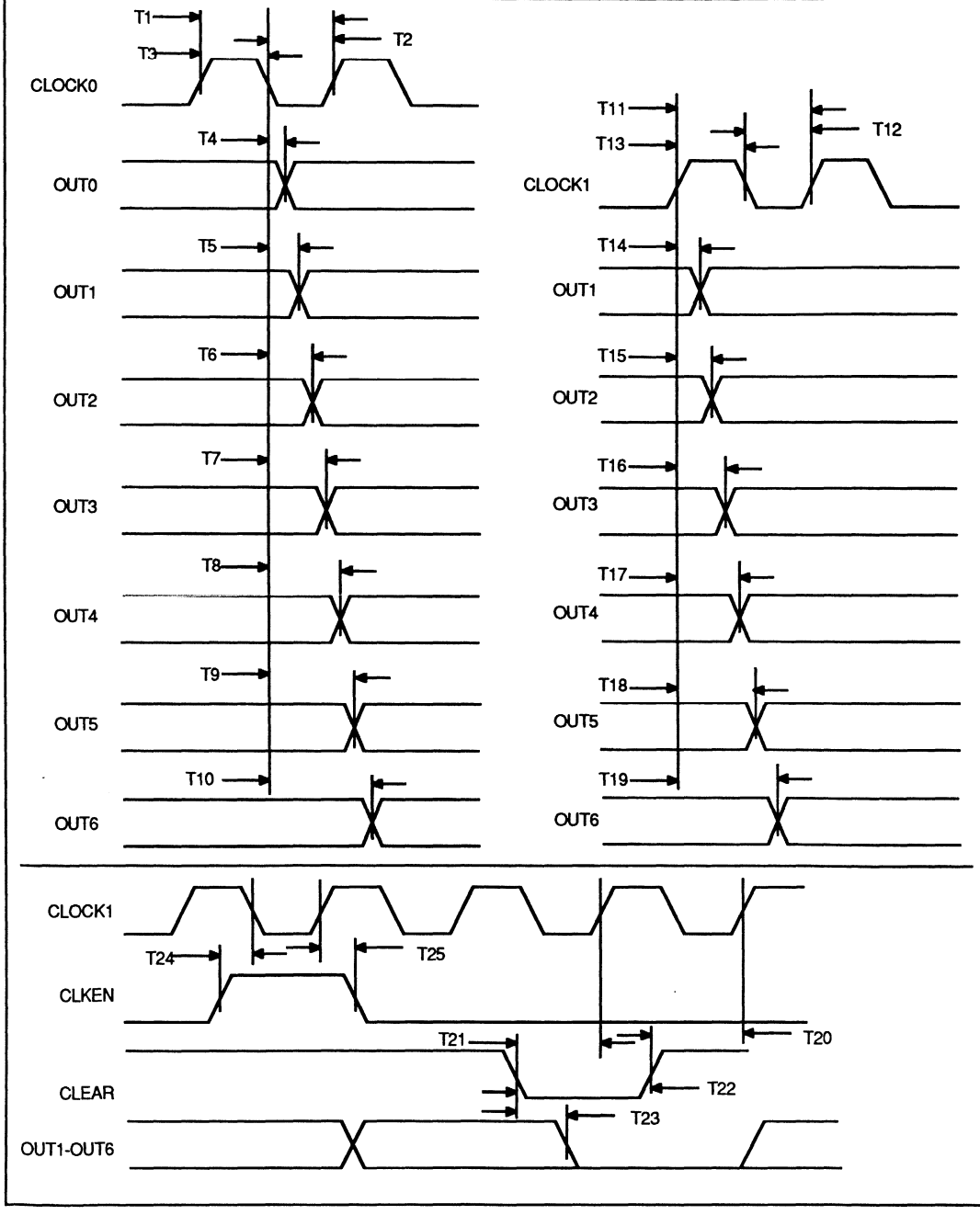
SYM-BOL	PARAMETER	Tc= -40°C		Tc = +25°C			Tc= +100°C		UNITS	NOTES
		MIN	MAX	MIN	TYP	MAX	MIN	MAX		
T1	$\overline{\text{CLOCK0}}$ Max Toggle Freq.	1.5		2.5			1.5		GHz	2, 3
T2	$\overline{\text{CLOCK0}}$ Low Time	330		200			330		ps	2, 3
T3	$\overline{\text{CLOCK0}}$ High Time	330		200			330		ps	2, 3
T4	$\overline{\text{CLOCK0}}$ Low to OUT0		2.9		1.3	1.8		2.9	ns	
T5	$\overline{\text{CLOCK0}}$ Low to OUT1		4.9		2.3	3.0		4.9	ns	
T6	$\overline{\text{CLOCK0}}$ Low to OUT2		6.9		3.1	4.2		6.9	ns	
T7	$\overline{\text{CLOCK0}}$ Low to OUT3		8.5		3.8	5.1		8.5	ns	
T8	$\overline{\text{CLOCK0}}$ Low to OUT4		11.0		4.5	6.1		11.0	ns	
T9	$\overline{\text{CLOCK0}}$ Low to OUT5		12.0		5.3	7.1		12.0	ns	
T10	$\overline{\text{CLOCK0}}$ Low to OUT6		14.0		6.0	8.1		14.0	ns	
T11	CLOCK1 Max Toggle Freq.	1.4		1.7			1.4		GHz	2, 3
T12	CLOCK1 Low Time	350		290			350		ps	2, 3
T13	CLOCK1 High Time	350		290			350		ps	2, 3
T14	CLOCK1 High to OUT1		2.9		1.3	1.8		2.9	ns	
T15	CLOCK1 High to OUT2		4.9		2.3	3.0		4.9	ns	
T16	CLOCK1 High to OUT3		6.9		3.1	4.2		6.9	ns	
T17	CLOCK1 High to OUT4		8.5		3.8	5.1		8.5	ns	
T18	CLOCK1 High to OUT5		11.0		4.5	6.1		11.0	ns	
T19	$\overline{\text{CLOCK1}}$ High to OUT6		12.0		5.3	7.1		12.0	ns	
T20	$\overline{\text{CLEAR}}$ Setup Time				190				ps	
T21	$\overline{\text{CLEAR}}$ Hold Time				190				ps	
T22	$\overline{\text{CLEAR}}$ Pulse Width				650				ps	
T23	CLEAR High to OUT1-6 Low				800				ps	
T24	CLKEN Setup Time				110				ps	
T25	CLKEN Hold Time				110				ps	
Tr	Output Rise Time				500				ps	4
Tf	Output Fall Time				250				ps	4

NOTES: 1. Test Conditions, unless otherwise stated:

Ta = 25°C	VICH = 0V	VDCH = 0V
VDDL = VDDO = 0V	VICL = VSS	VDCL = VSS
VEE = -5.2V	VLCH = -1.5V	VOH ≥ -0.8V
VSS = -3.4V	VLCL = -1.25V	VOL ≤ -1.8V
RLOAD = 50Ω to -2.0V	VTTC = -2.0V	VTRIM = VEE

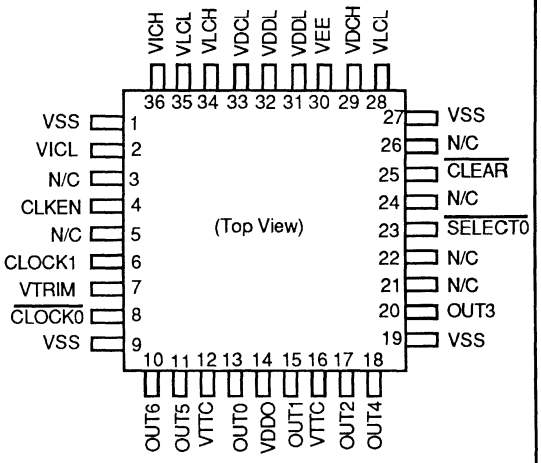
2. $\overline{\text{CLOCK0}}$ and CLOCK1 rise and fall times ≤150ps (measured from the 20% and 80% points)
3. $\overline{\text{CLOCK0}}$ and CLOCK1 input = 2V pp sine wave, -1.3V DC offset.
4. Rise and Fall times are measured at the 20% and 80% points of the transition from VOL max to VOH min.

SWITCHING WAVEFORMS



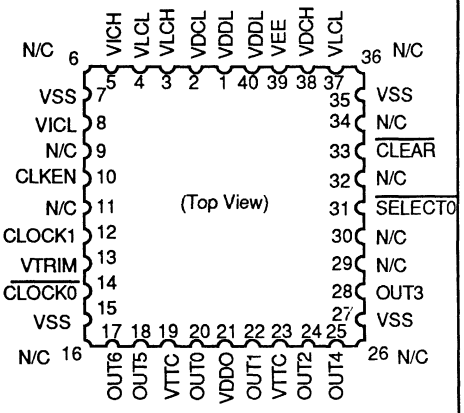
PACKAGE PINOUT DIAGRAM

36 LEAD FLATPACK
PACKAGE TYPE "F"



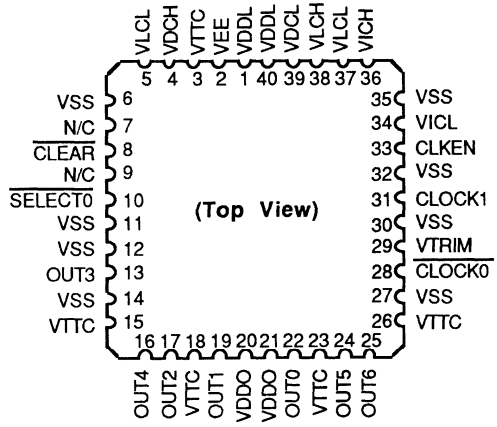
NOTES: Pin 1 is marked for orientation. N/C = No Connection. The package bottom surface is at VSS potential.

36 I/O LEADLESS CHIP CARRIER
PACKAGE TYPE "L36"



NOTES: Pin 1 is marked for orientation. N/C = No Connection. The package lid, bottom heat vias, and 4 N/C corner pins (6,16,26,36) are at Vss potential.

Pin Functions - 40 Pin Type "C" and "L" Packages



N/C = No Connection

GigaBit Logic

10G070
10G070K

Variable Modulus Divider
2.0 GHz Clock Rate
10G PicoLogic™ Family

DISTINCTIVE CAPABILITIES

- 2.0 GHz operation (25°C min.)
- 0°C to 85°C commercial temp. range, 10G070
- -40°C to 100°C extended temp. range, 10G070K
- Fixed divide by 5, 6, 10, 11, 20, 21, 40, 41
- Variable modulus operation selectable for divide by 5 and 6, 10 and 11, 20 and 21, or 40 and 41
- Wire-OR output capability
- Mode pin allows 10G PicoLogic, TTL, and CMOS control of N or N+1 division ratio
- 10G PicoLogic, TTL/CMOS I/O compatible
- Available in flatpack, leadless chip carrier (LCC) or dice form
- Packages contain internal decoupling capacitors for optimum high frequency performance

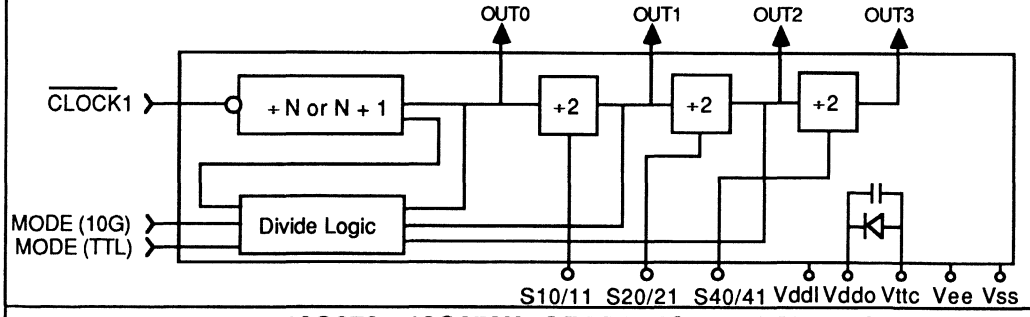
APPLICATIONS

- Frequency synthesizers and phase locked loops (with 10G061 Synchronous Counter and 16G044 Phase Frequency Comparator)

FUNCTIONAL DESCRIPTION

The 10G070 is an ultra-fast 2.0 GHz performance variable modulus divider for use in frequency synthesis and phase locked loop applications. By strapping the S10/11, S20/21, and S40/41 pins to VSS or VEE one of the following four N and N+1 division ratio pairs can be programmed: 5 and 6,10 and 11, 20 and 21, and 40 and 41. When the MODE input is switched to a logic high the counter will divide by N (5, 10, 20, or 40). When the MODE input is switched to a logic low the counter will divide by N+1 (6, 11, 21, or 41). A fixed divide ratio can be obtained by fixing the logic level of the MODE input. When the 10G070 is used to divide by 5 or 6, the output appears on the OUT0 pin. For division by 10 or 11, 20 or 21, and 40 or 41 the output appears on the OUT1, OUT2 and OUT3 pins, respectively. For divide by N ratios, all lower order ratios are simultaneously available.

BLOCK DIAGRAM



10G070, 10G070K ORDERING INFORMATION

PACKAGE TYPE	SPEED				
	10G070 (0°C to 85°C)			10G070K (-40°C to 100°C)	
	1.5 GHz	1.3 GHz	1.0 GHz	1.5 GHz	1.0 GHz
36 I/O Leadless carrier	10G070-2L36	10G070-L36	10G070-3L36	10G070K-2L36	10G070K-L36
36 I/O Flatpack	10G070-2F	10G070-F	10G070-3F	10G070K-2F	10G070K-F
40 I/O Leadless carrier	10G070-2L	10G070-L	10G070-3L	10G070K-2L	10G070K-L
40 I/O C- Leaded carrier	10G070-2C	10G070-C	10G070-3C	10G070K-2C	10G070K-C
Unpackaged Dice			10G070-3X		10G070K-X

FUNCTIONAL DESCRIPTION (cont.)

Also, divide by 5 and 10 are always available. The Mode input has two pins; MODE(10G) for 10G PicoLogic control interface, and MODE(TTL) for TTL and CMOS control interface. When driving the MODE(10G) input the MODE(TTL) pin should be left open. Similarly, when driving the MODE(TTL) input the MODE(10G) pin should be left open. It should be noted that the 10G070 inputs are not ECL compatible. A 10G002 XOR/XNOR/Line Receiver can be used as an ECL to GaAs level translator. The 10G070 has optional clamp inputs to provide flexibility when interfacing to other components. When connected to a supply voltage at the input threshold of -1.3V, input clamps VICH and VICL allow the 10G070 to be driven with input signals greater than 2.0Vp-p without damage to the internal gates. This is particularly useful when the 10G070 CLOCK pin is driven directly from a voltage controlled oscillator (VCO). When not used, input clamp VICH should be connected to VDDL (GND) and VICL to VSS (-3.4V). Logic clamps VLCH and VLCL provide a means of limiting the voltage swing of internal gates, thus increasing the performance of the divider. The recommended voltages for VLCH and VLCL are indicated with the notes for the AC characteristics specifications. When not used the VLCH and VLCL pins may be left open. The output driver high level clamp, VDCH, is not used when driving GaAs logic, but may be used to limit VOH when driving ECL. See App. Note 4 for details.

PIN DESCRIPTIONS

$\overline{\text{CLOCK}}$	High speed clock input. The falling edge of $\overline{\text{CLOCK}}$ causes the outputs to change.
MODE (10G)	Mode control input. When high the device counts by N, when low the device counts by N+1. The input is 10G level compatible. When MODE(TTL) is used then MODE(10G) must be left open.
MODE (TTL)	Mode control input. When high the device counts by N, when low, the device counts by N+1. This input is level shifted internally to make it TTL compatible. When MODE(10G) is used M ODE(TTL) must be left open.
OUT0-OUT3	Divide by 5 or 6 output, OUT0 Divide by 10 or 11 output, OUT1 Divide by 20 or 21 output, OUT2 Divide by 40 or 41 output, OUT3.
S10/11	Select 10/11inputs.
S20/21	Select 20/21 inputs.
S40/41	Select 40/41 inputs. Program the valid output by strapping these inputs to VSS or VEE according to the programming table in the 10G070 Operation section of this datasheet.
VDDO	Output driver ground (0V).
VDDL	Internal logic ground (0V).
VSS	-3.4V power supply.
VEE	-5.2V power supply.
VTTC	The AC return pin for the internal VDDO decoupling capacitor. VTTC is not brought into the 10G070 die. VTTC is typically tied to VTT (nominally -2.0V).
VDCH	Output driver high level clamp voltage. May be used to limit VOH when driving ECL. When driving GaAs, should be disabled by connecting to VDDO.
VICH, VICL	Input protection clamp voltages. When connected to -1.3V, these allow an overdriven sine wave input signal to be truncated to a square wave, thus providing faster rise and fall times at the $\overline{\text{CLOCK}}$ input. .
VLCH, VLCL	Logic clamp voltages. When connected as specified in the AC Characteristic Notes these pins clamp the internal logic voltage swing of the device, thus enhancing the AC performance of the part. When not used these pins may be left open.
VTRIM	Input threshold adjustment voltage. A value of VTRIM more or less negative than VEE will adjust all the input thresholds around their nominal value of -1.3V. Connect to VEE when not used.

10G070 PROGRAMMING

The operation of the 10G070 is described by the following function select table. The S10/11, S20/21, S40/41 inputs are strapped to select a fixed set of N/N+1 division ratios. The MODE input is logically controlled to select a variable modulus divide by N and N+1 operation or strapped to select a fixed N or N+1 divider operation. The MODE control input may be arbitrarily changed throughout most of the count cycle without affecting the output. However, the MODE input must be stable at the desired logic high or logic low level for the specified set-up and hold time before and after the high to low $\overline{\text{CLOCK}}$ transition that causes the chosen output to transition from a low (0) to a high (1).

S40/41	S20/21	S10/11	MODE	DIVISION RATIO	OUTPUT PIN
VSS	VSS	VSS	0	6	OUT0
VSS	VSS	VSS	1	5	OUT0
VSS	VSS	VEE	0	11	OUT1
VSS	VSS	VEE	1	10	OUT1
VSS	VEE	VEE	0	21	OUT2
VSS	VEE	VEE	1	20	OUT2
VEE	VEE	VEE	0	41	OUT3
VEE	VEE	VEE	1	40	OUT3

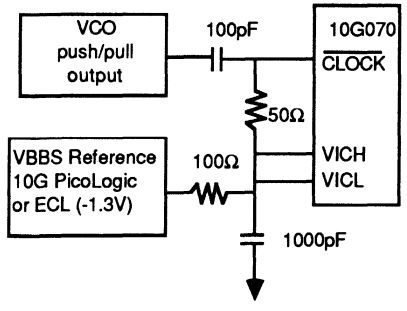
Another distinctive feature of the 10G070 Variable Modulus Divider is the availability of lower order divide ratio outputs.The table below shows the simultaneously available outputs for any given divide ratio. This feature will allow designers additional flexibility in synthesizer design.

	OUTPUTS			
PROGRAMMED RATIO	OUT0 (÷5/6)	OUT1 (÷10/11)	OUT2 (÷20/21)	OUT3 (÷40/41)
÷40	÷5	÷10	÷20	÷40
÷41	7x5 + 1x6	3x10 + 1x11	1X20 +1X21	÷41
÷20	÷5	÷10	÷20	—
÷21	3x5 + 1x6	1x10 + 1x11	÷21	—
÷10	÷5	÷10	—	—
÷11	1x5 + 1x6	÷11	—	—
÷5	÷5	÷10	—	—
÷6	÷6	2x5 + 1x1	—	—

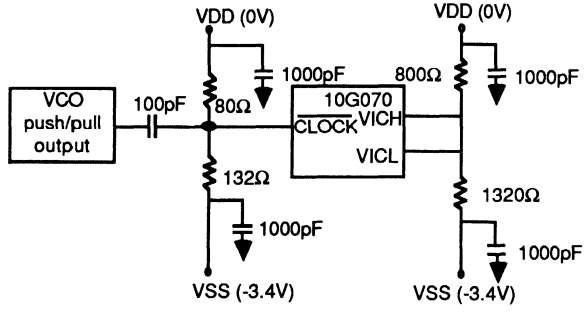
VOLTAGE CONTROLLED OSCILLATOR (VCO) INTERFACE

The $\overline{\text{CLOCK}}$ pin of the 10G070 has an input threshold of -1.3V. To interface the device to a general purpose VCO an AC coupling network is recommended. There are two common cases; one in which the input threshold VBB (-1.3V) is available, and another when VBB is not available.

VCO Interface to 10G070 With VBB Reference

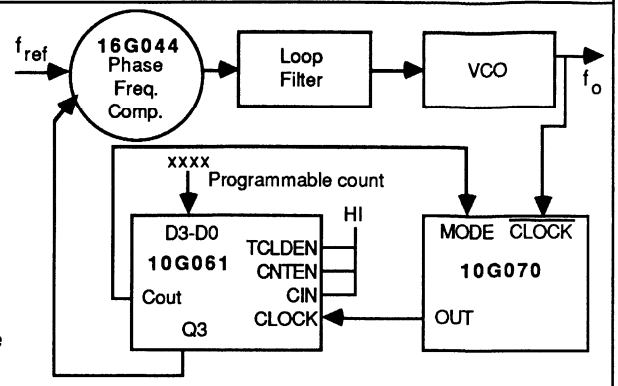


VCO Interface to 10G070 Without VBB Reference



Frequency Synthesis Applications

The 10G070, in combination with GigaBit's 10G061 Four Stage Synchronous Programmable Counter, provides the components necessary to design very high speed (2GHz) programmable counters for application in synthesizer phase locked loops using the pulse swallowing, or swallow counter technique. This technique uses programmable counters to toggle the MODE control of the 10G070 between modulus N and N+1 to switch among a large number of synthesizer output frequencies. Further information is provided in the 10G061 datasheet. A typical programmable frequency synthesizer block diagram is shown.



ABSOLUTE MAXIMUM RATINGS

(Beyond which useful life may be impaired) (Note 1)

SYMBOL	PARAMETER	ABSOLUTE MAXIMUM RATINGS	NOTES
TSTOR	Storage Temperature	- 65 °C to + 150 °C	
TJ	Junction Temperature	- 55 °C to + 150 °C	
TC	Case Temperature Under Bias	- 55 °C to + 125 °C	2
VDDO	Output Driver Supply Voltage	-0.8 V to + 1.0 V	
VSS	Supply Voltage	- 4.0 V to + 0.5 V	
VEE	Supply Voltage	- 7.0 V to VSS + 0.5 V	
VIN	Voltage Applied to Any Input; Continuous VSS = - 3.4 V, VEE = - 5.2 V	- 4.0 V to + 0.5 V	
VINTTL	Voltage Applied to MODE(TTL); Continuous	- 4.0 V to + 4.0 V	
I IN	Current Into Any Input; Continuous	- 0.5 mA to 1.0 mA	
VOUT	Voltage Applied to Any Output	-4.0V to + 7.0 V	3
IOUT	Current From Any Output; Continuous	-70 mA	
PD	Power Dissipation Per Output POUT = (VDDO-VOUT) x IOUT	100 mW	
VTTC	VDDO Internal Decoupling Cap. Return	-6.0 V to VDDO	
VTT	Load Termination Supply	-6.0 V to VDDO + 6.0 V	
VDCH	Output Driver Clamp Voltage	VSS to VDDO	4
IDCH	Output Driver Clamp Current	-20 mA	
VICH	Input Clamp High Voltage	-2.0V to VDDL	5
IICH	Input Clamp High Current	-20mA	
VICL	Input Clamp Low Voltage	VSS to -0.4V	5
IICL	Input Clamo Low Current	20 mA	
VLCH	Logic Clamp High Voltage	-2.0V to VDDL	5
ILCH	Logic Clamp High Current	-40mA	
VLCL	Logic Clamp Low Voltage	VSS TO 0.4V	5
ILCL	Logic Clamp Low Current	-40 mA	

Notes:
1. All voltages specified with VDDL defined as 0 V. Positive current is defined as current into the device.
2. TC is measured at case bottom.
3. Subject to IOUT and power dissipation limitations.
4. Subject to IDCH and power dissipation limitations.
5. Subject to clamp current and power dissipation limitations.

10G070 RECOMMENDED OPERATING CONDITIONS (note 3)

SYMBOL	PARAMETER	MIN	NOM	MAX	UNITS	NOTES
TC1	Case Operating Temp. (10G070)	0	25	85	℃	1
TC2	Case Operating Temp. (10G070K)	-40	25	100	℃	1
VDDL	Logic Supply Voltage		GND		V	
VDDO	Output Driver Supply Voltage	-0.8	GND	+1.0	V	
VSS	Supply Voltage	- 3.5	- 3.4	- 3.3	V	
VEE	Supply Voltage	- 5.5	- 5.2	- 5.1	V	
VTTC	VDDO Internal Decoupling Return	VSS	VTT	VDDO	V	
VTT	Load Termination Supply Voltage	VSS	- 2.0	- 2.0	V	2
RLOAD	Output Termination Load Resistance	25	50	100	Ω	2
VICH	Input Clamp High Voltage	-1.8	VDDL	VDDL	V	
VICL	Input Clamp Low Voltage	VSS	VSS	-0.8	V	
VLCH	Logic Clamp High Voltage	-1.8	VDDL	VDDL	V	
VLCL	Logic Clamp Low Voltage	VSS	VSS	-0.8	V	
VDCH	Output Driver Clamp High Voltage	-2.5	-2.0	VDDO	V	4
VTRIM	Input Threshold Adjust Voltage	VEE-1	VEE	VEE+1	V	

NOTES
1. Tcase measured at case bottom. **User attention to device thermal management is recommeded.** See GigaBit Application Note 3, "Thermal Management of PicoLogic and NanoRam GaAs Digital IC Families" for a complete discussion of all aspects of device thermal management.
2. The RLOAD and VTT combination used is subject to maximum output current and power restrictions.
3. See GigaBit Application Note - 4 for a discussion of interfacing requirements to and from PicoLogic devices.
4. When driving GaAs logic, VDCH is not used. To limit VOH when driving ECL, see App. Note 4.

10G070/K DC CHARACTERISTICS (Notes 1,2)

TC = 40°C to +100°C, VSS = -3.5V to -3.3V, VEE = -5.5V to -5.1V, VDDL=VDDO = 0V, unless otherwise indicated.

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	TEST CONDITIONS	NOTES
VOH	Output Voltage High	- 0.8	-0.6	-0.3	V		
VOL	Output Voltage Low	- 2.0	-1.9	- 1.8	V		
IOH	Output Current High		-70	-60	mA	VOH = -0.8V	
VIH1	Input Voltage High (70)	- 0.6		VDDL	V		4,5
VIL1	Input Voltage Low (70)	VSS		- 1.9	V		4,5
VIH2	Input Voltage High (70K)	-0.6		VDDL	V		4,5
VIL2	Input Voltage Low (70K)	VSS		-2.1	V		4,5
VIH(TTL)	Input Voltage High TTL	2.8		3.5	V		
VIL(TTL)	Input Voltage Low TTL	-1.0		0.8	V		
IIN	Input Current		200	500	uA	VIN = -0.6V to -1.9V	
ISS	Power Supply Current		110	200	mA		
IEE	Power Supply Current		18	25	mA		
PD	Power Dissipation		500	850	mW		3

Notes:
1. These characteristics are applicable from DC to 500MHz.
2. Test conditions (unless otherwise indicated) :
   VTT = -2.0V VTRIM = VEE
   VTTC = VTT
   RLOAD = 50Ω to -2.0V
   IOH is the available output current at VOH = -0.8V.
3. At nominal supply voltages and 50% duty cycle. Exclusive of VDDO output source follower power (typically 15 mW per output) and output clamp power (if any).
4. CLOCK input rise and fall times ≤ 2ns (measured from the 20% and 80% points).
5. Input levels are 10G PicoLogic compatible.

USER NOTES:
Unlike most PicoLogic circuits, the input threshold of the 10G065 is not stablized with a VBB feedback circuit. Therefore, the threshold of all inputs will vary from their nominal -1.3V room temperature level with variations in VSS and temperature. VTRIM may be used to compensate for threshold drift. This approach is detailed in App. Note 4. Alternatively, it is necessary to drive each used input with large peak-to-peak level signals as shown for VIH and VIL in the DC Characterisits table. Under high speed conditions, the clock input should be ≥2Vp-p to achieve maximum speed as described in the notes to th AC Characteristics tables. Other PicoLogic devices can be used as drivers to provide these levels by terminating the outputs to VSS instead of the more usual VTT.

10G070-2 AC CHARACTERISTICS (Note 1)

VSS = -3.5V to -3.3V, VEE = -5.5V to -5.1V, VDDL=VDDO = 0V, unless otherwise indicated.

SYM-BOL	PARAMETER	Tc= 0°C		Tc = +25°C			Tc= +85°C		UNITS	NOTES
		MIN	MAX	MIN	TYP	MAX	MIN	MAX		
T1	$\overline{\text{CLOCK}}$ Maximum Toggle Frequency	1.5		2.0			1.5		GHz	2,3
T2	$\overline{\text{CLOCK}}$ Low Time	333		250			333		ps	2,3
T3	$\overline{\text{CLOCK}}$ High Time	333		250			333		ps	2,3
T4	MODE to $\overline{\text{CLOCK}}$ Low (Mode Setup Time)	690		500			690		ps	4
T5	$\overline{\text{CLOCK}}$ Low to MODE (Mode Hold Time)	345		250			345		ps	4
T6	$\overline{\text{CLOCK}}$ Low to OUT0		1.9			1.5		1.9	ns	
T7	$\overline{\text{CLOCK}}$ Low to OUT1		3.0			2.5		3.0	ns	
T8	$\overline{\text{CLOCK}}$ Low to OUT2		4.1			3.5		4.1	ns	
T9	$\overline{\text{CLOCK}}$ Low to OUT3		5.3			4.5		5.3	ns	

10G070 AC CHARACTERISTICS (Note 1)

VSS = -3.5V to -3.3V, VEE = -5.5V to -5.1V, VDDL=VDDO = 0V, unless otherwise indicated.

SYM-BOL	PARAMETER	Tc= 0°C		Tc = +25°C			Tc= +85°C		UNITS	NOTES
		MIN	MAX	MIN	TYP	MAX	MIN	MAX		
T1	$\overline{\text{CLOCK}}$ Maximum Toggle Frequency	1.3		1.75			1.3		GHz	2,3
T2	$\overline{\text{CLOCK}}$ Low Time	385		285			385		ps	2,3
T3	$\overline{\text{CLOCK}}$ High Time	385		285			385		ps	2,3
T4	MODE to $\overline{\text{CLOCK}}$ Low (Mode Setup Time)	770		575			770		ps	4
T5	$\overline{\text{CLOCK}}$ Low to MODE (Mode Hold Time)	385		285			385		ps	4
T6	$\overline{\text{CLOCK}}$ Low to OUT0		2.3			1.9		2.3	ns	
T7	$\overline{\text{CLOCK}}$ Low to OUT1		4.6			3.0		4.6	ns	
T8	$\overline{\text{CLOCK}}$ Low to OUT2		6.3			4.1		6.3	ns	
T9	$\overline{\text{CLOCK}}$ Low to OUT3		8.2			5.3		8.2	ns	

10G070-3 AC CHARACTERISTICS (Note 1)

VSS = -3.5V to -3.3V, VEE = -5.5V to -5.1V, VDDL=VDDO = 0V, unless otherwise indicated.

SYMBOL	PARAMETER	Tc= 0°C		Tc = +25°C			Tc= +85°C		UNITS	NOTES
		MIN	MAX	MIN	TYP	MAX	MIN	MAX		
T1	$\overline{\text{CLOCK}}$ Maximum Toggle Frequency	1.0		1.5			1.0		GHz	2,3
T2	$\overline{\text{CLOCK}}$ Low Time	415		333			415		ps	2,3
T3	$\overline{\text{CLOCK}}$ High Time	415		333			415		ps	2,3
T4	MODE to $\overline{\text{CLOCK}}$ Low (Mode Setup Time)	835		690			835		ps	4
T5	$\overline{\text{CLOCK}}$ Low to MODE (Mode Hold Time)	415		345			415		ps	4
T6	$\overline{\text{CLOCK}}$ Low to OUT0		2.5			2.2		2.5	ns	
T7	$\overline{\text{CLOCK}}$ Low to OUT1		5.0			3.6		5.0	ns	
T8	$\overline{\text{CLOCK}}$ Low to OUT2		7.0			4.9		7.0	ns	
T9	$\overline{\text{CLOCK}}$ Low to OUT3		9.0			6.3		9.0	ns	

10G070K-2 AC CHARACTERISTICS (Note 1)

VSS = -3.5V to -3.3V, VEE = -5.5V to -5.1V, VDDL=VDDO = 0V, unless otherwise indicated.

SYMBOL	PARAMETER	Tc= -40°C		Tc = +25°C			Tc= +100°C		UNITS	NOTES
		MIN	MAX	MIN	TYP	MAX	MIN	MAX		
T1	$\overline{\text{CLOCK}}$ Maximum Toggle Frequency	1.5		2.0			1.5		GHz	2,3
T2	$\overline{\text{CLOCK}}$ Low Time	333		250			333		ps	2,3
T3	$\overline{\text{CLOCK}}$ High Time	333		250			333		ps	2,3
T4	MODE to $\overline{\text{CLOCK}}$ Low (Mode Setup Time)	690		500			690		ps	4
T5	$\overline{\text{CLOCK}}$ Low to MODE (Mode Hold Time)	345		250			345		ps	4
T6	$\overline{\text{CLOCK}}$ Low to OUT0		1.9			1.5		1.9	ns	
T7	$\overline{\text{CLOCK}}$ Low to OUT1		3.0			2.5		3.0	ns	
T8	$\overline{\text{CLOCK}}$ Low to OUT2		4.1			3.5		4.1	ns	
T9	$\overline{\text{CLOCK}}$ Low to OUT3		5.3			4.5		5.3	ns	

10G070K-3 AC CHARACTERISTICS (Note 1)

VSS = -3.5V to -3.3V, VEE = -5.5V to -5.1V, VDDL=VDDO = 0V, unless otherwise indicated.

SYM-BOL	PARAMETER	Tc= -40°C		Tc = +25°C			Tc= +100°C		UNITS	NOTES
		MIN	MAX	MIN	TYP	MAX	MIN	MAX		
T1	CLOCK Maximum Toggle Frequency	1.0		1.5			1.0		GHz	2,3
T2	CLOCK Low Time	500		333			500		ps	2,3
T3	CLOCK High Time	500		333			500		ps	2,3
T4	MODE to CLOCK Low (Mode Setup Time)	1000		690			1000		ps	4
T5	CLOCK Low to MODE (Mode Hold Time)	500		345			500		ps	4
T6	CLOCK Low to OUT0		3.0			1.9		3.0	ns	
T7	CLOCK Low to OUT1		5.0			3.0		5.0	ns	
T8	CLOCK Low to OUT2		7.0			4.1		7.0	ns	
T9	CLOCK Low to OUT3		9.0			5.3		9.0	ns	

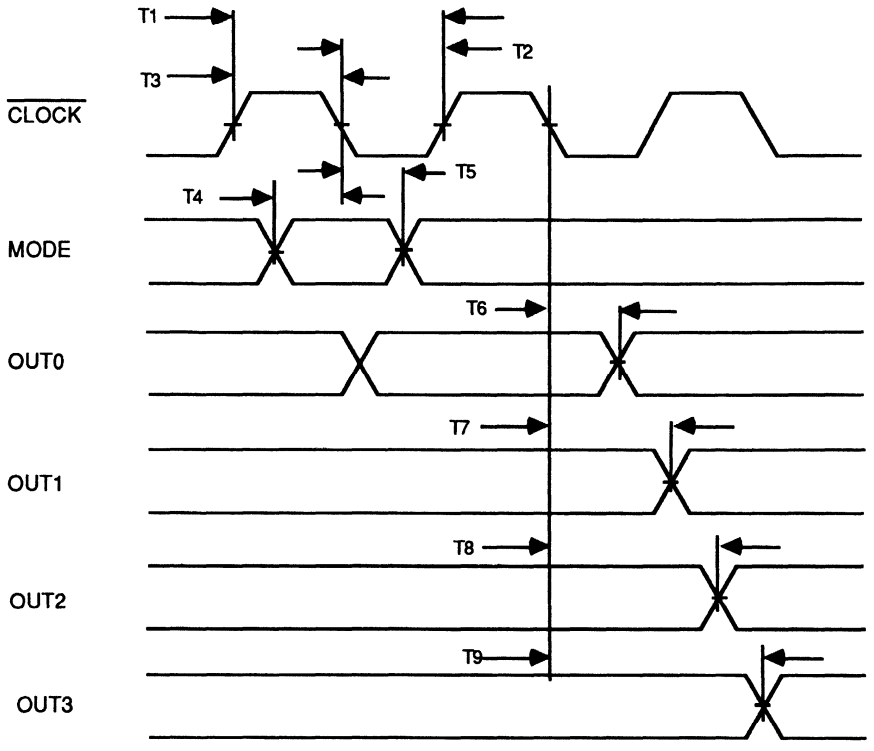
PHASE NOISE

	OFFSET (Hz)	RAW L(f)	CORRECTED dBc/Hz	
(+5)	1K	-116.7	-102.7	NOTES: Fin = 500MHz Noise Floor = -160dBc/Hz Input reference correction is 14dBc/Hz (+5) and 15.6dBc/Hz (+6).
	2.5K	-124.6	-110.6	
	5.0K	-128.7	-114.7	
	7.5K	-132.3	-118.3	
	10.0K	-132.9	-118.9	
	15.0K	-135.2	-121.2	
	20.0K	-137.6	-123.6	
	25.0K	-134.5	-120.5	
(+6)	1K	-121.7	-106.1	
	2.5K	-127.6	-112.0	
	5.0K	-129.4	-113.8	
	7.5K	-135.5	-119.9	
	10.0K	-138.1	-122.5	
	15.0K	-138.3	-122.7	
	20.0K	-140.8	-125.2	
	25.0K	-137.6	-122.0	

NOTES:

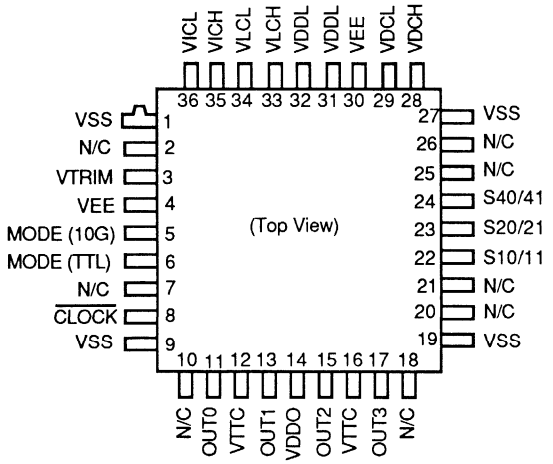
1. Test Conditions, unless otherwise stated:
   Ta = 25°C, VDDL = VDDO = 0V, VEE = -5.2V, VSS = -3.4V
   VICH = 0V, VICL = VSS, VLCH = -1.5V, VTTC = -2.0V
   VLCL = -1.25V, VDCH = 0V, VDCL = VSS, Output rise and fall times≤500ps (20% - 80%)
   VOH ≥ -0.8V, VOL ≤-1.8V, RLOAD = 50Ω to -2.0V
2. CLOCK rise and fall times ≤ 150 ps (measured from the 20% and 80% points).
3. Test conditions: CLOCK input = 2V pp sine wave, -1.3V DC offset.
4. The MODE control input may be arbitrarily changed throughout most the count cycle without affecting the output. However, the MODE input must be stable at the desired logic high or low level for the specified setup and hold time, respectively, before and after the high to low CLOCK transition that causes the chosen output to transition from a low (0) to a high (1).

SWITCHING WAVEFORMS



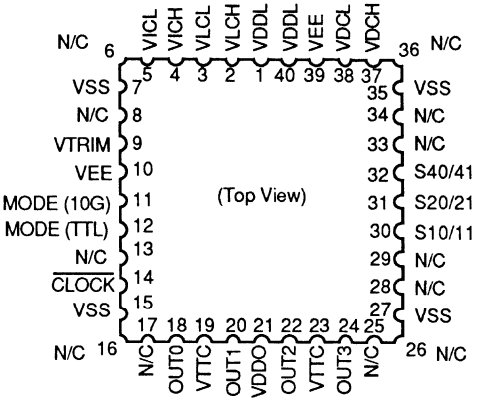
PACKAGE PINOUT DIAGRAM

36 LEAD FLATPACK
PACKAGE TYPE "F"



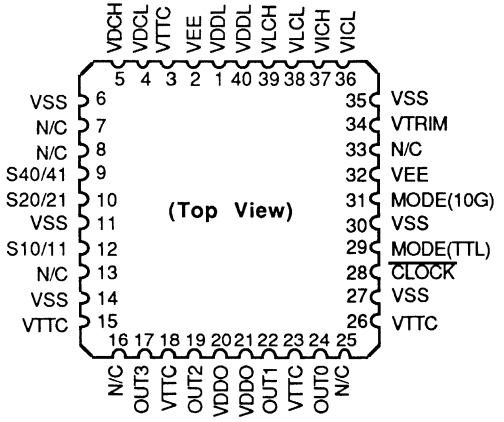
NOTES: Pin 1 is marked for orientation. N/C = No Connection. DNC = Do Not Connect. The package lid and bottom surface are at VSS potential.

36 PIN LEADLESS CHIP CARRIER
PACKAGE TYPE "L36"



NOTES: Pin 1 is marked for orientation. N/C = No Connection. DNC = Do Not Connect. The package lid, bottom heat vias, and 4 N/C corner pins (6,16,26,36) are at Vss potential.

40 PIN LEADLESS AND C-LEADED CHIP CARRIERS
PACKAGE TYPES "L" AND "C"



Note: N/C = No Connection

GigaBit Logic

10G100

High Speed 4-Bit Adder
1200 ps Propagation Delay / 1.3 GHz

10G PicoLogic™ Family

DISTINCTIVE CAPABILITIES

- Cascadable to provide N-bit addition
- 175 ps output rise and fall times
- High speed expansion using carry generate ($\overline{G}$), carry propagate ($P/\overline{P}$), and the10G101 carry lookahead generator
- Selectable active low carry output for ripple carry operations
- Selectable active high carry output for MSB
- $\overline{P}$ output for interface with ECL carry lookahead generators
- P output for higher speed interface with the 10G101 carry lookahead generator
- ECL and 10G PicoLogic™ compatible I/O with one set of inputs driven at GaAs levels
- Temperature and voltage compensated using VBB threshold reference input
- On chip threshold reference voltage supply (VBBS)
- Packages contain internal decoupling capacitors for optimum high frequency performance
- Available in 40 pin C-leaded or leadless chip carrier

APPLICATIONS

- High speed adders
- FFT processors
- Ones and twos complement arithmetic

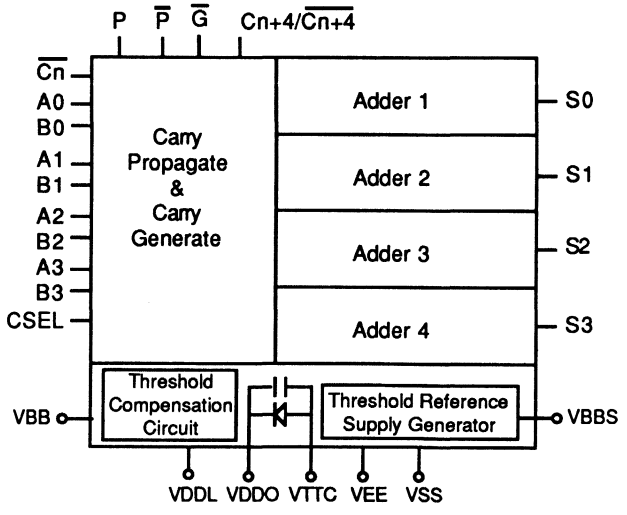
FUNCTIONAL DESCRIPTION

The 10G100 is an ultra-fast 4-bit adder capable of processing signals from DC to 1.3 GHz. The 10G100 performs a full 4-bit addition of two operands in 950 ps (typ.), four times faster than equivalent ECL adders. The 10G100 is cascadable to provide N-bit addition. It incorporates a carry output for ripple carry operations, and carry generate and carry propagate outputs for higher speed expansion schemes using the 10G101 carry lookahead generator.

For compatibility with other high speed logic families, the 10G100 features the PicoLogic™ family standard VBB input. This input allows the 10G100's threshold voltage to be controlled by the driving logic family. Therefore, mismatches in threshold level due to temperature and power supply variations can be compensated, providing high systems noise immunity. An on-chip threshold voltage output (pin VBBS) is also provided.

The 10G100 is a member of the10G PicoLogic™ family of gallium arsenide integrated circuits and is fabricated using GigaBit Logic's high volume, GaAs MESFET process technology.

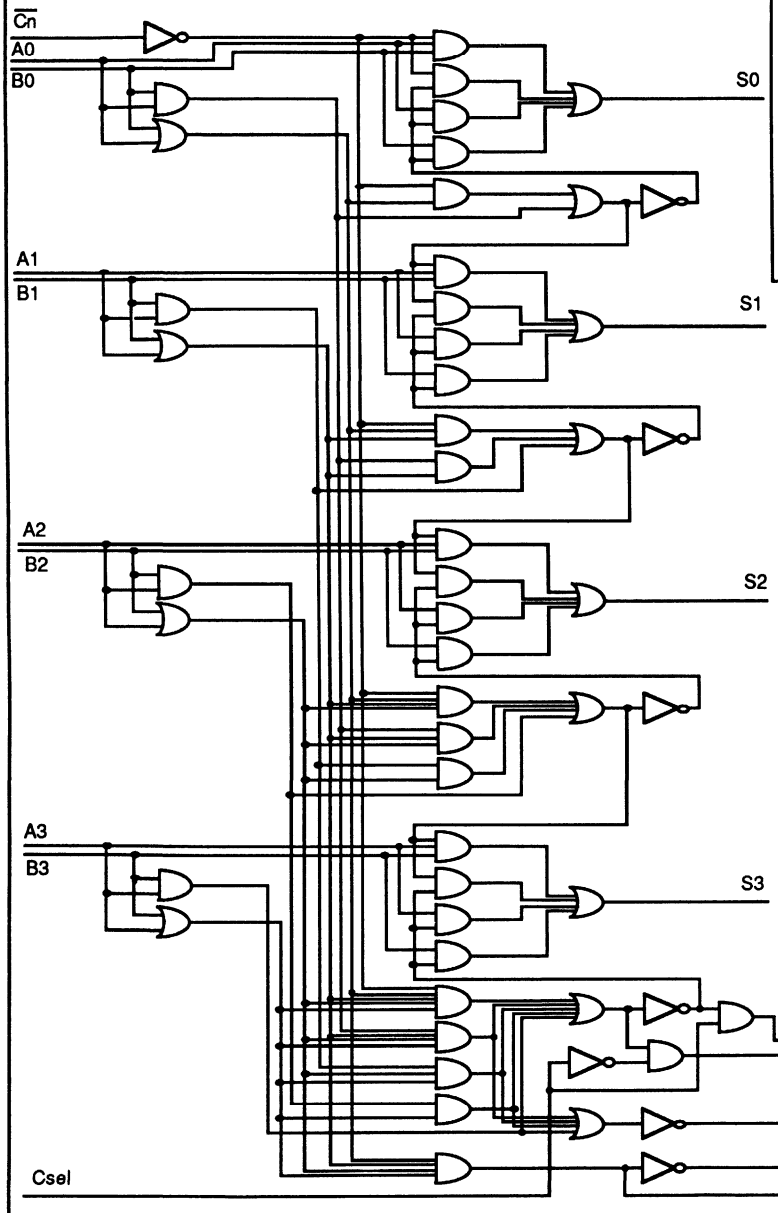
BLOCK DIAGRAM



10G100 ORDERING INFORMATION

PACKAGE TYPE	SPEED (Min 0° to 85° C)
	1.3 GHz
C-Leaded CC	10G100-2C
Leadless CC	10G100-2L
Dice	10G100-2X

LOGIC DIAGRAM



BOOLEAN EQUATIONS

$Sn = An \oplus Bn \oplus Cn$

$P = (A3+B3)(A2+B2)(A1+B1)(A0+B0)$

$\overline{P} = \overline{(A3+B3)(A2+B2)(A1+B1)(A0+B0)}$

$\overline{G} = \overline{A3B3+(A3+B3)A2B2+(A3+B3)(A2+B2)A1B1+(A3+B3)(A2+B2)(A1+B1)A0B0}$

$\overline{Cn+4} = \overline{G0+P0Cn}$; $Cn+4 = G0+P0Cn$

10G100 OPERATION

The operation of the 10G100 is derived from the logic diagram and the Boolean equations on page 2. The 10G100 incorporates a carry output which can be selected active high (Cn+4) or active low ($\overline{Cn+4}$). Cn+4 is applied to the $\overline{Cn}$ input of the higher order Adder in multiple adder implementations using a ripple carry mode. The active high carry output (Cn+4) is the fifth output (M.S.B.) in the case of the most significant adder. Cn+4/$\overline{Cn+4}$ is controlled by Carry Select (Csel) input. Csel low selects $\overline{Cn+4}$ and Csel high selects Cn+4.

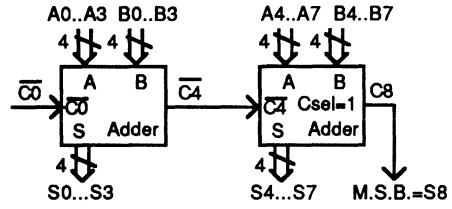
For multiple adder implementations with carry lookahead generators, the 10G100 outputs a carry generate ($\overline{G}$) and a carry propagate (P or $\overline{P}$). $\overline{P}$ output is necessary to drive ECL carry lookahead generators, but P should be used for higher speed with PicoLogic 10G101 carry lookahead generators. A 64-bit adder using the10G100/10G101 is described on page 4. Addition time for this 64-bit adder is reduced from 13.7 ns with ripple carry operations to 3.35 ns with PicoLogic 10G101 carry lookahead generators.
The 10G100 can also perform two's complement subtractions by complementing either the A or B inputs (1's complement) and forcing the lowest order input carry to high ($\overline{C0}$=0).

For compatibility with ECL circuits, the 10G100 allows one set of inputs (A0...A3 or B0...B3) and the input carry ($\overline{Cn}$) to be driven at ECL levels(Vih=-1.0V and Vil=-1.6V). The other set of inputs must be driven at GaAs levels(VIH=-0.7V AND VIL=-1.7V).

RIPPLE CARRY OPERATION

Ripple carry mode is recommended for up to 12 bit additions. It is simpler and faster than the scheme using the 10G101. For an 8 bit adder, typical propagation delay is 1.8 ns (Td1+Td2) for ripple mode versus 2.08 ns (Td5+525+Td2 ; see p. 4 for details) when using the 10G101 carry lookahead generator. In the case of a 12 bit adder, typical propagation delay is longer for ripple mode than when using a 10G101. Nevertheless, when board interconnects are considered, the total propagation delay is may be shorter for ripple mode .

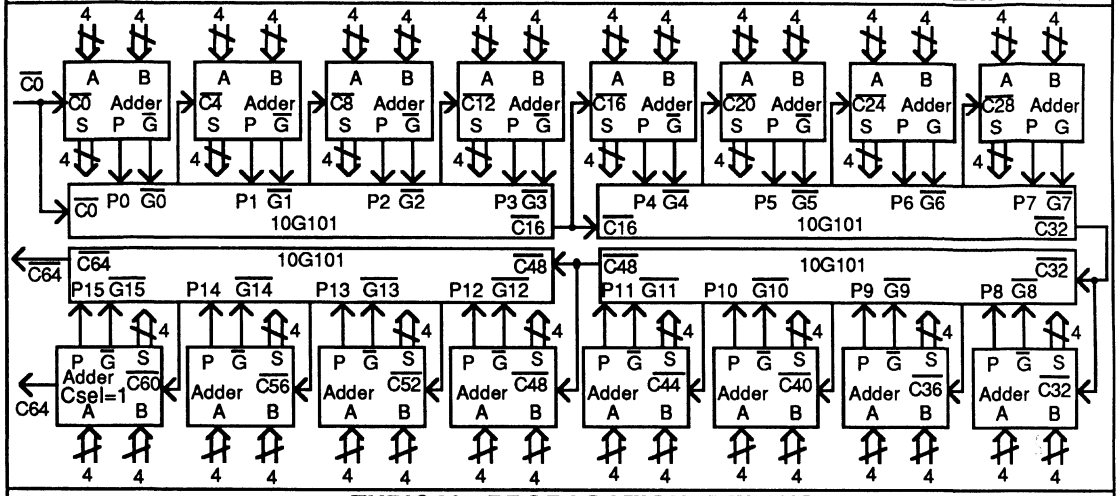
8 BIT ADDER USING A RIPPLE CARRY



PIN DESCRIPTIONS

A0...A3, B0...B3	Data inputs represented as true or complement numbers
$\overline{Cn}$	Carry input (Active Low)
S0...S4	Sum outputs of the Adder
Cn+4/$\overline{Cn+4}$	Carry Output (Active High or Low)
Csel	Carry Select Control . Low selects $\overline{Cn+4}$. High selects Cn+4.
P	Carry Propagate output (Active High)
$\overline{P}$	Carry Propagate output (Active Low)
$\overline{G}$	Carry Generate output (Active Low)
VDDO	Output driver ground pin (0V)
VDDL	Internal logic ground connection (0V)
VSS	-3.4 V power supply
VEE	-5.2 V power supply
VTTC	The AC return pin for the package internal VDDO decoupling capacitor. VTTC is not brought onto the 10G100 circuit, and is typically tied to VTT (nominally -2.0V).
VDCH	Output driver high level clamp voltage. When driving other GaAs devices, VDCH is generally left unconnected. When driving ECL, VDCH may be used to limit VOH. Consult Application Note 4 for detail.
VBB	Reference input to the 10G100's input threshold tracking circuit. Connect to the VBB supplied from ECL when driving the 10G100 from ECL. Must be strapped to the VBBS pin when the 10G100 is driven from PicoLogic. This pin may not be left unconnected.
VBBS	PicoLogic threshold reference output voltage. Connect to VBB when driving from PicoLogic. ΔVBBS/ΔTemp = 0.6mV/°C; ΔVBBS/ΔVSS = 0.2 mV/mV.

64 BIT ADDER USING 10G100&10G101 CARRY LOOKAHEAD GENERATOR



TYPICAL PROPAGATION DELAYS

	Operation	Typical Propagation Delay
a) •	Input signals ready : A, B, $\overline{C0}$ signals to 10G100/10G101	N/A
b) •	Input to Carry Propagate and Carry Generate outputs : A, B, $\overline{C0}$ to P, $\overline{G}$ (10G100)	700ps
c) •	Input to carry output : P, $\overline{G}$ to $\overline{C16}$ (10G101)	525ps
d) •	Carry inputs to carry outputs : $\overline{C16}$ to $\overline{C32}$, $\overline{C32}$ to $\overline{C48}$ and $\overline{C48}$ to $\overline{C64}$ (respectively 2nd, 3rd and 4th 10G101)	3 X 425 = 1275 ps
e) •	Carry input to sum output : $\overline{C48}$ to S (4 most significant 10G100 adders)	850ps
	Total Propagation Delay	3.35ns

FUNCTIONAL DESCRIPTION

a) The carry input $\overline{C0}$ is supplied to the first adder and carry lookahead generator. At the same time the A and B inputs are supplied to all adders.

b) All adders generate the Carry Propagate (P/$\overline{P}$) and the Carry Generate ($\overline{G}$) signals. P is the limiting factor since it takes 700ps to output P compared to 650ps to output $\overline{G}$.

c) The Carry Propagate (P) and Carry Generate ($\overline{G}$) signals are supplied to the 1st 10G101. It takes 525ps for the 10G101 to generate $\overline{C4}$, $\overline{C8}$, $\overline{C12}$ and $\overline{C16}$.

d) $\overline{C16}$ is supplied to the 2nd 10G101 and the 5th adder. Since all the P and G signals have been generated at stage (b) it takes 425ps for the 10G101 to output $\overline{C20}$, $\overline{C24}$, $\overline{C28}$ and $\overline{C32}$. The second group of 4 adders (Adders 5 to 8) then generates the sum outputs. The sum outputs propagation delay is always less than the remaining time to complete the entire 64 addition and, therefore, does not have to be accounted.

Step C is repeated for the third and fourth groups of adders respectively, adders 9 to 12 and adders 13 to 16.

e) After $\overline{C52}$, $\overline{C56}$, $\overline{C60}$, and $\overline{C64}$ have been generated, the sum output of the 4 most significant adders is calculated. The most significant adder should have Csel high to select the active high carry output (C64) for the M.S.B.

DC CHARACTERISTICS

Tc = 0°C to 85°C, VSS = -3.5 V TO -3.3 V, VEE = -5.5 TO -5.1 V, VDDL = VDDO = Gnd. , unless otherwise indicated

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
VIH	Input Voltage High	-0.8		VDDL	V	1
VIL	Input Voltage Low	VSS		-1.8	V	1
ISS	Power Supply Current		300	450	mA	
IEE	Power Supply Current		22	35	mA	
PD	Power Dissipation		1.1	1.7	W	

NOTES:

The remaining DC Characteristics are specified in the 10G PicoLogic™ Family Electrical Characteristics Table at the beginning of this section. This table notes parameter deviations to Family Characteristics and provides specific supplementary characteristics only.

1. One set of inputs (A0...A3 or B0...B3) and the input carry ($\overline{Cn}$) can be driven at ECL levels: VIH min = -1.0 V and VIL max = 1.6 V. The other set of inputs must be driven at GaAs levels as indicated in the above table.

AC CHARACTERISTICS (Note 1)

10G100-2 VSS = -3.5V to -3.3V, VEE = -5.5V to -5.1V, VDDL=VDDO = 0V, unless otherwise indicated.

SYMBOL	PARAMETER	Tc = 0°C		Tc = +25°C			Tc=+85°C		UNITS	NOTES
		MIN	MAX	MIN	TYP	MAX	MIN	MAX		
1/T1	Input frequency	1.3		1.3	1.5		1.2		GHz	
Td1	Delay, $\overline{An}$ or Bn to $\overline{Sn}$ or $\overline{Cn+4}$	500	1200	500	950	1200	550	1250	ps	
Td2	Delay, $\overline{Cn}$ to Sn or $\overline{Cn+4}$	500	1050	500	850	1050	550	1100	ps	
Td3	Delay, An or Bn to $\overline{G}$	400	850	400	650	850	425	900	ps	
Td4	Delay, An or Bn to $\overline{P}$	400	1050	400	800	1050	425	1100	ps	
Td5	Delay, An or Bn to P	400	950	400	700	950	425	1000	ps	
Tr,f	Output rise or fall time		225		175	200		225	ps	2

Notes: 1. Test conditions (unless otherwise indicated) :

VBB = -1.2V — VIH = -0.7V — VDCH = VDDO

VTT = -2.0V — VIL = -1.7V

VTTC = VTT — VOH ≥ -0.7V

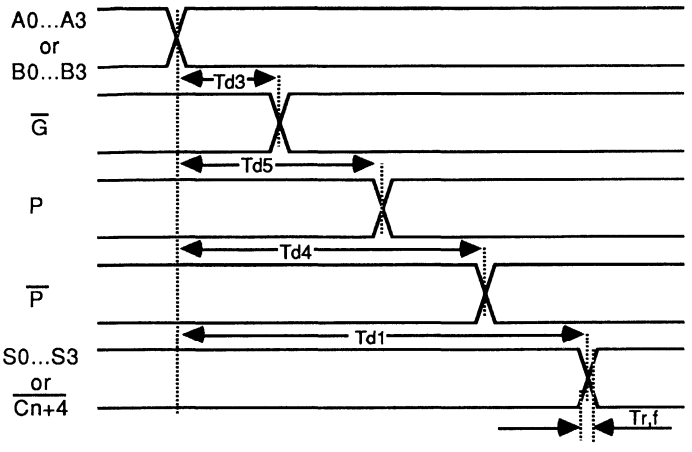
RLOAD = 50Ω to VTT — VOL ≤ -1.7V

Input signal rise and fall time ≤ 150 ps

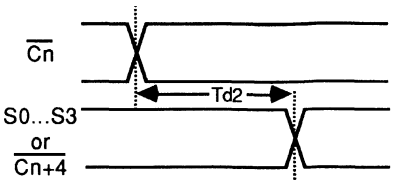
2. Rise and fall times are measured at the 20% and 80% points of the transition from VOL max to VOH min.

SWITCHING WAVEFORMS

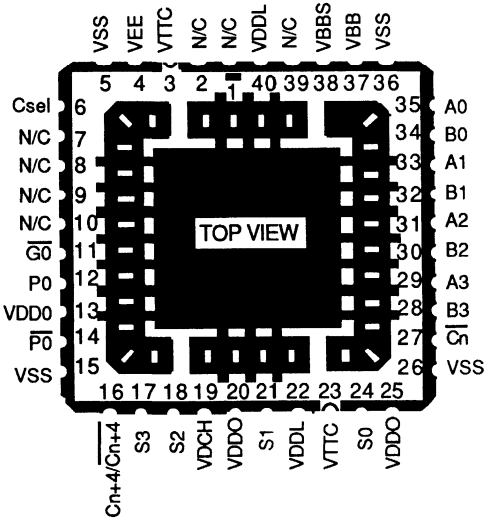
Data in (A0...A3 or B0...B3) to outputs delays



Carry in ($\overline{Cn}$) to Sum outputs (Sn)
or Carry out ($\overline{Cn+4}$) delay



Pin Functions - Type "L" and "C" Packages



GBL GigaBit Logic

10G101

Carry Lookahead Generator
675 ps Propagation Delay / 1.4 GHz
10G PicoLogic™ Family

DISTINCTIVE CAPABILITIES

- Typical input to carry output delay of 525 ps
- 150 ps output rise and fall times
- ECL and 10G PicoLogic™ compatible I/O
- Temperature and voltage compensated using $\overline{V}$BB threshold reference input
- $\overline{P}$ input provided for compatibility with ECL adders
- On chip threshold reference voltage supply (VBBS)
- Available in 40 pin C-leaded, leadless chip carrier or dice form
- Packages contain internal decoupling capacitors for optimum high frequency performance

APPLICATIONS

- Fast carry expander for 10G100 Adder and 10G181 ALU
- Replacement of ECL carry look ahead generators for higher speed performance

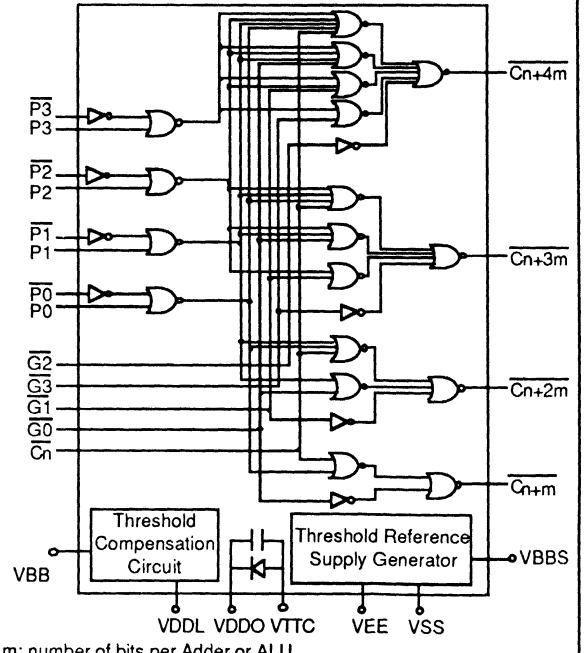
FUNCTIONAL DESCRIPTION

The 10G101 is an ultra-fast carry look ahead generator capable of generating carry outputs in 525 ps (typical delay), four times faster that equivalent ECL carry look ahead generators. The time reduction is even greater for word sizes longer than 16 bits. At room temperature, each additional 10G101 adds only 425 ps to the input to carry output delay. Both polarities of the carry propagate inputs are provided. The P input is used for higher speed with GigaBit's 10G100 adder. The P input is included for direct interface with ECL adders. Speed can be improved by over 30% by replacing 100K ECL carry lookahead generators with the 10G101 in existing ECL adder designs. The 10G101 can process input signals from DC to 1.4 GHz.

For compatibility with other high speed logic families, the 10G101 features the PicoLogic™ family standard VBB input. This input allows the 10G101's threshold voltage to be controlled by the driving logic family. Therefore, mismatches in threshold level due to temperature and power supply variations can be compensated, providing high system noise immunity. An on-chip threshold voltage output (VBBS) is also provided.

The 10G101 is a member of the 10G PicoLogic™ family of GaAs integrated circuits and is fabricated using GigaBit Logic's high volume GaAs MESFET process technology.

LOGIC DIAGRAM

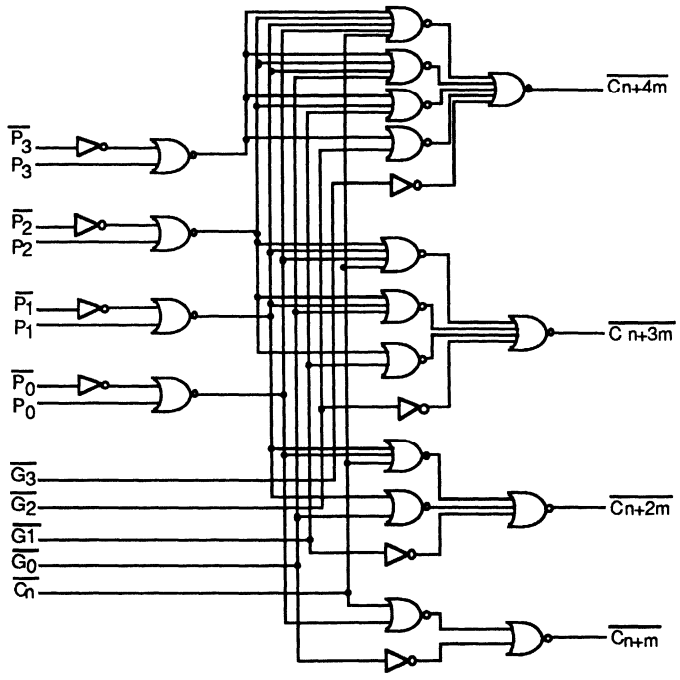


m: number of bits per Adder or ALU

10G101 ORDERING INFORMATION

PACKAGE TYPE	SPEED (Min 0° to 85° C) 1.4 GHz
C-Leaded CC	10G101-2C
Leadless CC	10G101-2L
Dice	10G101-2X

10G101 OPERATION



m: number of bits per Adder or ALU

PIN DESCRIPTIONS

$\overline{G0}$...$\overline{G3}$	Active low carry generate inputs
P0...P3	Active high carry propagate inputs Unused P should be tied up to VTT.
$\overline{P0}$...$\overline{P3}$	Active low carry propagate inputs Unused $\overline{P}$ should be tied up to VDD.
$\overline{Cn}$	Active low carry input
$\overline{Cn+m}$,...$\overline{Cn+4m}$	Active low carry outputs; m is the number of bits per Adder or ALU. For example for the Picologic 10G100, m is equal to 4.
VDDO	Output driver ground pin (0V)
VDDL	Internal logic ground connection (0V)
VSS	-3.4 V power supply
VEE	-5.2 V power supply
VTTC	The AC return pin for the package internal VDDO decoupling capacitor. VTTC is not brought onto the 10G101 circuit, and is typically tied to VTT (nominally -2.0V).
VDCH	Output driver high level clamp voltage. When driving other GaAs devices, VDCH is generally left unconnected. When driving ECL, VDCH may be used to limit VOH. Consult Application Note 4 for detail.
VBB	Reference input to the 10G101's input threshold tracking circuit. Connect to the VBB supplied from ECL when driving the 10G101 from ECL. Must be strapped to the VBBS pin when the 10G101 is driven from PicoLogic. This pin may not be left unconnected.
VBBS	PicoLogic threshold reference output voltage. Connect to VBB when driving from PicoLogic. ΔVBBS/ΔTemp = 0.6mV/°C; ΔVBBS/ΔVSS = 0.2 mV/mV.

10G101 Truth Table and Operations

• $\overline{Cn+4m}$ Output

$$\overline{Cn+4m} = \overline{G3 + P3 \cdot G2 + P3 \cdot P2 \cdot G1 + P3 \cdot P2 \cdot P1 \cdot G0 + P3 \cdot P2 \cdot P1 \cdot P0 \cdot C0}$$

Inputs								Output	Operation
$\overline{Cn}$	$\overline{G0}$	$\overline{P0}$	$\overline{G1}$	$\overline{P1}$	$\overline{G2}$	$\overline{P2}$	$\overline{G3}$ $\overline{P3}$	$\overline{Cn+4m}$	
X	X	X	X	X	X	X	L X	L	Carry generated by the 4th adder.
X	X	X	X	X	L	X	X L	L	Carry generated by the 3rd adder and propagated by the 4th adder.
X	X	X	L	X	X	L	X L	L	Carry generated by the 2nd adder and propagated by the 3rd and 4th adder.
X	L	X	X	L	X	L	X L	L	Carry generated by the 1st adder and propagated by the 2nd, the 3rd and the 4th adder.
L	X	L	X	L	X	L	X L	L	Carry supplied to the 1st adder and propagated by the 1st, the 2nd, the 3rd and the 4th adder.
All other combinations								H	No input carry, no generated carry or no propagated carry.

• $\overline{Cn+3m}$ Output

$$\overline{Cn+3m} = \overline{G2 + P2 \cdot G1 + P2 \cdot P1 \cdot G0 + P2 \cdot P1 \cdot P0 \cdot C0}$$

Inputs						Output
$\overline{Cn}$	$\overline{G0}$	$\overline{P0}$	$\overline{G1}$	$\overline{P1}$	$\overline{G2}$ $\overline{P2}$	$\overline{Cn+3m}$
X	X	X	X	X	L X	L
X	X	X	L	X	X L	L
X	L	X	X	L	X L	L
L	X	L	X	L	X L	L
All other combinations						H

• $\overline{Cn+2m}$ Output

$$\overline{Cn+2m} = \overline{G1 + P1 \cdot G0 + P1 \cdot P0 \cdot C0}$$

Inputs					Output
$\overline{Cn}$	$\overline{G0}$	$\overline{P0}$	$\overline{G1}$	$\overline{P1}$	$\overline{Cn+2m}$
X	X	X	L	X	L
X	L	X	X	L	L
L	X	L	X	L	L
All other combinations					H

• $\overline{Cn+m}$ Output

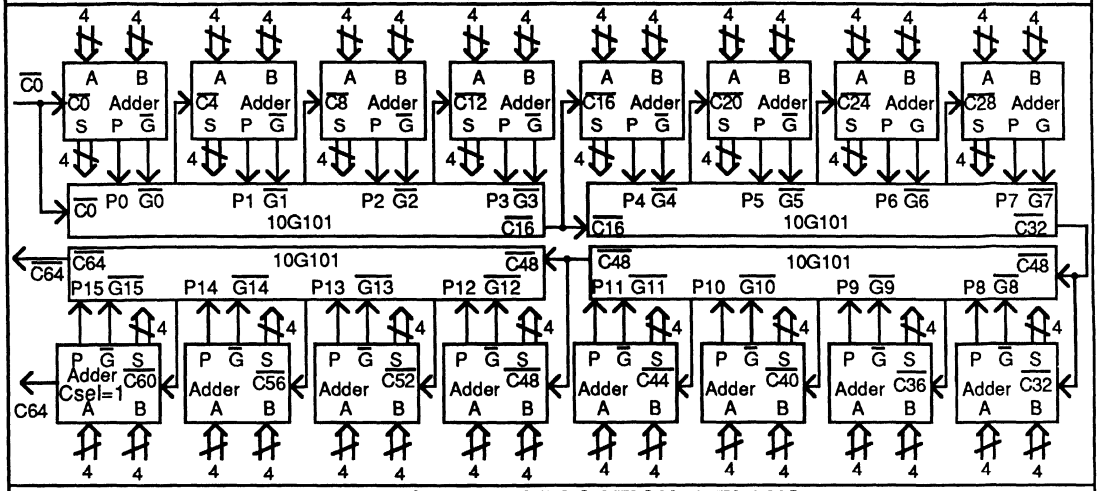
$$\overline{Cn+m} = \overline{G0 + P0 \cdot C0}$$

Inputs			Output
$\overline{Cn}$	$\overline{G0}$	$\overline{P0}$	$\overline{Cn+m}$
X	L	X	L
L	X	L	L
All other combinations			H

Notes :

- H: High voltage level
  L: Low voltage level
  X: don't care
  m: number of bits per adder or ALU
  n: input carry bit number
- $\overline{P}$ is used in the truth tables for compatibility with ECL adders. Truth tables for P (used with 10G100 Adders) can be derived by changing L to H in the P columns.
- Unused P inputs should be tied up to VTT. Unused $\overline{P}$ inputs should be tied up to VDD.

64 BIT ADDER USING 10G100 ADDER&10G101



TYPICAL PROPAGATION DELAYS

	Operation	Typical Propagation Delay
a) •	Input signals ready : A, B, $\overline{C0}$ signals to 10G100/10G101	N/A
b) •	Input to Carry Propagate and Carry Generate outputs : A, B, $\overline{C0}$ to P, $\overline{G}$ (10G100)	700ps
c) •	Input to carry output : P, $\overline{G}$ to $\overline{C16}$ (10G101)	525ps
d) •	Carry inputs to carry outputs: $\overline{C16}$ to $\overline{C32}$, $\overline{C32}$ to $\overline{C48}$ and $\overline{C48}$ to $\overline{C64}$ (respectively 2nd, 3rd and 4th 10G101)	3 X 425 = 1275 ps
e) •	Carry input to sum output : $\overline{C48}$ to S (4 most significant 10G100 adders)	850ps
	Total Propagation Delay	3.35ns

64 BIT ADDER DESCRIPTION

a) The carry input $\overline{C0}$ is supplied to the first adder and carry lookahead generator. At the same time the A and B inputs are supplied to all adders.

b) All adders generate the Carry Propagate (P/$\overline{P}$) and the Carry Generate ($\overline{G}$) signals. P is the limiting factor since it takes 700ps to output P compared to 650ps to output $\overline{G}$.

c) The Carry Propagate (P) and Carry Generate ($\overline{G}$) signals are supplied to the 1st 10G101. It takes 525ps for the 10G101 to generate $\overline{C4}$, $\overline{C8}$, $\overline{C12}$ and $\overline{C16}$.

d) $\overline{C16}$ is supplied to the 2nd 10G101 and the 5th adder. Since all the P and G signals have been generated at stage (b) it takes 425ps for the 10G101 to output $\overline{C20}$, $\overline{C24}$, $\overline{C28}$ and $\overline{C32}$. The second group of 4 adders (Adders 5 to 8) then generates the sum outputs. The sum outputs propagation delay is always less than the remaining time to complete the 64 bit addition and, therefore, does not have to be accounted.

Step C is repeated for the third and fourth groups of adders respectively, adders 9 to 12 and adders 13 to 16.

e) After $\overline{C52}$, $\overline{C56}$, $\overline{C60}$, and $\overline{C64}$ have been generated, the sum output of the 4 most significant adders is calculated. The most significant adder should have Csel high to select the active high carry output (C64) for the M.S.B.

DC CHARACTERISTICS

Tc = 0°C to 85°C, VSS = -3.5 V TO -3.3 V, VEE = -5.5 TO -5.1 V, VDDL = VDDO = Gnd., unless otherwise indicated

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
VBBS	Threshold Reference Voltage		-1.2		V
ISS	Power Supply Current		240	380	mA
IEE	Power Supply Current		18	32	mA
PD	Power Dissipation		910	1460	mW

NOTE:

The remaining DC Characteristics are specified in the 10G PicoLogic™ Family Electrical Characteristics Table at the beginning of this section. This table notes parameter deviations to Family Characteristics and provides specific supplementary characteristics only.

AC CHARACTERISTICS (Note 1)

10G101-2 VSS = -3.5V to -3.3V, VEE = -5.5V to -5.1V, VDDL=VDDO = 0V, unless otherwise indicated.

SYMBOL	PARAMETER	Tc = 0°C		Tc = +25°C			Tc=+85°C		UNITS	NOTES
		MIN	MAX	MIN	TYP	MAX	MIN	MAX		
1/T1	Input frequency	1.4		1.4	1.5		1.4		GHz	
Td1	Carry input ($\overline{Cn}$) or carry generate ($\overline{G}$) to carry outputs	325	575	325	425	575	325	575	ps	
Td2	Active high carry propagate (P) to carry outputs	350	675	350	525	675	350	675	ps	
Td3	Active low carry propagate ($\overline{P}$) to carry outputs	375	700	375	550	700	375	700	ps	
Tr,f	Output rise or fall time		200		150	200		225	ps	2

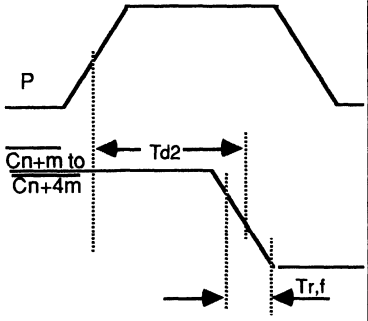
Notes: 1. Test conditions (unless otherwise indicated) :

VBB = -1.2V VIH = -0.7V VDCH = VDDO
VTT = -2.0V VIL = -1.7V
VTTC = VTT VOH ≥ -0.7V
RLOAD = 50Ω to VTT VOL ≤ -1.7V
Input signal rise and fall time ≤ 150 ps

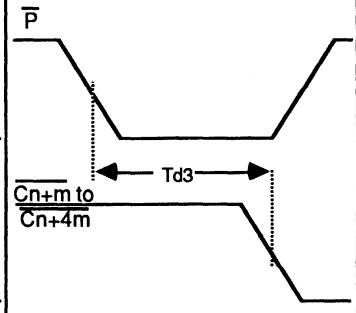
2. Rise and fall times are measured at the 20% and 80% points of the transition from VOL max to VOH min.

SWITCHING WAVEFORMS

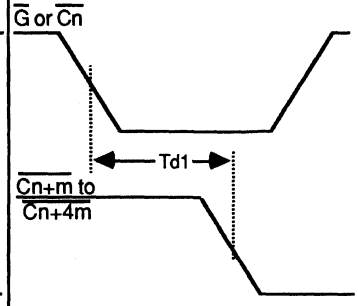
Active high carry propagate to carry outputs.



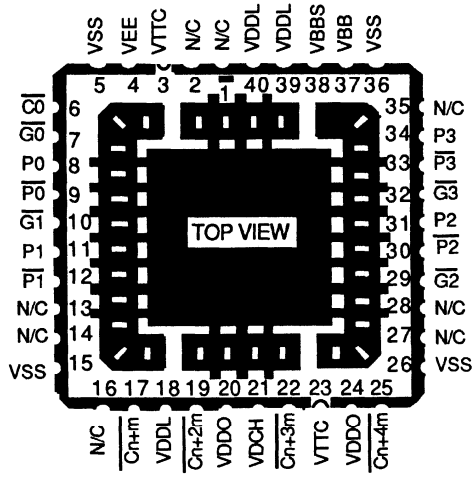
Active low carry propagate ($\overline{P}$) to carry outputs.



Active low carry generate ($\overline{G}$) or carry input ($\overline{Cn}$) to carry outputs.



Pin Functions - TYPE "L" and "C" Packages



GBL GigaBit Logic

10G102
ADVANCE

32-Bit DDS Phase Accumulator
1.0 GHz Clock Rate
10G PicoLogic™ Family

DISTINCTIVE CAPABILITES

- 1 GHz Typical clock frequency
- Less than 20ns freq. switching time
- 32-Bit frequency resolution
- 12-Bit parallel output
- TTL levels for Data and LDSTR inputs
- ECL/PicoLogic levels for Reset and CLK inputs
- ECL and 10G PicoLogic™ output levels
- On- chip 1's complement logic circuits for direct interface to a Quadrant Sine Lookup Table.
- On-chip threshold reference voltage supply (VBBS)
- Temperature and voltage compensated using VBB threshold reference input
- Available in 68 pin leaded chip carrier or die form.

FUNCTIONAL DESCRIPTION

The 10G102 32-Bit Phase Accumulator generates digital sine or cosine functions of very precise frequency when used with an external 14GX048 sine or cosine lookup table ROM. The 10G102 can be used in digital signal processing or in conjunction with a D/A converter to provide high resolution frequency synthesis with virtually instantaneous frequency switching.

The 10G102 maintains a record of phase, which is accurate to 32 bits of resolution. During each clock cycle, Δ-phase stored in the 32 bit input register is added to the previous value of the phase accumulator. The 12 MSBs of the accumulator (Q20-Q31) represent the current phase of the synthesized sine or cosine funtion, and Δ-phase (A0-A31) represents the change in phase at each clock cycle. Δ-Phase sets the output frequency (f0) by the following equation:

$$f0 = \frac{fc \cdot \Delta phase}{2^{32}}$$

where fc=clock frequency, and

$$0 \le \Delta phase \le 2^{32} - 1.$$

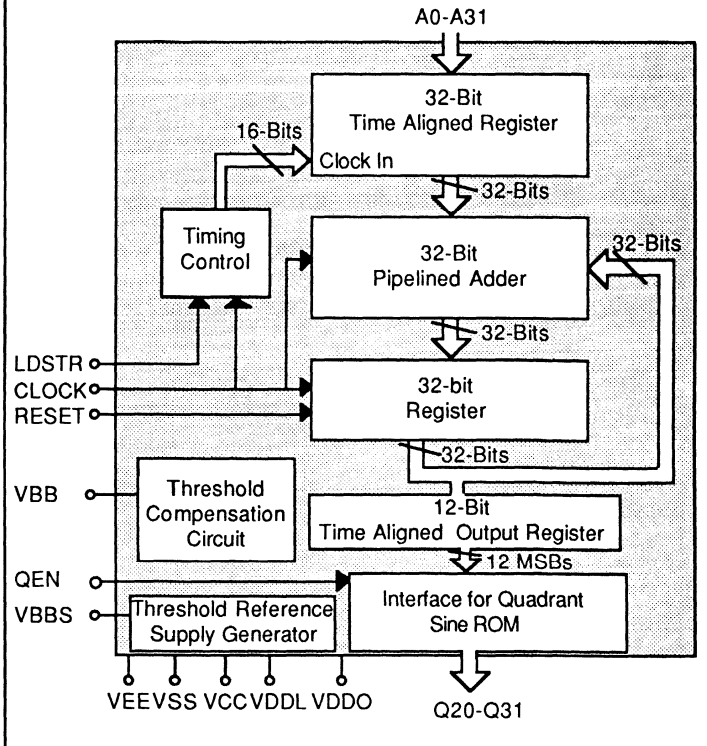
Practically f0 max should be about 40% of fc so that spurious frequency components can be easily filtered.

The switching time of the 10G102 is slightly longer than the pipelining delay (18 clock cycles). At a 1 GHz clock cycle, frequency can be switched in less than 20 ns.

APPLICATIONS

- High frequency digital synthesizers
- High speed frequency hopped sources
- Single sideband converters
- Baseband receivers
- Digital signal processors

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS
Beyond which useful life may be impaired. (Notes 1,4)

SYMBOL	PARAMETER	ABSOLUTE MAXIMUM RATINGS	NOTES
TSTOR	Storage Temperature	- 65 °C to + 150 °C	
TJ	Junction Temperature	- 55 °C to + 150 °C	
TC	Case Temperature Under Bias	- 55 °C to + 125 °C	2
VDDO	Output Driver Supply Voltage	VSS to + 1.0 V	
VSS	Supply Voltage	- 4.0 V to + 0.5 V	
VEE	Supply Voltage	- 7.0 V to VSS + 0.5V	
VIN	Voltage Applied to Any Input; Continuous VSS = - 3.4 V, VEE = - 5.2 V	- 4.0 V to + 0.5 V	
IIN	Current Into Any Input; Continuous	- 0.5 mA to 1.0 mA	
VOUT	Voltage Applied to Any Output	- 4.0V to + 7.0 V	3
IOUT	Current From Any Output; Continuous	-100 mA	
PD	Power Dissipation Per Output POUT = (VDDO-VOUT) x IOUT	100 mW	
VBB	Threshold Reference Input Voltage	-4.0V to +0.5V	
IBB	Input current (from interfacing family)	-0.5 mA to +1.0 mA	
VTT	Load Termination Supply	-6.0 V to VDDO + 6.0 V	
VCC	TTL Supply Voltage	0.0v to 7.0v	

Notes: 1. All voltages specified with VDDL defined as 0 V. Positive current is defined as current into the device.
2. TC is measured at case top. 3. Subject to IOUT and power dissipation limitations.
4. Sustained (>5 secs.) application of VSS in the absence of VEE may result in excessive power dissipation and damage to the device.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN	NOM	MAX	UNITS	NOTES
TC	Case Top Operating Temperature	0	25	85	°C	1
VDDL	Logic Supply Voltage		0		V	
VDDO	Output Driver Supply Voltage	-0.8	0	1.0	V	
VSS	Supply Voltage	- 3.5	- 3.4	- 3.3	V	
VEE	Supply Voltage	- 5.5	- 5.2	- 5.1	V	
VTT	Load Termination Supply Voltage	VSS	- 2.0	-2.0	V	2
RLOAD	Output Termination Load Resistance	25	50	100	Ω	2
VCC	TTL Supply Voltage	4.75	5.0	5.25	V	

DC CHARACTERISTICS (Notes 1,2)
Tc+0°C to +85°C, VSS=-3.5V to -3.3V, VEE=-5.5V to -5.1V, VDDL=VDDO=0V, unless otherwise indicated.

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT	TEST CONDITIONS	NOTES
VOH	Output Voltage High	-0.8	-0.4	-0.3	V		
VOL	Output Voltage Low	-2.0	-1.9	- 1.8	V		
IOH	Output Current High		-70	-60	mA	VOH = -0.8V	3
VIH	ECL/GaAs Input Voltage High	-1.0		VDDL	V		
	TTL Input Voltage High	2.0		VCC	V		
VIL	ECL/GaAs Input Voltage Low			- 1.6	V		
	TTL Input Voltage Low	-0.5		+0.8	V		
IIN	Input Current	-500	100	+500	uA	VIN = -1.0V to -1.6V	
VBBS	Threshold Reference Voltage		-1.2		V		4
IEE	VEE Power Supply Current		120		mA		
ISS	VSS Power Supply Current		1100		mA		
PD	Power Dissipation		4.25		W		

Notes: 1. These characteristics are applicable from DC to 500 MHz.
2. Test conditions unless otherwise indicated: VBB = -1.3V, VTT = -2.0V, Rload = 50Ω to VTT.
3. IOH is the available source follower output current at VOH = -0.8V.
4. Nominally equal to -1.2V with a 40Ω source impedance. The range of VBBS at 25°C is -1.05 t0 -1.4V. ΔVBBS/ΔTemp.=+0.6mV/°C; ΔVBBS/ΔVSS=+0.2 .

AC CHARACTERISTICS (Notes 1,2)

VSS = -3.5V to -3.3V, VEE = -5.5V to -5.1V, VDDL=VDDO = 0V, VCC= 4.75V to 5.25V, unless otherwise indicated.

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
Fc	Clock frequency		1.0		GHz
Tch	Clock high pulse width	350			ps
Tcl	Clock low pulse width	350			ps
Tcr,f	Clock rise and fall times		200		ps
Tsd	Input data setup time		1.0		ns
Thd	Input data hold time (Note 3)		1.0		ns
Tr,f	Output rise and fall times		250		ps
Trw	Reset pulse width		2.0		ns

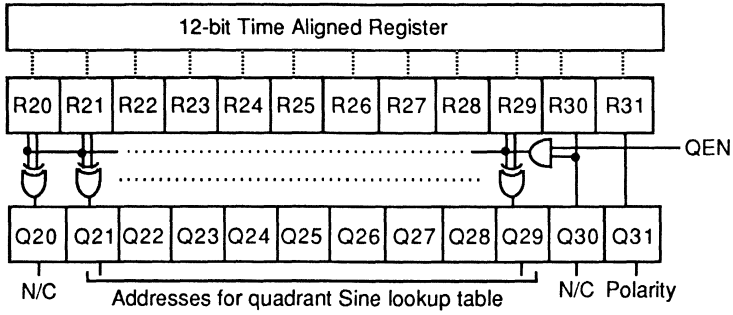
Notes: 1. Test conditions unless otherwise indicated: VBB = -1.2V, VTT = -2.0V, Rload = 50Ω to VTT; CLK/RESET : VIH=-0.7V, VIL=-1.7V; A0...A31/LDSTR : VIH=+2.0V, VIL=+0.8V; VOH≥ -0.7V, VOL≤-1.7V.

2. Output rise and fall time are measured at the 20% and 80% points of transition from Vol max to Voh min.

PIN DESCRIPTIONS

A0...A31	Input Data (TTL levels)
Q20...Q31	Output data (ECL levels)
LDSTR	Load Strobe (TTL levels).When high, LDSTR enables input data A0...A31 to be synchronously loaded in the 32-bit time aligned register.
CLOCK	High speed clock input (ECL levels).
RESET	When high,RESET forces the output of the 32-bit register low (ECL levels).
VDDO	Output driver ground (0V)
VDDL	Internal logic ground connection (0V)
VCC	+5.0 V power supply
VSS	-3.4 V power supply
VEE	-5.2 V power supply
QEN	When high,enables the 1's complement logic to interface directly with a sine lookup table. When low, interface logic is disabled.
VBB	Reference input to the 10G102's input threshold compensation circuit . Connect to VBB supplied from ECL when the 10G102 is driven from ECL. Connect to the VBBS pin when the 10G102 is driven from PicoLogic. This pin may not be left unconnected.
VBBS	PicoLogic™ threshold reference output voltage. Connect to VBB when driving from PicoLogic. ΔVBBS/ΔTemp = 0.6 mV/°C; ΔVBBS/ΔVSS = 0.2 mV/mV.

On Chip 1's Complements To Drive a Sine Quadrant Lookup Table



If QEN is high, then Q30 is XORed with Q20 to Q29 providing the correct addresses to the Quadrant Sine Lookup Table ROM without any external circuitry. If QEN is low, then Q20 to Q31 are the true outputs of the Phase Accumulator.

GBL GigaBit Logic

10G181
ADVANCE

4-Bit Arithmetic Logic Unit/Function Generator 2.0 ns Add Time

10G PicoLogic™ Family

DISTINCTIVE CAPABILITIES

- 150 ps typical output rise and fall times
- 700 mw typical power dissipation
- ECL and 10G PicoLogic compatible I/O
- VBB reference input for improved threshold tracking over temperature and power supply variation
- On chip VBBS (-1.2V) reference voltage supply
- 2.0 ns add time
- Available in leaded, leadless chip carrier or dice form
- Packages contain internal decoupling capacitors for optimum high frequency performance

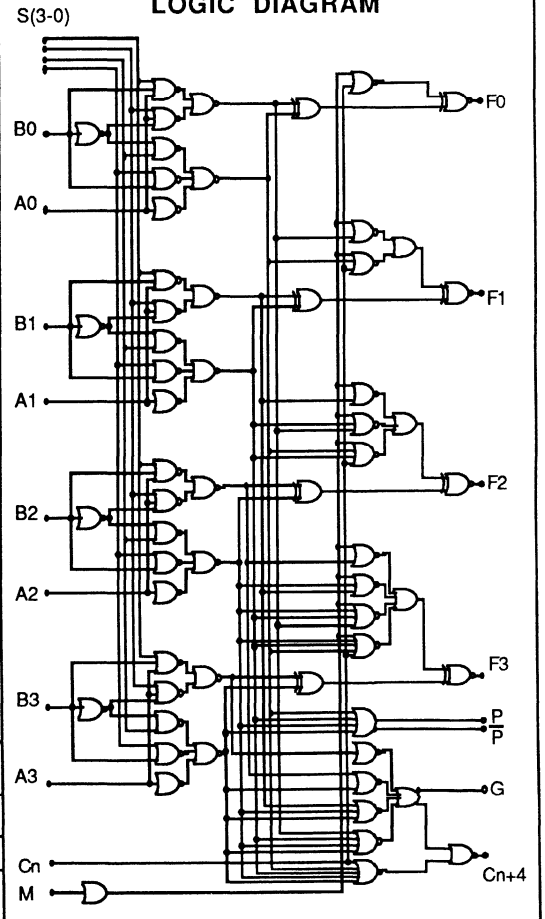
FUNCTIONAL DESCRIPTION

The 10G181 is an ECL or PicoLogic compatible ultra fast arithmetic logic unit capable of performing 16 logic functions and 16 arithmetic operations on two 4-bit words. The 10G181 performs a 4 bit add function with carry in 2.0 ns and exhibits 700 mW power dissipation.

The mode control input, M, selects the logic or arithmetic mode operation for the two 4 bit inputs, A(0-3) and B(0-3). The desired function can be selected applying the appropriate binary pattern on the select, S(0-3), inputs. When the mode control input is high, all the internal carries are inhibited and the device performs logical operations on the individual bits as listed. The device incorporates full internal carry look ahead & provides for both ripple carry using the Cn+4 output or for carry look ahead between packages using the carry propagate P, carry propagate complement $\overline{P}$, and carry generate G, signals.

The 10G181 is fabricated using GigaBit's production proven GaAs MESFET process technology.

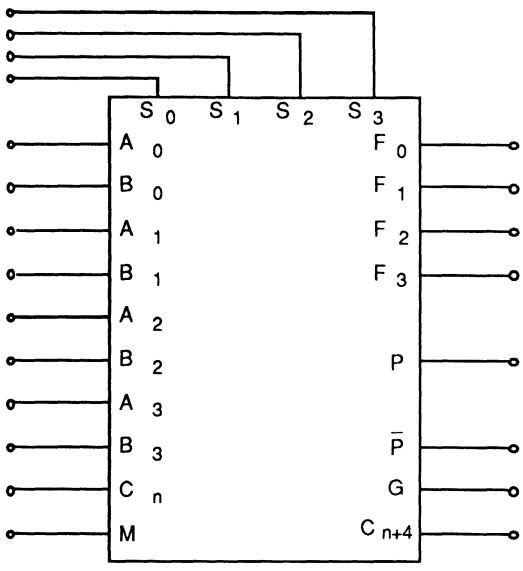
LOGIC DIAGRAM



10G181 ORDERING INFORMATION

PACKAGE TYPE	DELAY (Max. @ 25°C)
	2.0 ns
Leaded Chip Carrier	10G181-2C
Leadless Chip Carrier	10G181-2L
Dice	10G181-2X

BLOCK DIAGRAM



Positive logic: High level = '1'

FUNCTIONAL DESCRIPTION (cont.)

When the mode control input is low, the carries are enabled and the device performs arithmetic opeations. Note that the functional truth table shows P, $\overline{P}$, and G are not affected by carry-in.

For most applications where Gallium Arsenide is required, the carry look ahead unit, 10G101 should be used to fully utilize the capabilities of the technology. The 10G101 can support up to four 10G181's.

The function table lists the arithmetic operations without carry in. An incoming carry, Cn, adds one to each operation. For example, with carry in, Cn = 1, the output function, F = A - 1 becomes F = A - 1 + 1 = A - 0. All subtraction is carried out in complementary addition (1's complement). A carry out, Cn+4, means borrow; thus a carry out is generated (Cn+4 = 1) when there is under flow.

In the add mode, P indicates that F is 15, while G indicates F is 16 or more. In the subtract mode, P indicates that F is zero, while G indicates F is less than zero.

FUNCTIONAL TRUTH TABLE

Function Select S3 S2 S1 S0	Logic Functions M is High Cn is X F	Arithmetic Operation M is Low Cn is low F
L L L L	$F = \overline{A}$	F = A
L L L H	$F = \overline{A} + \overline{B}$	F = A plus (A • $\overline{B}$)
L L H L	$F = \overline{A} + B$	F = A plus (A • B)
L L H H	F = Logical "1"	F = A times 2
L H L L	$F = \overline{A \cdot B}$	F = (A + B) plus 0
L H L H	$F = \overline{B}$	F = (A + B) plus(A • $\overline{B}$)
L H H L	$F = A \odot B$	F = A plus B
L H H H	$F = A + \overline{B}$	F = A plus (A + B)
H L L L	$F = \overline{A} \cdot B$	F = (A + $\overline{B}$) plus 0
H L L H	$F = A \oplus B$	F = A minus B minus 1
H L H L	F = B	F = (A + $\overline{B}$) plus (A • B)
H L H H	F = A + B	F = A plus (A + $\overline{B}$)
H H L L	F = Logical " 0"	F = minus 1 (two's complement)
H H L H	$F = A \cdot \overline{B}$	F = (A • $\overline{B}$) minus 1
H H H L	F = A • B	F = (A • B) minus 1
H H H H	F = A	F = A minus 1

PIN DESCRIPTIONS

S(0-3)	Function select pins
M	Mode select
A(0-3)	A word operand inputs
B(0-3)	B word operand inputs
Cn	Carry input
Cn+4	Carry output
P	Carry look ahead propagate
$\overline{P}$	Carry look ahead propagate complement
G	Carry look ahead generate
F(0-3)	Function outputs
VEE	- 5.2 V. Power supply
VSS	- 3.4 V. Power supply

VTTC	Internal VDDO decoupling capacitor return pin. VTTC is bought into the 10G181 package as the AC return lead for the VDDO output driver decoupling capacitor. It is not brought on to the 10G181 die: VTTC is typically tied to VTT (-2.0V).
VBB	Input to the 10G181 input threshold tracking circuit. Connect to threshold voltage supplied from ECL if driven by ECL. Connect to VBBS when 10G181 is driven by PicoLogic™.
VBBS	Nominal -1.2V threshold reference output supply voltage (40Ω source impedence). Connect to VBB when 10G181 is driven by PicoLogic™.
VDDO	Ground connection for output drivers.
VDDL	Ground connection for input buffers & internal switching logic.

10G181 AC CHARACTERISTICS

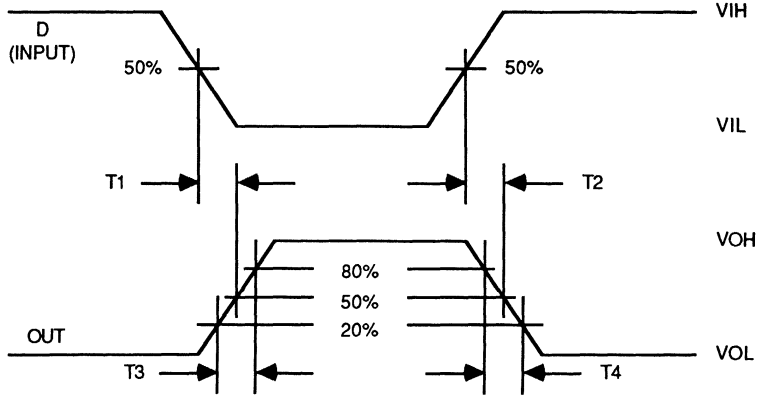
VSS = - 3.5V to- 3.3V, VEE = -5.5V to - 5.1V, VDDL = VDDO = Gnd., unless otherwise indicated

SYMBOL	PARAMETER	TC = 0°C		TC = +25°C			TC = 85°C		UNITS	NOTES
		Min	Max	Min	Typ	Max	Min	Max		
A(0-3) to F(0-3)	Propagation Delay				2.0				ns	
B(0-3) to F(0-3)	Propagation Delay				2.0				ns	
Cn to F(0-3)	Propagation Delay				TBD					
Cn to C n+4	Propagation Delay				TBD					
S(0-3) to F(0-3)	Propagation Delay				2.4				ns	
M to F(0-3)	Propagation Delay				1.6				ns	
B(0-3) to G	Propagation Delay				TBD					
A(0-3) to P	Propagation Delay				TBD					
A(0-3) to G	Propagation Delay				TBD					
B(0-3) to P	Propagation Delay				TBD					

Notes:

1. Test conditions (unless otherwise indicated):
   VBB = - 1.2V VIH = - 0.7V
   VTT = - 2.0V VIL = - 1.7V
   VTTC = VTT VOH≥ - 0.7V
   RLOAD = 50Ω to - 2.0V VOL ≤ - 1.7V
   Input signal rise and fall time ≤ 150 ps
2. Rise and fall times are measured at the 20% and 80% points of the transition from VOL max to VOH min.

SWITCHING WAVEFORMS



DC CHARACTERISTICS

Tc = 25°C, VSS = -3.5 V TO -3.3 V, VEE = -5.5 TO -5.1 V, VDDL = VDDO = Gnd, unless otherwise indicated

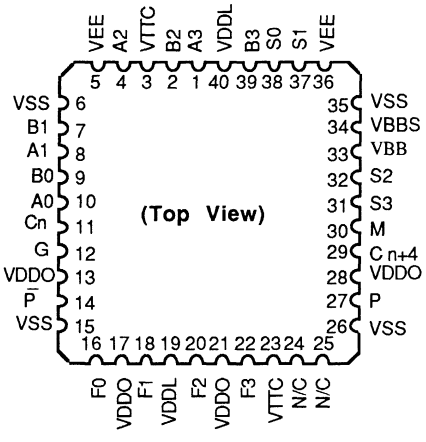
SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
VBBS	Threshold Reference Voltage		-1.2		V
ISS	Power Supply Current		165		mA
IEE	Power Supply Current		55		mA
PD	Power Dissipation		850		mW

NOTE:

The remaining DC Characteristics are specified in the 10G PicoLogic™ Family Electrical Characteristics Table at the beginning of this section. This table notes parameter deviations to Family Characteristics and provides specific supplementary characteristics only.

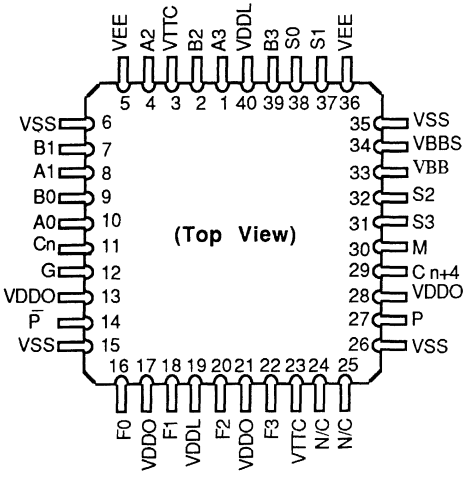
PACKAGE PINOUT DIAGRAMS

TYPE "L" PACKAGE



NOTES: Pin 1 is marked for orientation. N/C = No Connection.

TYPE "C" PACKAGE



NOTES: Pin 1 is marked for orientation. N/C = No Connection.

12G & 14G FAMILY MEMORY PRODUCTS

TABLE OF CONTENTS

256x4 Bit Registered, Self-Timed Static RAM 2.5 ns Cycle Time

12G NanoRam™ Family

DISTINCTIVE CAPABILITIES

- Nanosecond access and cycle times
- Fully registered architecture with 3 selectable output modes provides maximum usable speed
- Equal read and write cycle times
- Internally generated write pulse eliminates need for narrow write pulse
- Register mode output for fast access with minimum cycle time
- Latch mode output for fast access with extended cycle
- Single-ended or differential clock input
- ECL and 10G PicoLogic™ Family compatible
- Temperature & voltage compensated
- Source follower outputs permit wire-or capability
- Available in C-leaded or leadless chip carriers or in unpackaged dice form

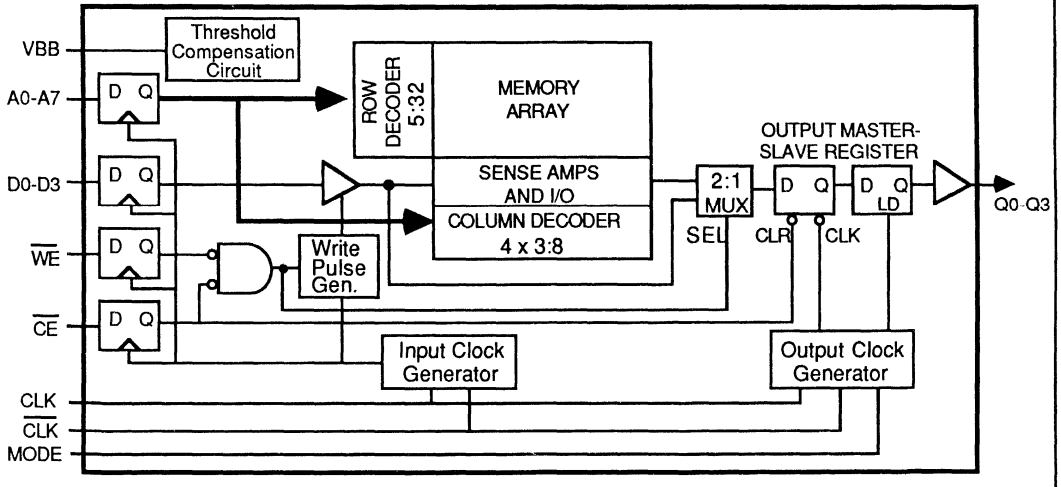
FUNCTIONAL DESCRIPTION

The 12G014 is an ultra-high speed 1024 bit synchronous, registered Random Access Memory, organized as 256 words by 4 bits. The device is designed for ultra- high speed cache and buffer storage applications. The innovative architecture of the NanoRam™ Family incorporates the functions of a traditional static RAM along with on-chip, fully pipelined, latched inputs and outputs, an internally generated write pulse, and a single clock to deliver maximum usable device speed in system applications.

The 12G014 RAM input and output levels are ECL and 10G PicoLogic Family compatible. A VBB input pin is provided for direct voltage and/or temperature compensation tracking with ECL interface circuitry. The device has source follower outputs to allow simple wire-OR expansion.

The 12G014 is packaged in a JEDEC outline leadless or C- leaded chip carrier and is fabricated using GigaBit's high volume GaAs MESFET process technology.

BLOCK DIAGRAM



12G014 ORDERING INFORMATION

PACKAGE TYPE	Register Mode R/W Cycle Time		Prototyping & Production Support Products
	2.5 ns	3.5 ns	
C-leaded chip carrier	12G014-2C	12G014-3C	90GKIT-40 - High Speed Prototyping Kit
Leadless chip carrier	12G014-2L	12G014-3L	90GSKT-40L - high speed socket for kit
Unpackaged dice		12G014-3X	90GHS40A/B - heatsinks

SYMBOL	PIN DESCRIPTIONS
A0 - A7	Address inputs: Lines A0 - A2 are column addresses. Lines A3 - A7 are row addresses. At the rising edge of Clock these lines determine the memory address state information.
$\overline{CE}$	Chip Enable: At the rising edge of Clock this line determines the enable state of the device. Chip Enable LOW activates the function and output of the memory. Chip Enable HIGH deactivates the memory and its output.
$\overline{WE}$	Write Enable: At the rising edge of CLOCK this line determines the read or write state of the device. Write Enable HIGH activates a read cycle. Write Enable LOW activates a self-timed write cycle.
CLK	Clock Input True: provides the basic timing of the memory device. All inputs are latched on the rising edge of Clock which defines the initiation of a new memory cycle.
$\overline{CLK}$	Clock Input Complement: provides an optional differential input for systems with differential Clock distribution. For single ended Clock distribution, $\overline{CLK}$ is tied to the Vbb input pin (nom. -1.3V).
MODE	Mode: sets the output mode of the device. When the Mode pin is tied to Vss the output operates in the Register Mode. When the Mode pin is tied to Vddl the output operates in the Latch Mode. When the Mode Pin is tied to Vcc the output operates in the Transparent Mode.
D0 - D3	Data In: at the rising edge of Clock during a Write Cycle these lines determine the data input state information to be written into the addressed memory location.
Q0 - Q3	Data Out: these lines provide the valid data output from a Read Cycle and input data written from a Write Cycle. In the Register Mode, the pipelined Data Out is activated by the rising edge of Clock. In the Latch Mode, the non-pipelined Data Out is activated by the falling edge of Clock.
VCC	VCC: + 5.0 Volt power supply pin.
VDDL	VDDL: ground supply pin for the memory circuitry.
VDDO	VDDO: ground supply pin for the output drivers.
VSS	VSS: - 3.4 Volt power supply pin
VEE	VEE: - 5.2 Volt power supply pin.
VTTC	VTTC: the AC return pin for the package internal Vddo decoupling capacitor. Vttc is not brought onto the 12G014 circuit, and is typically tied to Vtt (nominally -2.0V).
VBB	VBB: ECL Threshold Reference Voltage Input (Nominal - 1.3 V) provided to allow direct tracking of an ECL logic family's Vbb reference voltage. Must be tied to a nominal - 1.3 V when interfacing to 10G PicoLogic circuitry (or to the VBBS supply pin of a PicoLogic device).
DNC	DNC: Do Not Connect. Reserved for future use.

DEVICE DESCRIPTION

NanoRam Architecture

The NanoRam architecture provides a fully registered, clocked, static memory operation. This architecture is optimized for ultra high speed memory applications requiring nanosecond access and cycle times. A single clock establishes the simple synchronous timing for the device. The rising edge of Clock determines the start of each memory cycle and controls the registered inputs and outputs.

Registered Inputs

All input state information, including Addresses, Write Enable, Chip Enable, and Data In are latched into the on-chip pipeline registers at the rising edge of Clock to begin a new cycle. The setup times and hold times relative to the rising edge of Clock are the same for all inputs and controls. Once the input and control signals have been latched on-chip, they may begin transition to another state for the next cycle. This allows considerable time for address and control signals to propagate across an array of memory devices without slowing the memory cycle timing.

Output Modes

The MODE pin determines the function of the 12G014's output register. When the MODE pin is strapped to Vss, the output operates in the fully pipelined REGISTER MODE. In this mode, the Data Out remains valid for the entire memory cycle and transitions only at the next rising edge of the Clock. This allows sufficient time for the data output signals to propagate across an array of memory devices without slowing memory cycle timing. Register Mode operation offers the fastest possible cycle time operation of the NanoRam memory in a system application.

When the Mode pin is strapped to Vddl, the output operates in the Latch Mode. In this mode, the non-pipelined Data Out is fed through on the falling edge of Clock in the current cycle and latched on the next rising edge of Clock. This allows the data output to appear without waiting for the next rising edge of Clock. Latch Mode operation offers the flexibility to achieve the fastest possible memory access time with output latches in system applications with extended cycle time.

When the Mode Pin is strapped to Vcc, the output operates in the Transparent Mode. In this mode, the data from the memory array appears at the output pins as soon as it is available from the memory array through the sense amplifiers. The input registers are unaffected by the state of the Mode Pin, with the rising edge of the clock loading them and starting the memory cycle.

For all modes of operation during write cycles, the data being written is also routed directly from the data input register to the output register where it appears as valid data out. This simplifies system design by eliminating the appearance of invalid or indeterminate states on the output pins. The Data Out drivers are source followers to allow wire-OR configurations.

Output Master/Slave Register Operation

The output M/S register is controlled by the Clock and the Mode control and operates as follows:

Mode C'ntl	Master Reg.	Slave Reg.
= Vss (Register)	Transparent when clock is low	Transparent when clock is high
= Vddl (Latch)	" " "	Always transparent
= Vcc (Transparent)	Always transparent	Always transparent

Clock Options

The Clock input is differential to provide optimum sensitivity and noise immunity. If it is driven from a single-ended clock source, the $\overline{CLK}$ input must be tied to a nom. -1.3V reference. This reference voltage is available on pin VBBS if a PicoLogic device is used to drive the Clock input. All specifications in this data sheet assume the rising edge of CLK as the active edge. If $\overline{CLK}$ is used instead (with CLK tied to a nom. -1.3V source), all timimg diagrams should be referenced to the clock edge opposite to that shown. The sum of Clock high and Clock low pulse widths is considerably less than total cycle time allowing ample time for clock transitions in practical systems. The Clock duty cycle may be asymmetrical within the limits allowed by the minimum clock pulse width specifications.

ECL and PicoLogic Family Compatibility

All 12G014 inputs are ECL and PicoLogic I/O level compatible. The Vbb input pin allows the input logic threshold to be controlled by the driving logic family, thereby compensating for mismatches in threshold due to temperature and power supply variation, resulting in high system noise immunity. If PicoLogic is used to drive the 12G014, the Vbb pin should be connected to the VBBS pin of a driving PicoLogic device. If the 12G014 is driven from ECL logic, the Vbb pin should be connected to the VBB threshold reference voltage derived from the driving ECL logic family.

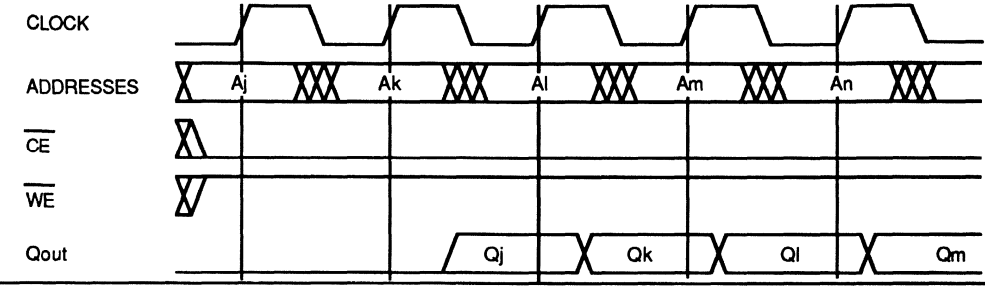
Power Supply Sequencing

Power to the device should be applied first to Vee and then to Vss and Vcc. When powering down, power should first be removed from Vss and Vcc, then from Vee. During power up and power down sequencing, the absolute maximum ratings apply.

DEVICE DESCRIPTION

Register Mode Read Cycle

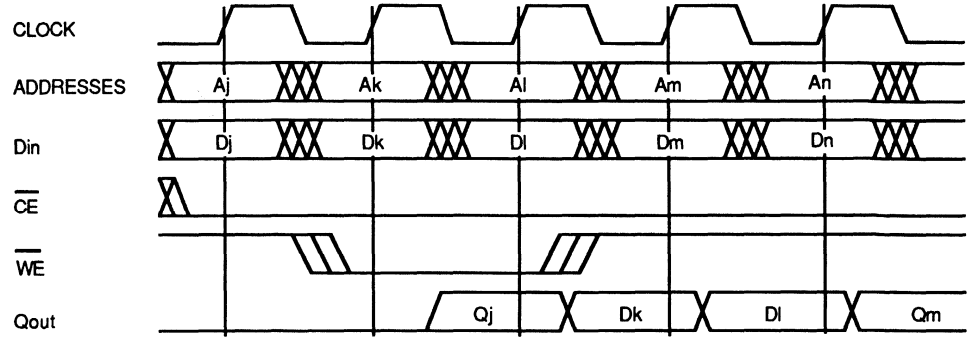
The MODE pin is strapped to Vss for all Register Mode operations. The Read Cycle in the Register Mode is performed by presenting a Write Enable ($\overline{WE}$) HIGH and valid Addresses to the input registers prior to the rising edge of Clock. The Jth memory access takes place during the present Clock cycle and valid Jth cycle read data is presented to the on-chip output registers. At the next rising edge of Clock the Kth memory cycle is started and the valid Jth cycle read data is loaded into the output registers, propagates through the output drivers and appears at Data Out where it is held for a full cycle. Successive Read Cycles proceed in a fully pipelined manner where each rising edge of Clock loads the input registers with the valid state for the present memory cycle while the output registers are loaded with read data from the previous cycle.



Register Mode Write Cycle

The MODE pin is strapped to Vss for all Register Mode operations. The Jth Write Cycle in the Register Mode is performed by presenting a Write Enable ($\overline{WE}$) low and valid Addresses to the input registers prior to the rising edge of Clock. No write pulse is required. The Jth memory write takes place totally self-timed during the present Clock cycle and valid Jth cycle write data is presented to the on-chip output registers. At the next rising edge of clock, the Kth memory cycle is started and valid Jth cycle write data is loaded into the output registers and appears at the Data Out pins where it is held for a full cycle. Successive Write Cycles proceed in a fully pipelined manner with each successive rising edge of Clock.

Write Cycles have timing parameters identical to Read Cycles. Any combination of Read Cycles and Write Cycles can be performed in succession with identical pipelined timing.



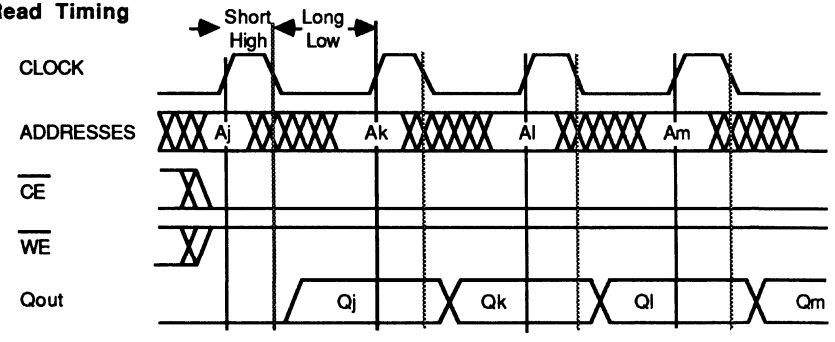
DEVICE DESCRIPTION

Latch Mode Read and Write Cycles

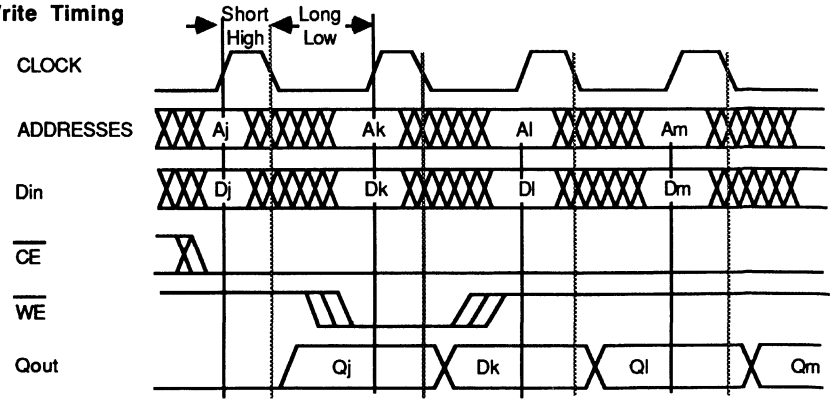
The MODE pin is strapped to Vddl for all Latch Mode operations. The Jth read cycle in Latch Mode is performed by presenting the same pipelined inputs prior to the rising edge of Clock as for the Register Mode read cycle. The Jth memory access takes place during the present clock cycle. At the falling edge of Clock within the cycle, the output latch becomes transparent and allows valid Jth cycle read data to appear at Data Out. At the next rising edge of Clock, the Kth memory cycle is started and valid Jth cycle read data is held until the next falling edge of Clock. Latch Mode operation is typically used to achieve a fast access time in applications with extended cycle times. To achieve the fastest possible access time in Latch Mode, the Clock is operated asymmetrically. The clock is held HIGH for a minimum time and brought LOW to allow valid read data from the present cycle to appear at Data Out as soon as possible. The Clock is then held LOW for the remainder of the extended cycle.

The Kth Write Cycle in Latch Mode is performed by presenting the same pipelined inputs prior to the rising edge of Clock as for the Register Mode Write Cycle. Valid Kth cycle write data appears at Data Out at the falling edge of Clock in the present cycle. At the next rising edge of Clock the Lth memory cycle is started and valid Kth cycle write data is held until the next falling edge of Clock. Latch Mode Write Cycles have timing parameters identical to Latch Mode Read Cycles. Any combination of Read Cycles and Write Cycles can be performed in succession with identical timing.

Latch Mode Read Timing



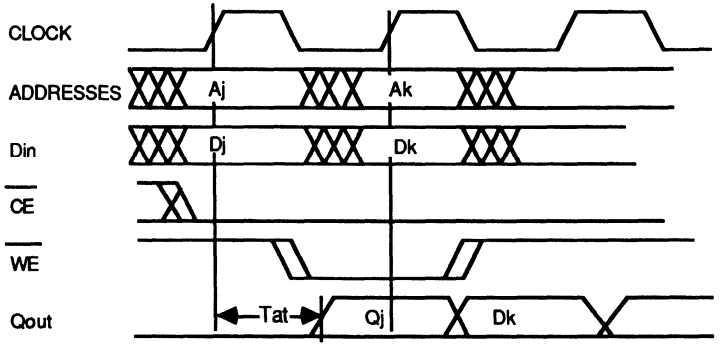
Latch Mode Write Timing



DEVICE DESCRIPTION

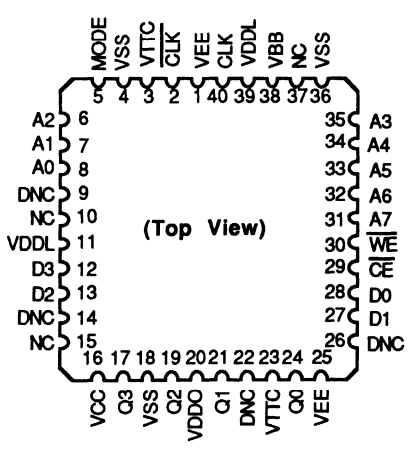
Transparent Mode Read and Write Cycles

The MODE pin is strapped to Vcc for all transparent mode operations. The Jth read or write cycle is performed by presenting the appropriate Write Enable signal and valid addresses to the input registers prior to the rising edge of Clock. No write pulse is required during a write operation. The Jth memory cycle takes place during the present Clock cycle and valid read or write data is presented to the output pins through the output registers which are held transparent in this mode. Successive cycles are initiated with each subsequent rising clock edge.



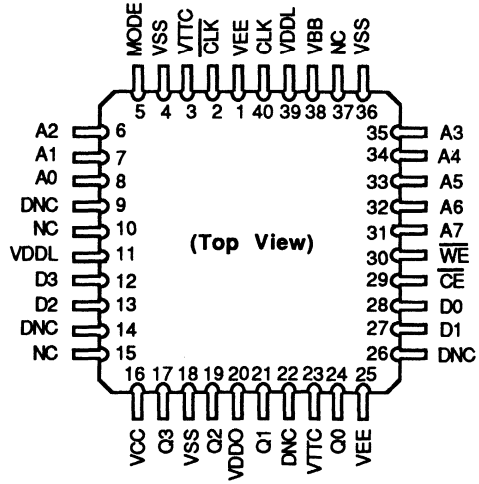
PIN FUNCTION DIAGRAMS

PACKAGE TYPE "L"



NOTES: Pin 1 is marked for orientation. N/C = No Connection. DNC = do not connect.

PACKAGE TYPE "C"



NOTES: Pin 1 is marked for orientation. N/C = No Connection. DNC = do not connect.

ABSOLUTE MAXIMUM RATINGS (Notes 1, 5)

(Beyond which useful life may be impaired)

SYMBOL	PARAMETER	ABSOLUTE MAXIMUM RATINGS	NOTES
Tstor	Storage Temperature	- 65 °C to + 150 °C	
Tj	Junction Temperature	-55 °C to + 150 °C	
Tc	Case Temperature Under Bias	-55 °C to + 125 °C	2
Vcc	Supply Voltage	- 0.5 V to + 6.0 V	
Vddo	Output Driver Supply Voltage	Vss to + 1.0 V	
Vbb	ECL Reference Voltage	-4.0 V to +0.5 V	
Ibb	Input current (from interfacing family)	-0.5 mA to +1.0 mA	
Vss	Supply Voltage	- 4.0 V to + 0.5 V	
Vee	Supply Voltage	- 7.0 V to Vss - 1.0 V	
Vin	Voltage Applied to Any Input; Continuous Vcc = 5.0, Vss = - 3.4 V, Vee = - 5.2 V	- 4.0 V to + 0.5 V	
Iin	Current Into Any Input; Continuous	- 0.5 mA to 1.0 mA	
Vout	Voltage Applied to Any Output	- 4.0V to +7.0 V	3
Iout	Current From Any Output; Continuous	-100 mA	3
Pd	Total Power Dissipation Tc = 85° C	3.9 W	4
Pout	Power Dissipation Per Output Pout = (Vddo-Vout) x Iout	100 mW	
Vttc	Vddo Internal Decoupling Cap. Return	- 6.0 V to Vddo	
Vtt	Load Termination Supply	- 6.0 V to Vddo + 6.0 V	3

NOTES:
1. All voltages specified with Vddl defined as 0 V. Positive current flows into the device.
2. Tc is measured at case top.
3. Subject to power dissipation limitations.
4. Total power dissipation is the limit of the package power dissipation. The operating power dissipation of the device is specified under DC Characteristics.
5. Sustained application of Vss or Vcc in the absence of Vee may result in excessive power dissipation and damage to the device.

RECOMMENDED OPERATING CONDITIONS (Note 1)

SYMBOL	PARAMETER	MIN	NOM	MAX	UNITS	NOTES
Tc	Case Operating Temperature	25		85	°C	3
Vcc	Supply Voltage	4.75	5.0	5.25	V	
Vddl	Logic Supply Voltage		Gnd		V	
Vddo	Output Driver Supply Voltage	-0.8	Gnd	1.0	V	
Vbb	ECL Reference Voltage		- 1.3		V	
Vss	Supply Voltage	- 3.6	- 3.4	- 3.2	V	
Vee	Supply Voltage	- 5.5	- 5.2	- 4.9	V	
Vttc	Vddo Internal Decoupling Return	Vss	Vtt	Vddo	V	
Vtt	Load Termination Supply Voltage	Vss	- 2.0	- 1.8	V	2
Rload	Output Termination Load Resistance	25	50	100	Ω	2

NOTES:
1. All voltages are specified with respect to Vddl and Vddo, which are grounded.
2. The Rload and Vtt combination used is subject to maximum output current and output power restrictions.
3. This operating temperature can be maintained with a heat sink and air flow as determined by using Application Note 3. Tc measured at case top. ***HEATSINKING IS REQUIRED.***

DC CHARACTERISTICS (note 5)

TEST CONDITIONS: Tc =25 °C to 85 °C, VCC = 4.75 to 5.25V, VSS = -3.6V to -3.2V, VEE = -5.5V to -4.9V, VDDL=VDDO = Gnd, Output load = 50Ω to VTT = - 2.0 V, clock input edge rate ≤ 2 ns.

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	TEST CONDITIONS	NOTES
Voh	Output Voltage High	- 0.7	-0.4	-0.3	V		
Vol	Output Voltage Low	Vtt	-1.9	- 1.8	V		
Ioh	Output Current High		-70	-60	mA	Voh = - 0.7 V	1
Iol	Output Current Low		0.01	10	µA	Vol = -1.8V	
Vih	Input Voltage High	- 1.0		Vddl	V	Vbb = - 1.3 V	2
Vil	Input Voltage Low	-2.0		- 1.6	V	Vbb = - 1.3 V	2,3
Iin	Logic Input Current	-100	10	100	uA	-1.8 V ≤ Vin ≤ -0.7 V	
Imode	Mode Input Current			1.0	mA	Vss ≤ Vmode ≤ Vcc	
Ibb	Vbb Input Current	-500		500	uA	Vbb = -1.3 V	
Iss	Power Supply Current	-460	-290		mA		
Iee	Power Supply Current	-140	-100		mA		
Icc	Power Supply Current		160	200	mA		
Pd	Power Dissipation		2.3	3.3	W		4

NOTES:

1. Ioh is the maximum current the output can source under any Rload and Vtt combination.
2. The input threshold is referenced to the Vbb input. Therefore Vih and Vil will track the Vbb input.
3. Inputs may be connected to Vss (-3.4V) to establish a logic low level.
4. Measured at nominal supply voltages and 50% output duty cycle. Excludes Vddo output source follower power (typically 10 mW per loaded output).
5. For proper operation, the clock input edge rate should be ≤ 2 ns.

12G014 - 2 AC CHARACTERISTICS (Note 1)

Test Conds.: Tc = 25°C to 85°C, VCC = 4.75 to 5.25, VSS = -3.6V to -3.2V, VEE = -5.5V to -4.9V, VDDL=VDDO = Gnd.

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
ALL MODES, READ AND WRITE CYCLES						
Tclkh	Clock High Pulse Width	1000			ps	
Tclkl	Clock Low Pulse Width	1000			ps	
Ts	Input Setup Time	-400			ps	2
Th	Input Hold Time	1500			ps	2
Tr,Tf	Output rise and fall times		175	250	ps	3
REGISTER MODE, READ AND WRITE CYCLES						
Trc	Read/Write Cycle Time	2500			ps	
Tar	Clock Rising Edge to Output Delay	800	1000	1200	ps	
LATCH MODE, READ AND WRITE CYCLES						
Tlc	Read/Write Cycle Time	3800			ps	
Tarl	Clock Rising Edge to Output Delay	2600		3800	ps	
Tafl	Clock Falling Edge to Output Delay	1200	1500	1700	ps	
TRANSPARENT MODE READ AND WRITE CYCLES						
Ttc	Read/Write CycleTime	3800			ps	
Tat	Clock Rising Edge to Output Delay	2600		3800	ps	

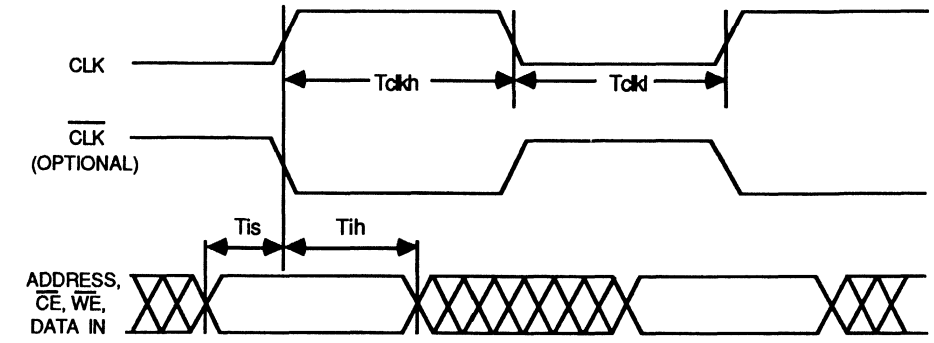
12G014 - 3

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
ALL MODES, READ AND WRITE CYCLES						
Tclkh	Clock High Pulse Width	1250			ps	
Tclkl	Clock Low Pulse Width	1250			ps	
Ts	Input Setup Time	-100			ps	2
Th	Input Hold Time	1800			ps	2
Tr,Tf	Output Rise and Fall Times		200	300	ps	3
REGISTER MODE, READ AND WRITE CYCLES						
Trc	Read/Write Cycle Time	3500			ps	
Tar	Clock Rising Edge to Output Delay	800	1400	1700	ps	
LATCH MODE, READ AND WRITE CYCLES						
Tlc	Read/Write Cycle Time	4500			ps	
Tarl	Clock Rising Edge to Output Delay	3300		4500	ps	
Tafl	Clock Falling Edge to Output Delay	1300	1600	2000	ps	
TRANSPARENT MODE READ AND WRITE CYCLES						
Ttc	Read/Write CycleTime	4500			ps	
Tat	Clock Rising Edge to Output Delay	3300		4500	ps	

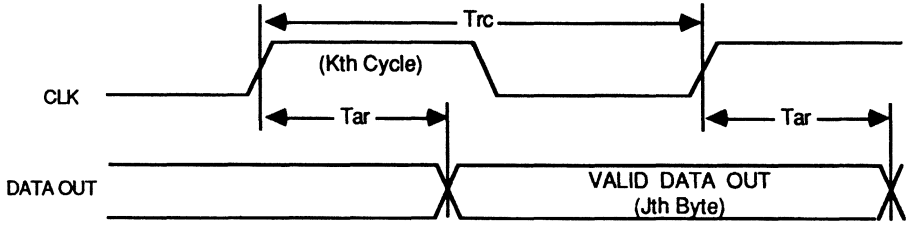
NOTES:
1. AC test conditions, unless otherwise stated:
   VBB = -1.3V, Rload = 50Ω to VTT = -2.0V, VIH = -0.8V, VIL = -1.8V, edge rate (all inputs) = 400 ps measured between 20% and 80% points. All delays measured between 50% points of signal transitions.
2. Measured from the rising edge of the clock input between 50% points.
3. Output rise and fall times are measured at the 20% and 80% points of the transition from VOL max. to VOH min.

SWITCHING WAVEFORMS

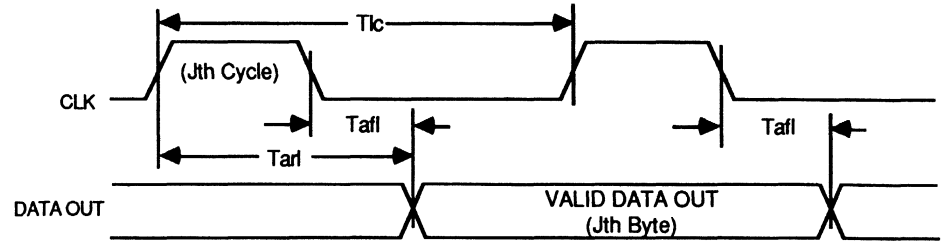
ALL MODES, READ AND WRITE CYCLES



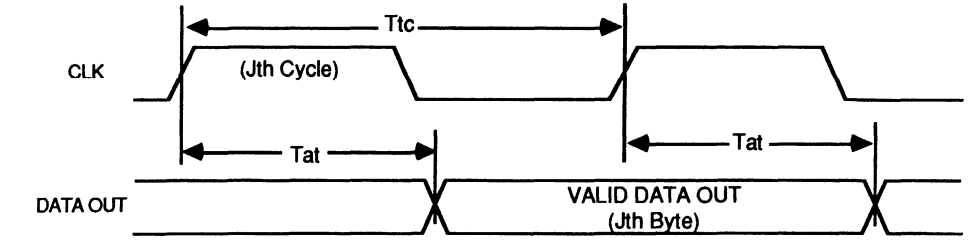
REGISTER MODE, READ AND WRITE CYCLES



LATCH MODE, READ AND WRITE CYCLES



TRANSPARENT MODE, READ AND WRITE CYCLES



1024 x 4 Bit Latched, Self-Timed Static RAM
3.0 ns Cycle = Access Time
12G NanoRam™ Family

DISTINCTIVE CAPABILITIES

- Equal read and write cycle times
- Fully latched I/O architecture
- Internally generated write pulse eliminates need for narrow write pulse
- Latch mode output achieves minimum machine access and cycle time
- Source follower outputs permit wire-OR capability
- On-chip output current sources for optional series termination
- Differential clock inputs
- ECL and 10G PicoLogic™ Family I/O compatible
- Temperature & voltage compensated
- Available in C-leaded or leadless chip carriers or in unpackaged die form

FUNCTIONAL DESCRIPTION

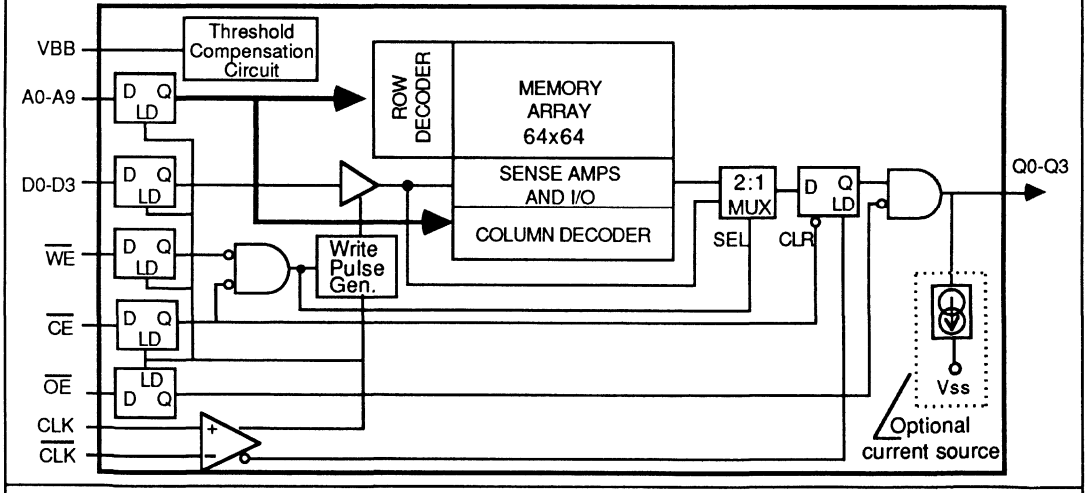
The 12G044 is a high speed 1024 word by 4-bit latched, Self-Timed Random Access Memory. The device is designed for high speed cache and buffer storage applications. The12G044 incorporates the innovative architecture of the NanoRam™ Family: latched inputs and outputs, internally generated write pulse, and a single clock to deliver maximum usable device speed in system applications.

The 12G044's input and output levels are ECL and 10G PicoLogic Family compatible. The VBB input pin provides direct voltage and temperature compensation for interface with ECL circuitry.

The 12G044 has source follower outputs to allow simple wire-OR expansion. As a wire bond option it can be offered with internal current sources (active pull-down) connected at the outputs for series termination.

The 12G044 is packaged in a 40 I/O leadless or C- leaded chip carrier and is fabricated using GigaBit's high volume GaAs MESFET process technology.

FUNCTIONAL BLOCK DIAGRAM



12G044 ORDERING INFORMATION

PACKAGE TYPE	Read/Write Cycle = Access Time		Optional Output Current Source(s)
	3.0 ns	TBD ns	
C-leaded chip carrier Leadless chip carrier Unpackaged die	12G044-2C 12G044-2L	12G044-3C 12G044-3L 12G044-3X	Please contact factory for special part number.

SYMBOL	PIN DESCRIPTIONS
A0 - A9	Address inputs: Lines A0 - A3 are column addresses. Lines A4 - A9 are row addresses.
$\overline{CE}$	Chip Enable: determines the enable state of the device. Chip Enable LOW activates the the memory. Chip Enable HIGH deactivates the memory and its output.
$\overline{WE}$	Write Enable: determines the read or write state of the device. Write Enable HIGH activates a read cycle. Write Enable LOW activates a self-timed write cycle.
CLK	Clock Input True: provides the basic timing for the memory device. All input latches are open (transparent) when clock is low and closed (latched) when clock is high. Data output latches are open (transparent) when clock is high and closed (latched) when clock is low.
$\overline{CLK}$	Complementary clock input. The 12G044 must be driven with a differential clock signal.
D0 - D3	Data In: with $\overline{WE}$ low, these lines determine the data input state information to be written into the addressed memory location.
Q0 - Q3	Data Out: these lines provide the valid data output from a Read Cycle or a copy of the input data (Di) being written into the memory during a Write Cycle.
$\overline{OE}$	Output Enable: Outputs are disabled when $\overline{OE}$ is high. They are either pulled low by a an external termination resistance to VTTor an optional on-chip current source (see block diagram), or forced high by the active output of another memory tied to the same bus line.
Vddl	Vddl: ground supply pin for the memory circuitry.
Vddo	Vddo: ground supply pin for the output drivers.
Vss	Vss: - 3.4 Volt power supply pin
Vee	Vee: - 5.2 Volt power supply pin.
Vttc	AC return pin for the package internal Vddo decoupling capacitor. Vttc is not brought onto the12G044 circuit, and is typically tied to Vtt (nominally -2.0V).
Vbb	Vbb: Reference input to the 12G044's input threshold compensation circuit. Connect to the VBB supplied from ECL when driving from ECL. Connect to VBBS supply pin when driving from PicoLogic. This pin must not be left unconnected.

Read Cycle

A read cycle is activated when Write Enable ($\overline{WE}$) is high. The read cycle is performed by presenting an address word (A0-A9) at the address input latches of the 12G044.

Addresses (Ai) presented when CLK is low (Address Access Time)

When clock (CLK) is low, the input address latches of the 12G044 are transparent and address information (Ai) immediately flows through the address latches into the memory Row and Column Decoders. When clock (CLK) goes high the output latches become transparent and read output data are then avalaible at Q0 to Q3, completing the read cycle. Therefore read access time is referenced to the transition of address input data (see Fig. 2, Ai, Address Access Time).

Addresses (Ak) presented when CLK is high (Clock Access Time)

If CLK is high when Addresses (Ak) are presented to the memory, the next CLK transition from high to low starts the read cycle. When CLK is high, the input address latches of the 12G044 are closed. Therefore, addresses (Ak) presented to the memory cannot flow through the address input latches. When clock (CLK) goes low, the memory read cycle starts, identical to the one described in the previous paragraph except that read access time is referenced to the falling edge of the CLK (see Fig. 2, Ak, Clock Access Time).

Write Cycle

A write cycle is activated when Write Enable ($\overline{WE}$) is low. Because the write pulse is internally generated, timing of Write Enable ($\overline{WE}$) is not critical. In addition, there is no need for a Write Enable ($\overline{WE}$) transition for each write operation. Therefore, $\overline{WE}$ can stay low during consecutive write operations. A write cycle is performed by presenting an address word (A0-A9) at the address input latches and a data word (D0-D3) at the data input latches of the 12G044. During a write cycle, $\overline{WE}$ is low and data is written into the memory array. The output pins (Q0-Q3) are updated with a copy of the input data (D0-D3) and the write cycle is completed.

Write cycle operation

When clock (CLK) is low, the input address and data latches of the 12G044 are transparent. Addresses (Ai) presented to the memory immediately flow through the input latches into the memory row and column decoders. Data Inputs (Di) flow through the data input latches, but are only written into the memory array when clock (CLK) goes high, assuming Write Enable ($\overline{WE}$) is low. Therefore, there is no possibility of writing invalid data in the memory array when clock is low and data is undefined. When clock (CLK) goes high, the output latches become transparent. A copy of the input Data (D0-D3) is then present at Q0-Q3 and the write cycle is completed.

Fig. 1 DEVICE OPERATION

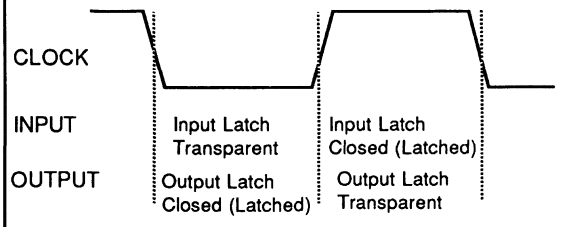
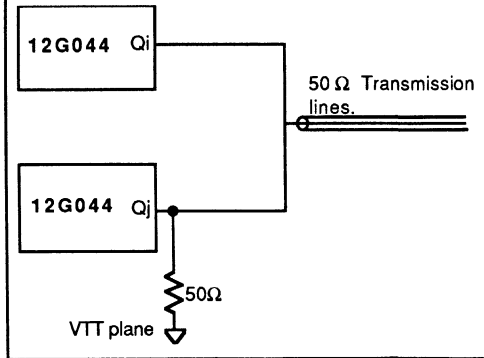
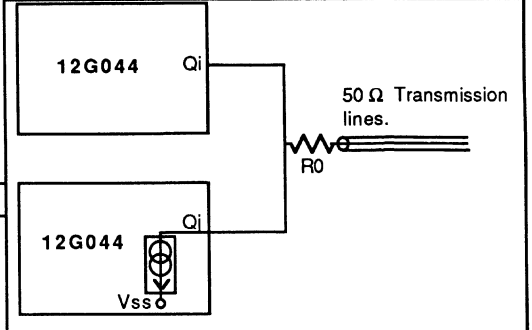


Fig. 2 OUTPUT TERMINATION OPTIONS

Shunt Termination Wire-OR



Series Termination Wire-OR



Notes:
- R0 is about 35Ω to 40Ω.
- only one pull down current source to Vss per bus line.

DEVICE DESCRIPTION

NanoRam™ Architecture

The NanoRam architecture provides a fully latched, clocked memory operation. This architecture is optimized for ultra high speed memory applications requiring fast nanosecond access and cycle times. A pair of complementary clocks (CLK and $\overline{CLK}$) establish the simple synchronous timing for the device.

Latched Inputs

The input latches are transparent when clock goes low (see fig. 1). All input state information, including Addresses (A0-A9), Write Enable ($\overline{WE}$), Chip Enable ($\overline{CE}$), Output Enable ($\overline{OE}$), and Data In (D0-D3) can then flow through the input latches into the chip. The setup and hold times relative to the rising edge of Clock are the same for all inputs. Addresses and all other input signals must be presented at least a set-up time (ts) before clock goes high and must be held valid for at least a hold time (th) thereafter. Once address, data and control inputs signals have been latched on-chip, they may transition to another state for the next cycle. This allows considerable time in each cycle for address, data and control input signals to change states without slowing the memory cycle timing.

Latched Outputs

Data Output latches are transparent when clock goes high (see fig. 1). Output data can then flow through the output latches to pins Q0 - Q3. The 12G044 features an Output Enable ($\overline{OE}$) control. Outputs are disabled when $\overline{OE}$ is high, effectively disconnecting the memory from the output data bus. Each disabled output of a 12G044 is pulled low by an external shunt resistance to VTT or by an optional on-chip current source (see next paragraph). For applications where outputs of different memories are wire-OR tied, the output of the active 12G044 determines bus line logic levels. A simplified example of a cache memory application on page 4 covers the Output Enable function in more detail.

The 12G044 uses source follower outputs. Since these outputs are floating, they can be easily wire-ORed. 12G044 outputs must be pulled low via a line termination resistance tied to VTT and equal to the characteristic impedance of the output transmission line (usually 50Ω). As a wire bond option, 12G044 outputs can be pulled down on-chip to VSS via a current source (active load). This enables series terminations which are particularly convenient for multiple output fanning. To series terminate, the user has to place an external resistance, Rs, in series with the output of the 12G044. Rs is defined such that : Rs + Ro =Zo, where Ro is the output impedance of the 12G044 (about 10Ω to 15Ω) and Zo is the characteristic impedance of the output transmission line (usually 50Ω). Upon customer request, GigaBit can supply any combination of standard source follower or on-chip current source outputs (see fig.2).

12G044 TRUTH TABLE

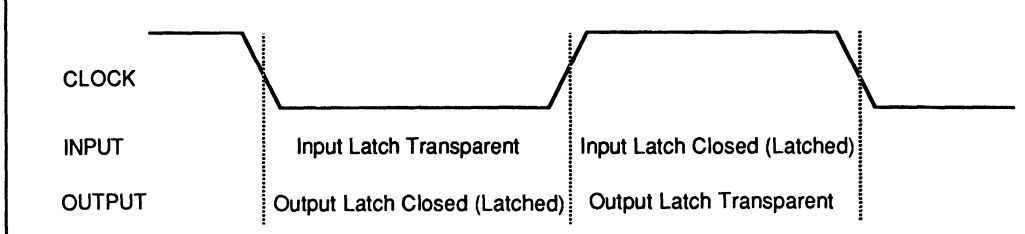
$\overline{CE}$	$\overline{WE}$	$\overline{OE}$	Q0-Q3	FUNCTION
H	X	X	DISABLED*	CHIP DISABLED
L	H	H	DISABLED*	READ CYCLE
L	H	L	Qi	READ CYCLE
L	L	H	DISABLED*	WRITE CYCLE
L	L	L	Di	WRITE CYCLE

*A Disabled output is either pulled low by an external termination resistance to VTT or on-chip current source, or forced high by the active output of another memory tied to the same bus line.

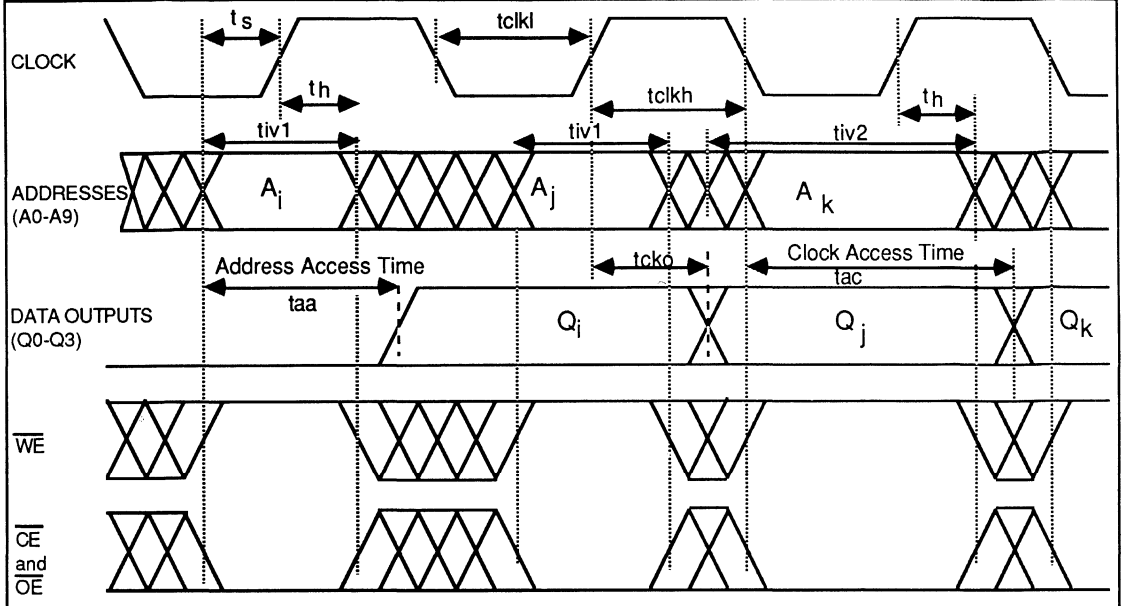
Differential Clock Inputs

The Clock input is differential to provide optimum sensitivity and noise immunity. Both CLK and $\overline{CLK}$ inputs must be provided. The Clock duty cycle may be asymmetrical within the limits allowed by the minimum clock pulse width specified in the AC Characteristics table.

Fig. 1 DEVICE OPERATION

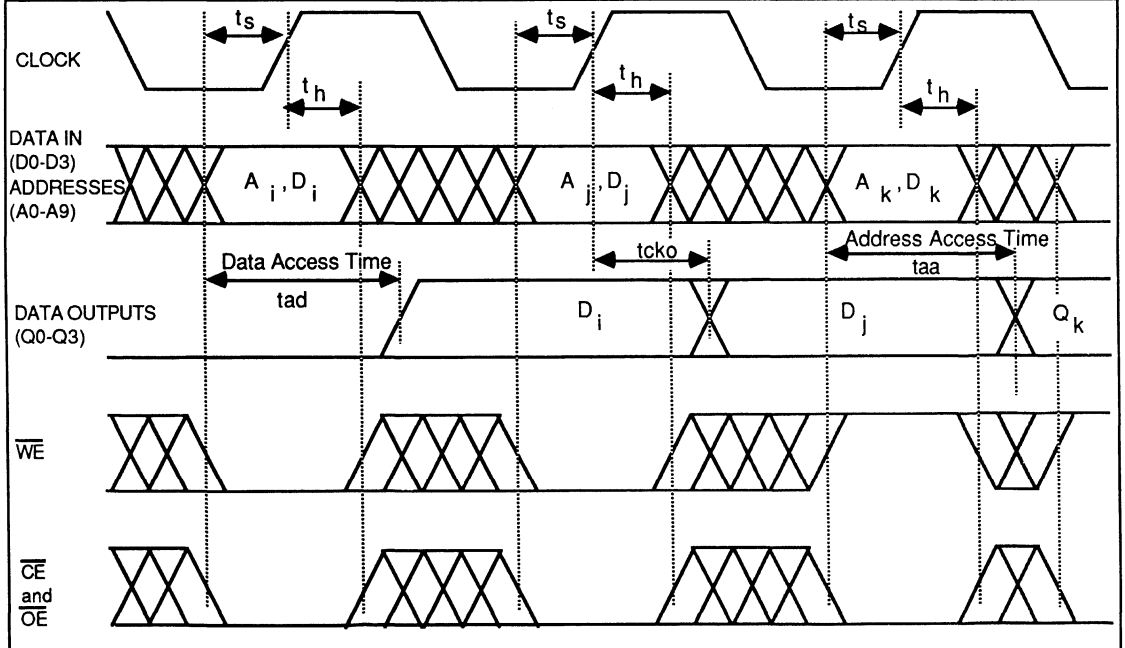


READ CYCLE



Note: Input Valid periods: tiv1≥ ts + th, tiv2≥ tclkl +th ; tiv2>tiv1.

WRITE CYCLE



CACHE MEMORY APPLICATION

The 12G044 can be used to configure a high speed cache memory. The diagram below shows a simplified 4K x 4 Cache Memory. Larger word size, 4K x 8, 4K x 16 or 4K x 32 can be realized by using 2, 4, or 8 rows respectively of four 12G044 SRAMs. Memory depth can be expanded to 16Kx4, 32Kx 4, or 64K X 4 with rows of 16, 32, or 64 12G044 SRAMs respectively. In both cases, Main Memory output data bus to the cache memory is then 32, 64 or 128-bits wide.

4K X 4 Cache Memory

A 4K X 4 Cache Memory requires one row of four 12G044 SRAMs. The Main Memory output data bus is 16 bits wide and drives the 4 bit data inputs of four 12G044. The data outputs of the 12G044 are wire ORed to form the C.P.U. data bus.

"Address Miss" Operation

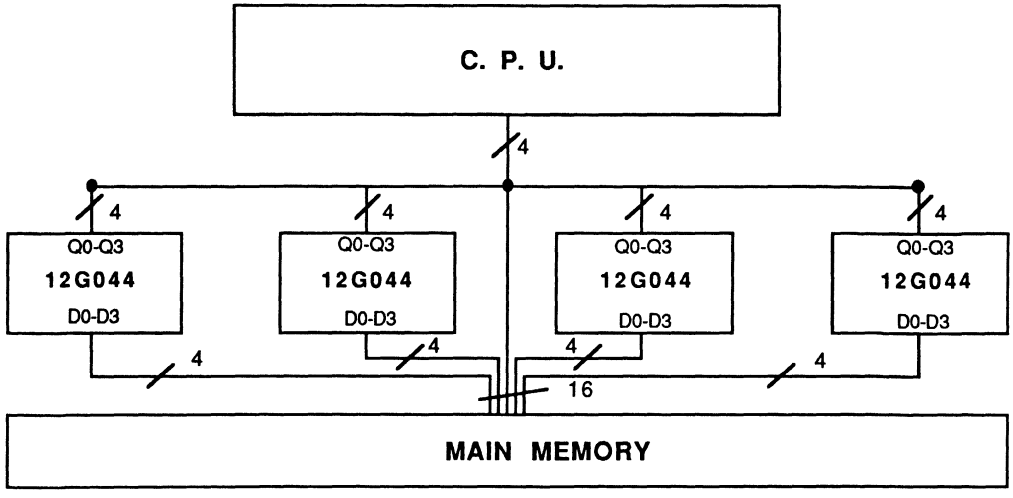
The most critical timing operation occurs during an "address miss", i.e. when the cache memory does not contain the Address/Data, (Ai/Di) combination of the Main Memory that the CPU wants to address. First, the Main Memory is read and outputs the desired data word (Di) to the 12G044 cache memory. Then, the 12G044 cache memory writes the data word (Di) into its on-chip memory array. Finally, the cache memory outputs the data word (Di) so that the C.P.U. can process it. The last two steps should be realized as fast as possible because Main Memory read cycle time is relatively long compared with the system cycle time. Any added delay through the cache memory penalizes overall system performance.

The 12G044 SRAM can perform both "address miss" cache memory operations (write from Main Memory and output to C.P.U.) in just 1 clock cycle, making it ideal for this application. Refer to the section on write cycle for more details.

Simultaneous Write to Cache Memories

In the example below, the Main Memory outputs a 16-bit data word to write simultaneously to all 4 cache memories. In order to write these data words to cache at the same time, all 4 cache memories have to be selected ($\overline{CE}$ low) and in the write cycle mode. Nevertheless, only one of the 4 cache memories should output a data word (Di) to the C.P.U.. The 12G044 features an output enable ($\overline{OE}$) to select which cache memory outputs should be enabled to provide the data word (Di) to the C.P.U..

SIMPLIFIED EXAMPLE OF A 4K X 4 CACHE MEMORY DIAGRAM



ABSOLUTE MAXIMUM RATINGS (Notes 1, 5)

(Beyond which useful life may be impaired)

SYMBOL	PARAMETER	ABSOLUTE MAXIMUM RATINGS	NOTES
Tstor	Storage Temperature	- 65 °C to + 150 °C	
Tj	Junction Temperature	-55 °C to + 150 °C	
Tc	Case Temperature Under Bias	-55 °C to + 125 °C	2
Vddo	Output Driver Supply Voltage	Vss to + 1.0 V	
Vbb	ECL Reference Voltage	-4.0 V to +0.5 V	
Ibb	Input current from interfacing family	-0.5 mA to +1.0 mA	
Vss	Supply Voltage	- 4.0 V to + 0.5 V	
Vee	Supply Voltage	- 7.0 V to Vss - 1.0 V	
Vin	Voltage Applied to Any Input; Continuous Vcc = 5.0, Vss = - 3.4 V, Vee = - 5.2 V	- 4.0 V to + 0.5 V	
Iin	Current Into Any Input; Continuous	- 0.5 mA to 1.0 mA	
Vout	Voltage Applied to Any Output	- 4.0V to +7.0 V	3
Iout	Current From Any Output; Continuous	-100 mA	3
Pd	Total Power Dissipation Tc = 85° C	3.9 W	4
Pout	Power Dissipation Per Output Pout = (Vddo-Vout) x Iout	100 mW	
Vttc	Vddo Internal Decoupling Cap. Return	- 6.0 V to Vddo	
Vtt	Load Termination Supply	- 6.0 V to Vddo + 6.0 V	3

NOTES: 1. All voltages specified with Vddl defined as 0 V. Positive current flows into the device.
2. Tc is measured at case top.
3. Subject to power dissipation limitations.
4. Total power dissipation is the limit of the package power dissipation. The operating power dissipation of the device is specified under DC Characteristics.
5. Sustained application of Vss in the absence of Vee may result in excessive power dissipation and damage to the device.

RECOMMENDED OPERATING CONDITIONS (Note 1)

SYMBOL	PARAMETER	MIN	NOM	MAX	UNITS	NOTES
Tc	Case Operating Temperature	0		85	℃	3
Vddl	Logic Supply Voltage		Gnd		V	
Vddo	Output Driver Supply Voltage	-0.8	Gnd	1.0	V	
Vbb	ECL Reference Voltage		- 1.3		V	
Vss	Supply Voltage	- 3.6	- 3.4	- 3.2	V	
Vee	Supply Voltage	- 5.5	- 5.2	- 4.9	V	
Vttc	Vddo Internal Decoupling Return	Vss	Vtt	Vddo	V	
Vtt	Load Termination Supply Voltage	Vss	- 2.0	- 1.8	V	2
Rload	Output Termination Load Resistance	25	50	100	Ω	2

NOTES: 1. All voltages are specified with respect to Vddl and Vddo, which are grounded.
2. The Rload and Vtt combination used is subject to maximum output current and output power restrictions.
3. This operating temperature can be maintained with a heat sink and air flow as determined by using Application Note 3. Tc measured at case top.
HEATSINKING IS REQUIRED. Heatsinks are available from GigaBit.

DC CHARACTERISTICS (note 5)

TEST CONDITIONS: Tc =0 °C to 85 °C, VSS = -3.6V to -3.2V, VEE = -5.5V to -4.9V, VDDL=VDDO = Gnd, Output load = 50Ω to Vtt = - 2.0 V, clock input edge rate ≤ 2 ns.

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	TEST CONDITIONS	NOTES
Voh	Output Voltage High	- 1.0	-0.8	-0.3	V		
Vol	Output Voltage Low	Vtt	-1.8	- 1.6	V		
Ioh	Output Current High		-70	-60	mA	Voh = - 1.0 V	1
Iol	Output Current Low		0.01	10	µA	Vol = -1.6V	
Vih	Input Voltage High	- 1.0		Vddl	V	Vbb = - 1.3 V	2
Vil	Input Voltage Low	- 2.0		- 1.6	V	Vbb = - 1.3 V	2,3
Iin	Logic Input Current	-100	10	100	uA	-1.8 V ≤ Vin ≤ -0.7 V	
Icir	Clock Input Current		220		µA		
Ibb	Vbb Input Current	-200	20	200	uA	Vbb = -1.3 V	
Iss	Power Supply Current		TBD		mA		
Iee	Power Supply Current		TBD		mA		
Pd	Power Dissipation		2.4	3.3	W		4

NOTES:

1. Ioh is the maximum current the output can source under any Rload and Vtt combination.
2. The input threshold is referenced to the Vbb input. Therefore Vih and Vil will track the Vbb input.
3. Inputs may be connected to Vss (-3.4V) to establish a logic low level.
4. Measured at nominal supply voltages and 50% output duty cycle. Excludes Vddo output source follower power (typically 10 mW per loaded output).
5. For proper operation, the clock input edge rate should be ≤ 2 ns.

12G044 - 2 AC CHARACTERISTICS (note 1)

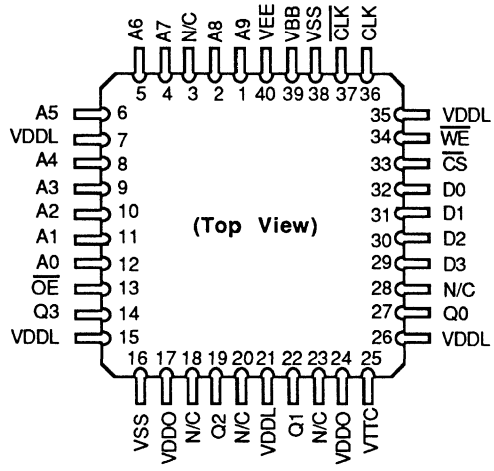
Test Cond.: Tc =0 °C to 85 °C, VSS = -3.6V to -3.2V, VEE = -5.5V to -4.9V, VDDL=VDDO = Gnd

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
READ AND WRITE CYCLES						
tclkh	Clock High Pulse Width		2000		ps	
tclkl	Clock Low Pulse Width		1000		ps	
ts	Input Setup Time		500		ps	2
th	Input Hold Time		800		ps	2
tc	Read/Write Cycle Time		3000		ps	
taa	Address access time		3000		ps	
tac	Clock access time		3000		ps	
tad	Data access time		3000		ps	
tcko	Clock Rising Edge to Output Delay		1000		ps	
tr, f	Output Rise and Fall Times		200		ps	

NOTES:

1. AC test conditions, inless otherwise stated:
   Vbb = -1.3V, Rload = 50Ω to Vtt = -2.0V, Vih = -0.8V, Vil = -1.8V, edge rate (all inputs) = 400 ps measured between 20% and 80% points. All delays measured between 50% points of signal transitions.
2. Measured from the rising edge of the clock input between 50% points.
3. Output rise and fall times are measured at the 20% and 80% points of the transition from Vol max. to Voh min.

PIN FUNCTION DIAGRAM - 40 I/O TYPE "L" & "C" PACKAGES



NOTES: • Pin 1 is marked for orientation.
• N/C = No Connection.

GigaBit Logic

14GM048
14GD048
ADVANCE

512 x 8-Bit Mask-Programmable ROM
1.0 GByte/s Access Rate
14G NanoRom™ Family

DISTINCTIVE CAPABILITIES

- 512 word x 8-bit organization
- 1 ns typical address access time
- 500 ps typical OE access time
- ECL compatible I/O levels
- ECL compatible power supplies
- Temperature and voltage compensated design
- Wire-OR output capability for bus connection
- On-chip output (chip) enable decoder (14GD048)
- Available in 40 pin C-leaded or leadless chip carriers, or in dice form

APPLICATIONS

- Direct digital synthesis
- High speed control, mapping, code conversion
- High speed table look up
- High speed sequencers and state machines

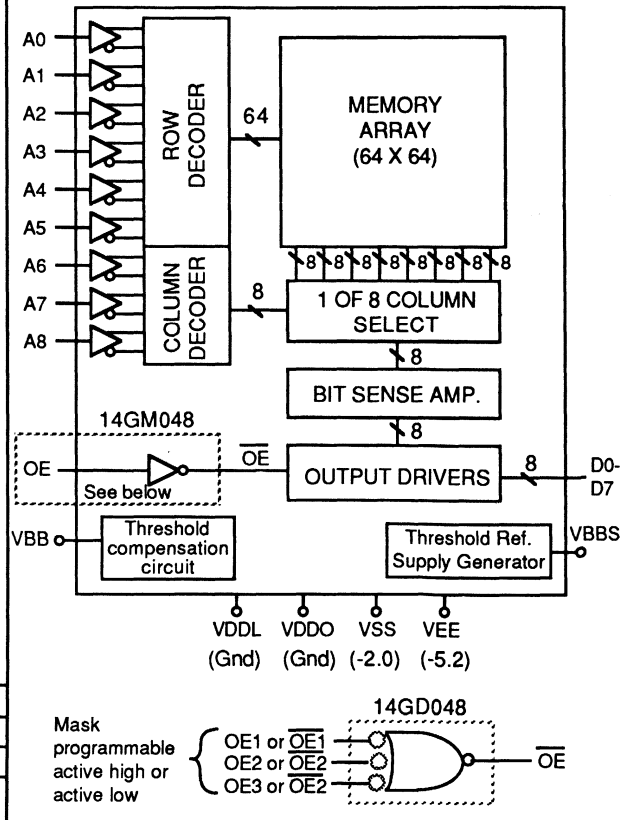
FUNCTIONAL DESCRIPTION

The 14GX048 is a high speed, single metal mask layer programmable read only memory organized as 512 words of 8 bits each. Typical address access time is just 1 ns making the device ideal for application in a wide varierty of high speed systems. Input/output levels are ECL and GaAs compatible. The device requires standard ECL power supplies of -5.2V and -2.0V.

The 14GX048 also features open source follower outputs which permit wire-OR connection in bus organized systems. The 14GM048 has a single OE input for fastest OE access time. The 14GD048 features a user programmable OE decoder for logic flexibility and for memory expansion up to 32K without the need for external decoding. The fast (500 ps typical, 14GM048) output enable access time permits direct address decoding without increasing overall memory access time. The 14GX048 features the PicoLogic family standard VBB input which allows the input logic threshold to be controlled by the driving logic family.

The 14GX048 is fabricated using GigaBit's high performance, low power HME/D GaAs MESFET process technology.

BLOCK DIAGRAM



14GX048 ORDERING INFORMATION

PACKAGE TYPE	Address access time
	1.0 NS ACCESS TIME
C-Leaded CC	14GX048-2C
Leadless CC	14GX048-2L
Die	14GX048- X

PIN DESCRIPTONS

A0-A8	Address inputs	VBBS	PicoLogic threshold reference output voltage (nom. - 1.2V). Connect to VBB when driving from PicoLogic.
OE	14GM048 active high output enable input	VDDL	Internal circuitry ground connection
OE1-OE3	14GD048 output enable inputs. Signal sense is mask programmable.	VDDO	Output driver ground connection
D0-D7	Read data output word	VSS	-2.0 volt power supply
VBB	Reference input to the 14GX048's input threshold compensation circuit. Connect to the VBB supplied from ECL when the 14GX048 is driven from ECL. Connect to the VBBS pin when driving from PicoLogic. Do not leave open.	VEE	-5.2 volt power supply
		VTT	Termination voltage connection to the package top surface plane.

14GX048 PROGRAMMING INSTRUCTIONS

ROM Code Data

GigaBit prefers to receive ROM bit pattern in EPROMs. Two EPROMs should be submitted: one programmed to the desired pattern and the other one blank. GigaBit will read the programmed EPROM, transfer its data content to a disk and then program the blank EPROM with the data stored in the disk. The EPROM programmed by GigaBit is returned to the customer for verification of the ROM pattern. Unless otherwise requested, GigaBit will not proceed until the customer confirms that the program in the returned EPROM is equivalent to the one originally sent. This procedure guarantees that the bit pattern has been properly entered into GigaBit's computer.

EPROM Requirements

2716, 2732 or 2764 EPROM should be used to submit ROM code data. Data in the EPROM should be entered from address 000 to address 1FF. Customers should also specify the type of ROM desired:

- 14GM048 active high output enable
- 14GD048:
  OEi =1 $1 \le i \le 3 \rightarrow$ OE active high
  OEi =0 $1 \le i \le 3 \rightarrow$ OE active low

Pattern Data from ROMs or EEPROMs

GigaBit will accept pattern data in ROMs or EEPROMs if these are pin compatible with 2716, 2732 or 2764 EPROMs.

Optional Method of Supplying ROM Data

GigaBit will also accept ROM patterns in IBM PC floppy disks or 9-Track NRZ Magnetic Tapes, VMS operating system 1600 BPI or 6250 BPI. Format for these two optional media should be:

- 1st line: For identification only (not processed)
- 2nd line: 14G x 048_____OE1 OE2 OE3
  (at least on blank)

  If X =D Decoder:
  OEi =1 $1 \le i \le 3 \rightarrow$ OE active high
  OEi =0 $1 \le i \le 3 \rightarrow$ OE active low

If X=M Fixed OE (active high); OE1, OE2 and OE3 disregarded.

- 3rd line to Nth line:
  Address _____ 16 Data Words
  (at least on blank)

Address in hexadecimal starting with location zero — Data in hexadecimal separated by one blank

(Carriage return at the end of each line)

ABSOLUTE MAXIMUM RATINGS

(Beyond which useful life may be impaired) (Notes 1, 4)

SYMBOL	PARAMETER	ABSOLUTE MAXIMUM RATINGS	NOTES
TSTOR	Storage Temperature	- 65 °C to + 150 °C	
TJ	Junction Temperature	- 55 °C to + 150 °C	
TC	Case Temperature Under Bias	- 55 °C to + 125 °C	2
VDDO	Output Driver Supply Voltage	VSS to + 1.0 V	
VSS	Supply Voltage	-3.0 V to + 0.5 V	
VEE	Supply Voltage	- 7.0 V to VSS + 0.5 V	
VIN	Voltage Applied to Any Input; Continuous VSS = -2.0 V, VEE = - 5.2 V	- 4.0 V to + 0.5 V	
IIN	Current Into Any Input; Continuous	- 0.5 mA to 1.0 mA	
VOUT	Voltage Applied to Any Output	-4.0V to + 7.0 V	3
IOUT	Current From Any Output; Continuous	-100 mA	
PD	Power Dissipation Per Output POUT = (VDDO-VOUT) x IOUT	100 mW	
VBB	Threshold Reference Input Voltage	-4.0V to +0.5V	
IBB	Input current (from interfacing family)	-0.5 mA to +1.0 mA	
VTT	Load termination supply voltage	-6.0V to Vddo + 6.0V	3

Notes:

1. All voltages specified with VDDL defined as 0 V. Positive current is defined as current into the device.
2. TC is measured at case top.
3. Subject to IOUT and power dissipation limitations.
4. Power supply sequencing is not necessary, but since the VEE supply is used to bias off the normally-on depletion mode transistors, sustained (>5 secs.) application of VTT in the absence of VEE may result in excessive power dissipation and damage to the device.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN	NOM	MAX	UNITS	NOTES
TC	Case Operating Temperature	0	25	85	℃	1
VDDL	Logic Supply Voltage		Gnd		V	
VDDO	Output Driver Supply Voltage	-0.8	Gnd	1.0	V	
VSS	Supply Voltage	- 2.2	- 2.0	- 2.0	V	
VEE	Supply Voltage	- 5.6	- 5.2	- 5.0	V	
VTT	Load Termination Supply Voltage	VEE	- 2.0	- 2.0	V	2,3
RLOAD	Output Termination Load Resistance	25	50		Ω	2,3

Notes:

1. Tcase measured at case top. **User attention to device thermal management is recommended.** See GigaBit Application Note 3, "Thermal Management of PicoLogic and NanoRam GaAs Digital IC Families" for a complete discussion of all aspects of device thermal management. Heatsinks are available from GigaBit. See last page, notes 6 and 7.
2. The RLOAD and VTT combination used is subject to maximum output current and power restrictions.
3. VOL max. will not be met if Rload is > 100Ω (for VTT = -2.0V) or for VTT > -2.0V.

DC CHARACTERISTICS (Notes 1,2)

Tc = 0°C to 85°C, VSS = -2.0V to -2.2V, VEE = -5.6V to -5.0V, VDDL=VDDO = 0V, unless otherwise indicated.

Symbol	Parameter	Min	Typ	Max	Units	Test Conditions	Notes
VOH	Output voltage high	-0.8	-0.4	- 0.3	V		
VOL	Output voltage low	VTT	-1.9	- 1.8	V		
IOH	Output current high		-70	- 60	mA	VOH = -0.8V	3
VIH	Input voltage high	-1.0		VDDL	V		
VIL	Input voltage low	VSS		- 1.6	V		
Iin	Input current	-500	0	500	uA	VIN = -1.0V to -1.6V	
VBBS	Threshold reference voltage		-1.2		V		4
ISS	Vss power supply current			50	mA		
IEE	Vee power supply current			350	mA		
PD	Power dissipation		1.5	2.0	W		5

Notes:
1. These characteristics are applicable from DC to 500 MHz.
2. Test conditions unless otherwise indicated: VBB = -1.3V, VTT = -2.0V, Rload = 50Ω to VTT.
3. IOH is the available source follower output current at VOH = -0.8V.
4. Nominally equal to -1.2V with a 40Ω source impedance. The range of VBBS at 25°C is -1.05V to -1.3V. ΔVBBS/ΔTemp. = +0.6mV/°C; ΔVBBS/ΔVSS = +0.2mV/mV.
5. Measured at nominal supply voltages and 50% output duty cycle. Excludes VDDO output source follower power (typically 10 mW per loaded output).

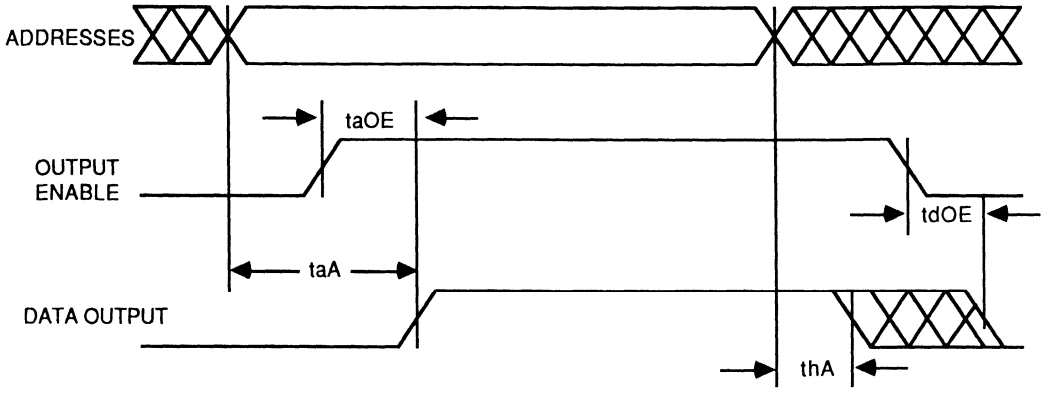
14GX048-2 AC CHARACTERISTICS (Notes 1, 2)

Test Conds: Tc = 0°C to 85°C, VSS= -2.0V to -2.2V,VEE= -5.0V to -5.6V,VDDL=VDDO=Gnd.

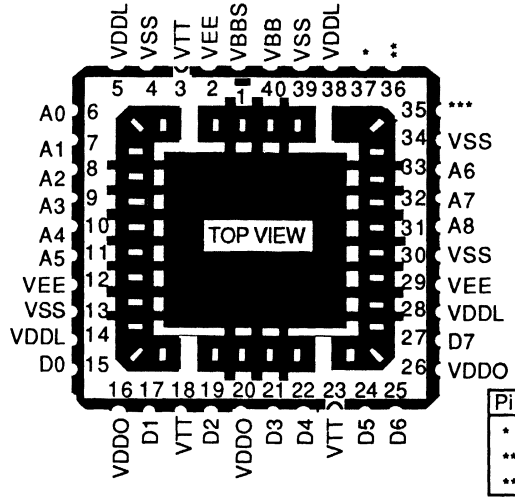
SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
taA	Address access time		1000	1500	ps	
taOE	Output enable access time		500	800	ps	
thA	Data valid hold time	200			ps	
tdOE	Output disable delay		500	800	ps	
tr	Output rise time		175	225	ps	
tf	Output fall time		150	200	ps	

NOTES:
1. Test conditions (unless otherwise noted): Vbb = -1.2V, Vtt = -2.0V, Rload = 50Ω to Vtt, Vih = -0.7V, Vil = -1.7V, Voh ≥ -0.7V, Vol ≤ -1.7V. Input signal rise and fall times <150ps.
2. Output rise and fall times are measured at the 20% and 80% points of the transition from Vol max to Voh min.

SWITCHING WAVEFORMS



PIN FUNCTIONS - PACKAGE TYPES "L" AND "C"



NOTE: Pin 1 is marked for orientation.

Pin	14GM048	14GD048
*	DNC	OE1 or $\overline{OE1}$
**	DNC	OE2 or $\overline{OE2}$
***	OE	OE3 or $\overline{OE3}$

DNC: Do not connect (pin at VSS potential)

16G FAMILY PRODUCTS

TABLE OF CONTENTS

Programmable GaAs Schottky Diode Arrays

DISTINCTIVE CAPABILITIES

- 14 Schottky barrier diodes and one full wave rectifier on each chip
- 15 mA (16G010) and 100 mA (16G011) versions
- Very low junction capacitance
- Low series resistance
- Excellent thermal and electrical matching
- 150 GHz typical RC cutoff frequency
- Available with personalized interconnects in the package for design integration and improved performance
- Available in leadless chip carrier (LCC) , flatpack, or die form.

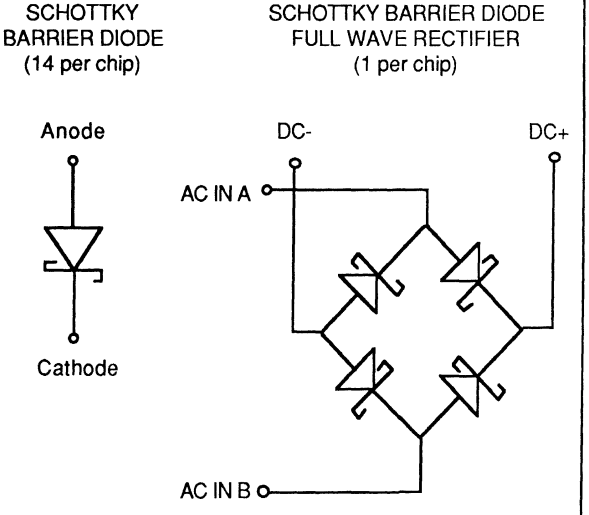
APPLICATIONS

- Sample and Hold Amplifiers
- High speed switching
- Waveform clamps
- High frequency mixers
- Video to microwave detectors
- Harmonics generators
- Input overload protection devices for electrostatic discharge (ESD) or RF overload
- Low capacitance varactors

FUNCTIONAL DESCRIPTION

The 16G010 and 16G011 are respectively, 15 mA and 100 mA GaAs Schottky barrier diode arrays. Each arrary consists of 14 individual diodes plus a full wave rectifier. Both arrays feature exceedingly low junction capacitance (0.042 pf typ. for the 16G010 and 0.12 pf typ. for the 16G011) and low series resistance (25Ω typical @ If = 5mA for the 16G010 and 7Ω typical @ If =30mA for the 16G011). The 3 dB cut-off frequency is 150 GHz for the 16G010 and 190 GHz for the 16G011. It is lower for packaged parts due to package capacitance. In order to take better advantage of the high frequency characteristics of the diodes in the 16G010/16G011, GigaBit offers the option to interconnect Diodes and add chip components as necessary inside the package (LCC or Flatpack). Package parasitic capacitance and inductance generally limits the performance of packaged parts. By interconnecting the Diodes inside the package to form a personalized analog function, the overall effect of package parasitic impedance is reduced since there is less I/O per function. The 16G010 and 16G011 are fabricated using GigaBit Logic, GaAs planar process technology.

16G010, 16G011 CIRCUIT DIAGRAM



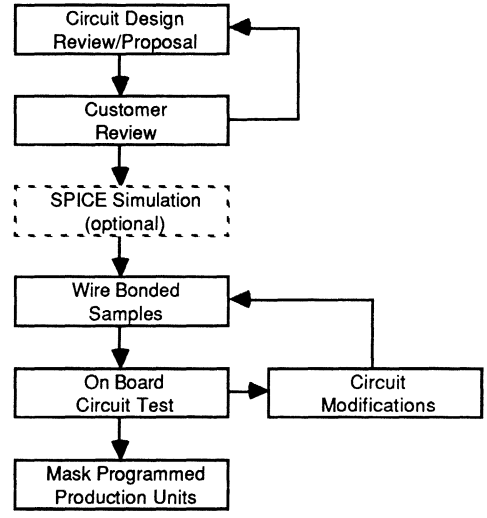
ORDERING INFORMATION		
PACKAGE TYPE	16G010	16G011
36 I/O Leadless CC	16G010-L36	16G011-L36
36 I/O Flatpack	16G010-F	16G011-F
Die	16G010-X	16G011-X

ORDERING INFORMATION
16G010/16G011 DIODE ARRAY PERSONALIZATIONS
Please contact factory for special part number.

CIRCUIT DESIGN INTEGRATION USING PERSONALIZED 16G010/16G011

GigaBit Logic can integrate certain analog designs by utilizing the 14 Diodes in the 16G010/16G011. Chip resistors and capacitors can also be added in the package cavity to realize more complex circuits. By interconnecting 16G010/16G011 Diodes inside the package, GigaBit can offer personalized analog functions with better performance than when the interconnects are external. First, the effect of package and wire bonds parasitic capacitance and inductance is reduced since there are fewer I/O per function. Chip capacitors and resistors can be attached close to the die bond pads in order to minimize wire bond length. Second, since there are fewer overall I/O per package, it is possible to adopt a Ground-Signal-Ground approach for the pin-out. This lowers cross capacitance between adjacent pins reducing cross talk as well as potential jitter in the circuit.

DESIGN INTEGRATION PROGRAM FLOW



PROGRAM FLOW FOR PROTOTYPES

GigaBit will review or propose a circuit schematic to personalize the 16G010/16G011 to the desired function. Prototypes are custom wire-bonded during assembly. Chip resistors and capacitors are added in the package as necessary. This approach has two main advantages: no Non-Recurring Engineering Expenses (NRE) and a quick turnaround time (2 to 4 weeks). Since there is no NRE, designers have total flexibility to try out a design and modify it if necessary.

GigaBit can provide, as an option, complete simulation of the circuit utilizing its proprietary spice model.

PROGRAM FLOW FOR PRODUCTION DEVICES

Production devices are customized via mask programming. The interconnects are realized in the IC substrate by changing the top metal layer mask of the 16G010/16G011.

Mask programming for production devices is advised to improve reliability and reproducibility compared with wire bonded prototypes. In addition, mask programmed ICs require less assembly work and are lower in cost compared with wire bonded prototypes.

EXAMPLES

Applications that can be integrated using the 16G010/16G011 Diode arrays include:

- Sample and hold amplifiers
- High frequency detectors
- Input overload protection diodes

ABSOLUTE MAXIMUM RATINGS
(Beyond which useful life may be impaired)

SYMBOL	PARAMETER	ABSOLUTE MAXIMUM RATINGS
I_F	Forward Current 16G010	28 mA
	16G011	200 mA
V_R	Reverse Bias Voltage	18 V
V_{ISOL}	Isolation Voltage Between Diodes	50 V
P_D	Maximum Power Dissipation -- per chip 16G010	1.5 W
	10G011	1.5 W
	-- per diode 16G010	100 mW
	16G011	500 mW
T_{STOR}	Storage Temperature	- 65 °C to + 150 °C

16G010L, 16G010F, 16G010X
ELECTRICAL CHARACTERISTICS (Note 1)

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
V_F	Forward Voltage (Note 2)	I_F = 1 mA	0.68	0.73	0.78	V
		I_F = 5 mA		0.82	0.92	V
		I_F = 15 mA		0.96	1.1	V
V_{FM}	Forward Voltage Match	I_F = 5 mA		9	20	mV
I_R	Reverse Current	V_R = 4 V		0.01	1.0	µA
V_{BR}	Breakdown Voltage	I_R = 15 µA	6.0	8.0		V
V_{ISOL}	Isolation Voltage Between Diodes	I = 15 µA		40		V
I_{ISOL}	Leakage current Between Diodes	V = 30 V			1.0	µA
I_F+I_R	Forward + Reverse Current	V_F = 230 mV		60		nA
C_{jo} + C_p	Junction plus Parasitic Capacitances (Note 3)	DIE, V_F = 0 V		0.042		pF
R_S	Series Resistance	I_F = 1mA, 3mA, 5mA		25	35	Ω
Δ V / Δ T	Temp. Coeff of Forward Voltage Match	T_A = 0 °C to 85 °C		±20		µV/°C
$\frac{1}{2\pi RsCjo}$	Series RC Cutoff Frequency (Note 3)	DIE		150		GHz

16G011L, 16G011F, 16G011X
ELECTRICAL CHARACTERISTICS (Note 1)

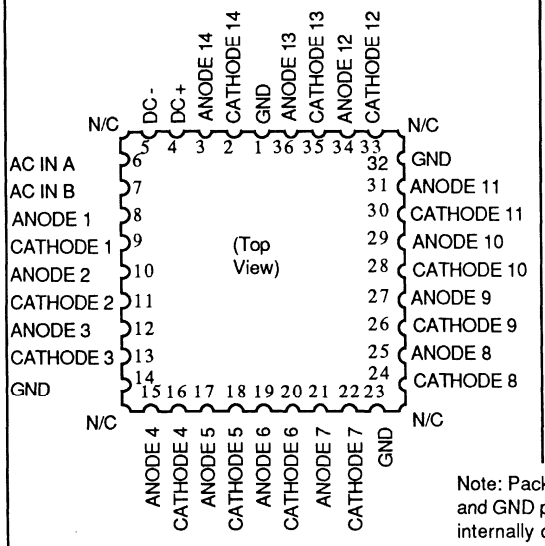
SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
V_F	Forward Voltage (Note 2)	I_F = 5 mA	0.60	0.68	0.76	V
		I_F = 15 mA		0.76	0.88	V
		I_F = 30 mA		0.82	0.94	V
		I_F = 50 mA		0.89	1.01	V
		I_F = 100 mA		1.06	1.18	V
V_{FM}	Forward Voltage Match	I_F = 50 mA		8	20	mV
I_R	Reverse Current	V_R = 4 V		0.01	5.0	µA
V_{BR}	Breakdown Voltage	I_R = 100 µA	6.0	7.0		V
V_{ISOL}	Isolation Voltage Between Diodes	I = 100 µA		40		V
I_{ISOL}	Leakage current Between Diodes	V = 30 V			1.0	µA
I_F+I_R	Forward + Reverse Current	V_F = 230 mV		60		nA
C_{jo} + C_p	Junction plus Parasitic Capacitances (Note 3)	DIE, V_F = 0 V		0.12		pF
R_S	Series Resistance	I_F = 15mA, 30mA, 50mA		7	25	Ω
$\Delta V / \Delta T$	Temp. Coeff of Forward Voltage Match	T_A = 0 °C to 85 °C, I_F = 50 mA		±20		µV/°C
$\frac{1}{2\pi RsCjo}$	Series RC Cutoff Frequency (Note 3)	DIE		190		GHz

NOTES:

1. Test conditions, unless otherwise stated: TA = 25°C
2. Max V_F for single diodes only. For Diode Bridge add 0.05 V.
3. For packaged parts, the measured capacitances will be increased by both shunt capacitance (C1G from each pin to ground) and interelectrode capacitance (C12, between adjacent pins). For the flatpack (assuming 0.150" external leads), the shunt capacitance is C1G = 0.25 pf and the interelectrode contribution is C12 = 0.20 pf. In addition, each lead has a series inductance of about 7nH in the flatpack (including the 0.150" Leads). For the leadless chip carrier package these values are C1G = 0.5 pf shunt and C12 = 0.1 pf, with a series inductance of 4nH on each lead. The shunt capacitances are principally to the ground pin on the package, which should be connected to an AC ground to minimize high frequency crosstalk between diodes.

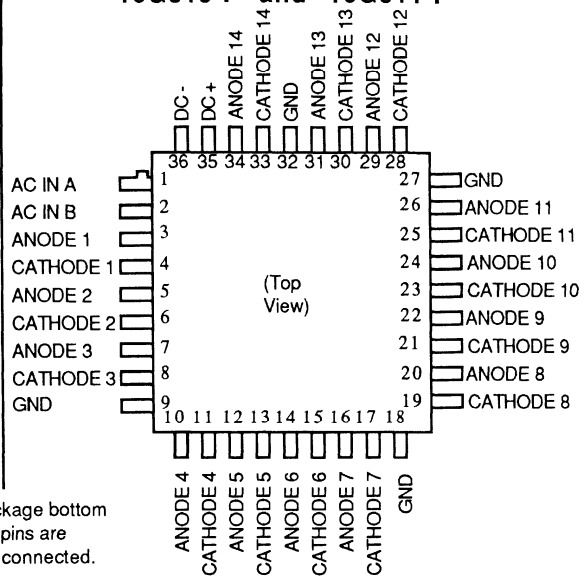
PIN FUNCTION DRAWINGS

36 I/O LEADLESS CHIP CARRIER
16G010-L36 and 16G011-L36



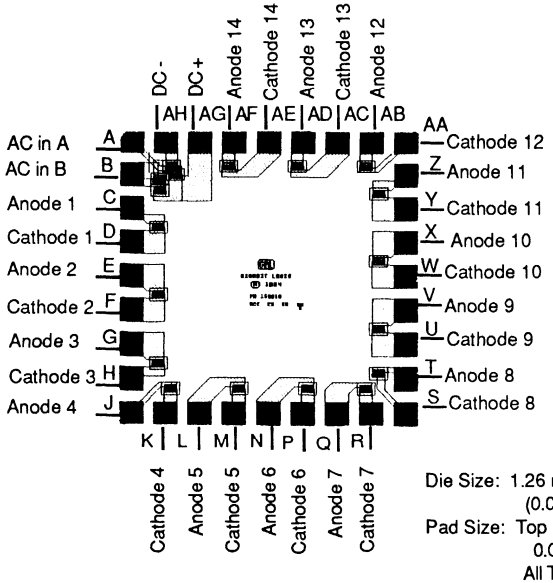
Note: Package bottom and GND pins are internally connected.

36 LEAD FLATPACK PACKAGE
16G010-F and 16G011-F



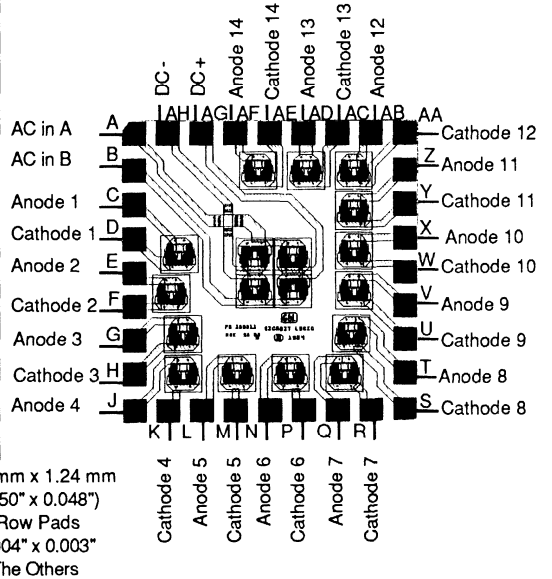
METALLIZATION AND PAD LAYOUT

16G010-X



Die Size: 1.26 mm x 1.24 mm
(0.050" x 0.048")
Pad Size: Top Row Pads
0.004" x 0.003"
All The Others
0.004" x 0.003"

16G010-X



Programmable Single Gate GaAs D-MESFET Array

DISTINCTIVE CAPABILITIES

- 11 single gate depletion MESFETs on each chip
- f_t = 22 GHz typical frequency response
- -0.9 V pinchoff voltage, 35 mA I_{DSS} (typ.)
- Excellent thermal and electrical matching
- Very low capacitance
- Available with personalized interconnects in the package for design integration and improved performance
- Available in leadless chip carrier (LCC), flatpack or die form

APPLICATIONS

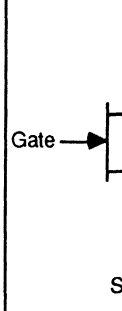
- Low noise amplifiers (broadband, video, IF, RF, or microwave)
- Interface circuitry to digital logic
- Ultra low capacitance buffers
- RF or high-speed current source/Active load
- Analog switches
- Switch drivers
- Laser drivers
- Source-follower line drivers (digital or analog)
- Differential amplifiers/current-steering circuits

FUNCTIONAL DESCRIPTION

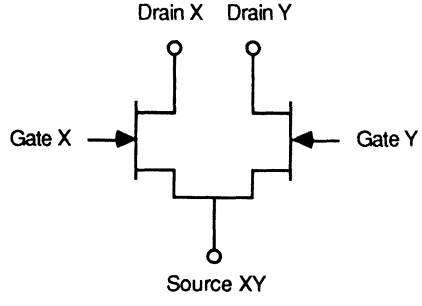
The 16G020 contains 11 single gate GaAs depletion mode MESFETs on a single chip. The device characteristics of these N-channel, Schottky-gate D-MESFETs are similar to those of silicon N-channel JFETs. Typical gate voltage ranges between Vgs =-0.9V (threshold of drain conduction) to Vgs = +0.6 V (onset of strong gate forward conduction current). The device structure is symmetrical, allowing interchange of source and drain electrodes. Electrically, the source is defined as the more negative of these two electrodes. To reduce Miller capacitance (Cgd), the source electrode is defined as the pad immediately adjacent to the gate bonding pad, since this will have slightly more parasitic capacitance than to the second pad over, identified as the drain. One pair of MESFETs has a common source for use as a differential pair. 16G020 MESFETs feature a -0.9V pinchoff voltage and very low junction capacitance, making them ideal for high frequency applications utilizing relatively small signal levels in both digital and analog circuits. In order to take better advantage of the high frequency characteristics of the FETs in the 16G020, GigaBit offers the option to interconnect FETs and add chip components as necessary inside the package (LCC or Flatpack). Package parasitic capacitance and inductance generally limits the performance of packaged parts. By realizing the interconnects inside the package to form a personalized analog function, the overall effect of package parasitic impedance is reduced since there is less I/O per function.

CIRCUIT DIAGRAMS

SINGLE GATE D-MESFETS (9 per chip)



SINGLE GATE D-MESFETS DIFFERENTIAL PAIR (1 per chip)



ORDERING INFORMATION

PACKAGE TYPE	PART NUMBER
36 I/O Leadless CC	16G020-L36
36 I/O Flatpack	16G020-F
Die	16G020-X

16G020 FET ARRAY PERSONALIZATION

Please contact factory for special part number.

CIRCUIT DESIGN INTEGRATION USING PERSONALIZED 16G020

GigaBit Logic can integrate certain analog designs by utilizing the 11 single gate MESFETs in the 16G020. Chip resistors and capacitors can also be added in the package cavity to realize more complex circuits. By interconnecting 16G020 FETs inside the package, GigaBit can offer personalized analog functions with better performance than when the interconnects are external. First, the effect of package and wire bond parasitic capacitance and inductance is reduced since there are fewer I/O per function. Chip capacitors and resistors can be attached close to the die bond pads in order to minimize wire bond length. Second, since there are fewer overall I/O per package, it is possible to adopt a Ground-Signal-Ground approach for the pin-out. This lowers cross capacitance between adjacent pins reducing cross talk as well as potential jitter in the circuit.

PROGRAM FLOW FOR PROTOTYPES

GigaBit will review or propose a circuit schematic to personalize the 16G020 to the desired function. Prototypes are custom wire-bonded during assembly. Chip resistors and capacitors are added in the package as necessary. This approach has two main advantages: no Non-Recurring Engineering Expenses (N.R.E.) and a quick turnaround time (2 to 4 weeks). Since there is no NRE, designers have total flexibility to try out a design and modify it if necessary.

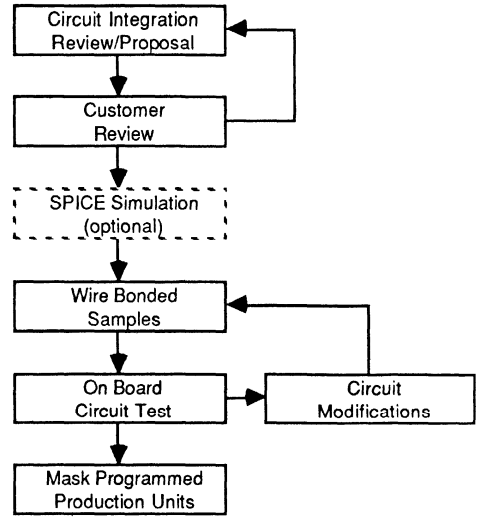
GigaBit can provide, as an option, complete simulation of the circuit utilizing its proprietary spice model.

PROGRAM FLOW FOR PRODUCTION DEVICES

Production devices are customized via mask programming. The interconnects are realized in the IC substrate by changing the top metal layer mask of the 16G020.

Mask programming for production devices is advised to improve reliability and reproducibility compared with wire bonded prototypes. In addition, mask programmed ICs require less assembly work and are lower in cost compared with wire bonded prototypes.

DESIGN INTEGRATION PROGRAM FLOW

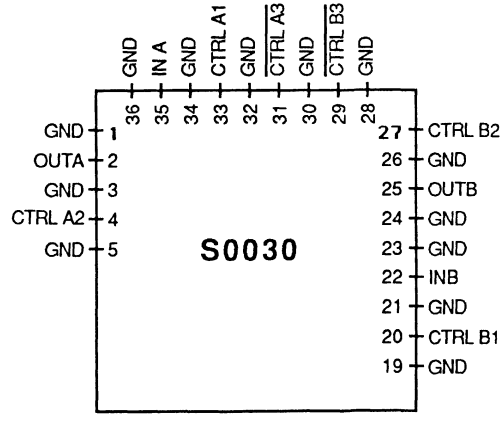


EXAMPLES

Some examples of analog ICs developed using the 16G020 FET arrays are:

- Dual high isolation analog switch with 0.5 ns switching time and 80 dB isolation at 1 GHz (S0030)
- Switch driver/high speed driver with 9V/ns output slew rate
- Octal GaAs to TTL translator

Dual Analog Switch
S0030



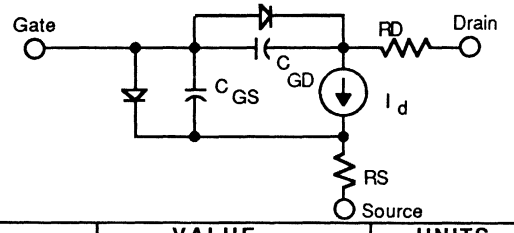
ABSOLUTE MAXIMUM RATINGS
(Beyond which useful life may be impaired)

SYMBOL	PARAMETER	ABSOLUTE MAXIMUM RATINGS
V_{DS}	Drain to Source Voltage	15V
V_{GS}, V_{GD}	Gate to Source Voltage	-15V
V_{GD}	Gate to Drain Voltage	- 15V
V_{ISOL}	Isolation Voltage Between FETs	50V
I_G	Gate Forward Biased Current	20 mA
I_D, I_S	Continuous Drain/Source Current	50mA
I_D, I_S	Pulsed Drain/Source Current	100mA
P_D	Total Power Dissipation -- Per Chip -- Per FET	1.5W 400mW
T_{STOR}	Storage Temperature	- 60°C to + 150°C

SPICE PARAMETERS

The following parameters may be used as a first order approximation with the Berkeley Spice Version 2 G JFET, Model. All parameters are normalized to 1µm FET width. For the16G020 FETs: W = 400µm.

FET EQUIVALENT CIRCUIT



SYMBOL	PARAMETER	VALUE	UNITS
VTO	Pinchoff Voltage	-0.90	V
BETA	Gain Coefficient	1.48×10^{-4}	$A/V^2 \times \mu m$
LAMBDA	DC Drain Cond. Coefficient (Note1)	0.05	V^{-1}
RS	Source Resistance	1055	$\Omega \times \mu m$
RD	Drain Resistance	1055	$\Omega \times \mu m$
CGS	Gate-Source Capacitance (Note 2)	1.3×10^{-15}	F/µm
CGD	Drain-Gate Capacitance (Note 2)	0.62×10^{-15}	F/µm
IS	Gate Diode Saturation Current	2×10^{-14}	A/µm
PB	Barrier Height For Capacitance [C(V)]	0.85	V

Notes : 1. Varies Substantially from dc (typically LAMBDA = 0.023 V^{-1}) to ac operating frequencies (typically LAMBDA = 0.13 V^{-1} for f > 100 KHz).

2. The SPICE JFET model assumes C gs = W x CGS / $\sqrt{1-(Vg-Vs)/PB}$, Cgd = W x CGD / $\sqrt{1+(Vd-Vg)/PB}$ which ignores the fact that both Cgs and Cgd are functions of both Vgs and Vdg. Values calculated for CGS and CGD give average capacitances under typical switching conditions.

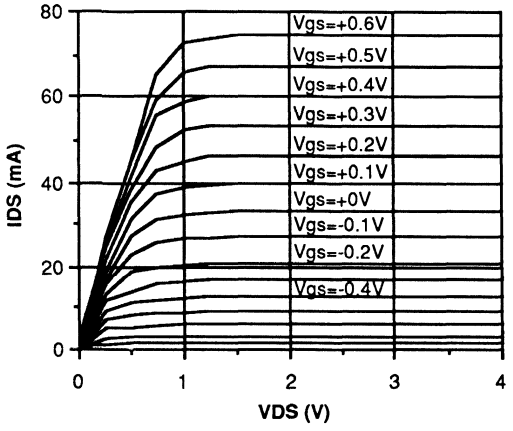
16G020L, 16G020F
ELECTRICAL CHARACTERISTICS (Note 1)

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
V_P	Pinchoff Voltage	V_{DS} = 2.5V	-0.7	-0.9	-1.1	V
I_{DSS}	Saturation Current	V_{DS} = 2.5V, V_{GS} = 0V	23	32	50	mA
C_{gs}	Gate -- Source Capacitance (Die) (Note 3)	V_{DS} = 2.5V, V_{GS} = 0V		0.5		pF
C_{gd}	Gate - Drain Capacitance (Die) (Note 3)	V_{DS} = 2.5V, V_{GS} = 0V		0.2		pF
C_{ds}	Drain -- Source Capacitance (Die) (Note 3)	V_{DS} = 2.5V, V_{GS} = 0V		0.05		pF
g_m	Transconductance	V_{DS} = 2.5V, V_{GS} = 0V	45	63	80	mS
ΔV_P	Pinchoff Voltage Match (Between any FET and the average pinchoff voltage of the chip)	V_{DS} = 2.5V		30		mV
Δg_m	Transconductance Match (Between any FET and the average transconductance of the chip)	V_{DS} = 2.5V, V_{GS} =0V		5		mS
R_{on}	Drain-Source On Resistance	V_{GS} = 0.6V V_{GS} = 0V		10 16	20	Ω Ω
R_s	Source Resistance	I_G =0.8mA		4		Ω
g_{os}	Common Source Output Conductance (Note 2)	V_{DS} = 2.5V, V_{GS} = 0V f > 10 MHz		4.5		mS
V_{BRDS}	Drain-Source Breakdown Voltage (Note 4)	V_{GS} = -1.5V, $I_D \leq$ 0.5mA	9	11		V
V_{BRGS}	Gate-Source Breakdown Voltage	I_D = .1mA		8		V
I_{DS}	Drain-Source Leakage Current	V_{DS} = 2.5V, V_{GS} = - 2.5V		500		nA
I_{GS}	Gate-Source Leakage Current	V_{DS} = 2.5V, V_{GS} = -2.5V		100		nA
F_t	Unity Gain Frequency	V_{DS} = 2.5V, V_{GS} = 0V		22		GHz
N_F	Optimum Noise Figure	V_{DS} = 2.5V, V_{GS} = -0.3V f0 = 1 GHz f0 = 2 GHz f0 = 4 GHz		 .45 .85 1.65		 dB dB dB

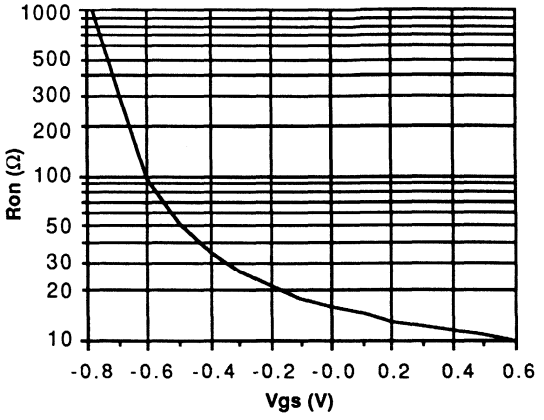
NOTES:
1. Test conditions, unless otherwise stated: TA = 25°C
2. At frequencies below the 10 KHz to 1 MHz range, the common source output conductance is typically at least an order of magnitude lower than the high frequency value given above.
3. For packaged parts, the measured capacitances will be increased by both shunt capacitance (C1G from each pin to ground) and interelectrode capacitance (C12, between adjacent pins). For the flatpack (assuming 0.150" external leads), the shunt capacitance is C1G = 0.25 pf and the interelectrode contribution is C12 = 0.20 pf. In addition, each lead has a series inductance of about 7nH in the flatpack (including the 0.150" Leads). For the leadless chip carrier package these values are C1G = 0.5 pf shunt and C12 = 0.1 pf, with a series inductance of 4nH on each lead. The shunt capacitances are principally to the ground pin on the package, which should be connected to an AC ground to minimize high frequency crosstalk between FETs.
4. Operation at drain to source voltages above VBRDS may involve some degradation in output conductance (gos) and some increase in noise (particularly flicker or "popcorn" noise). These factors should not interfere with switching applications at higher VDS voltage levels.

DEVICE CHARACTERISTICS (Ta = 25°C)

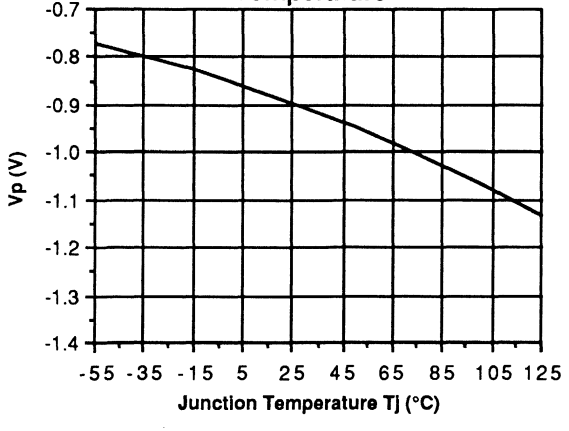
IDS vs. VDS



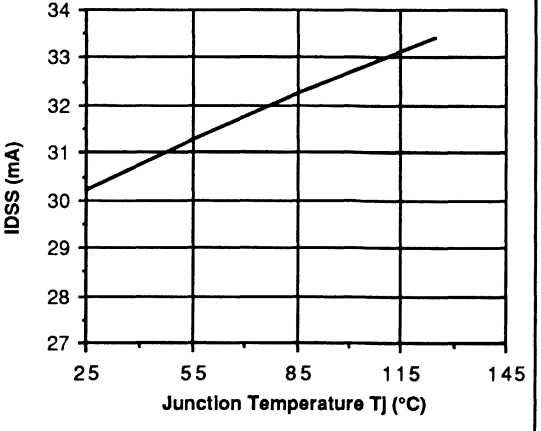
"ON" RESISTANCE VS. VGS



Pinchoff Voltage vs. Temperature



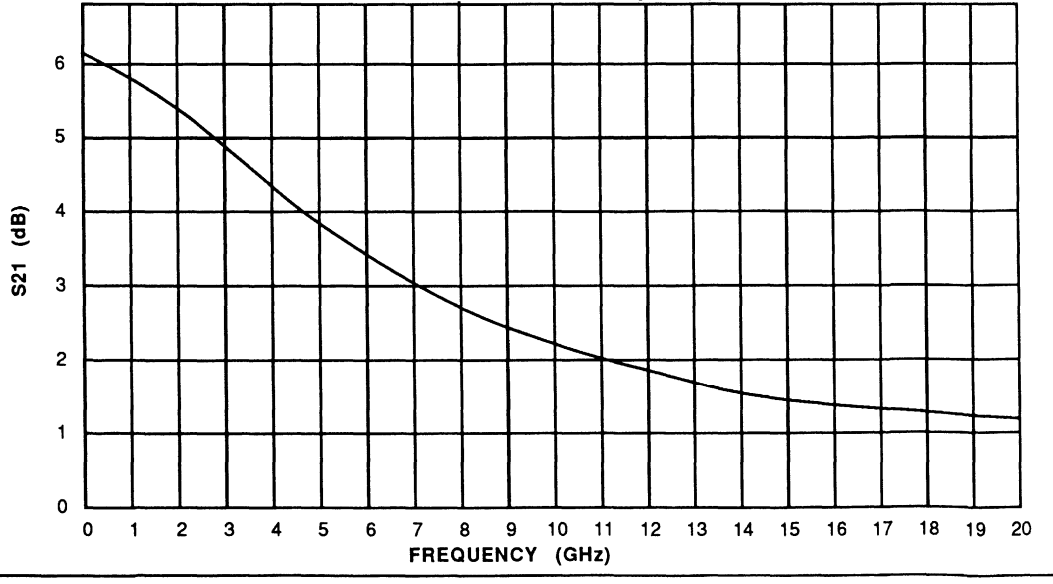
IDSS vs. Temperature



TYPICAL S-PARAMETERS (Vds=2.5V, Vgs=0V)

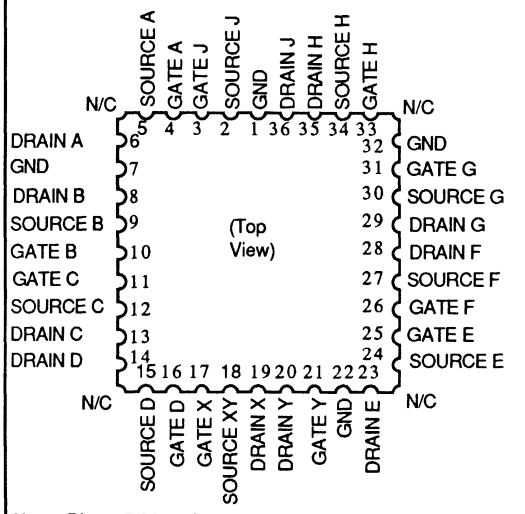
Frequency (MHz)	S11		S21		S12		S22	
	MAG	PHASE	MAG	PHASE	MAG	PHASE	MAG	PHASE
100	.99	-2.6	6.1	178	0.004	8.9	0.56	-1.77
1000	.99	-25.4	5.92	164	0.037	7.5	0.55	-17.4
2000	.97	-48.3	5.46	150	0.068	6.2	0.52	-33.2
2800	.95	-64.6	4.99	140	0.088	5.2	0.497	-44.4
4000	.92	-83	4.33	129	0.11	4.2	0.46	-57.4
5000	.90	-96	3.80	120	0.12	3.4	0.44	-66.6
7000	.88	-115	2.99	108	0.13	2.3	0.41	-80
10000	.86	-130	2.24	95.8	0.14	1.3	0.4	-92
12500	.85	-140	1.81	87.6	0.142	0.5	0.41	-99
16000	.85	-147	1.45	79.1	0.142	-3.8	0.44	-105
18000	.85	-150	1.28	74	0.141	-3.1	0.46	-109
20000	.85	-153	1.14	70	0.14	-6.2	0.48	-111

Insertion Gain vs. Frequency (Vds = 2.5V, Vgs = 0)



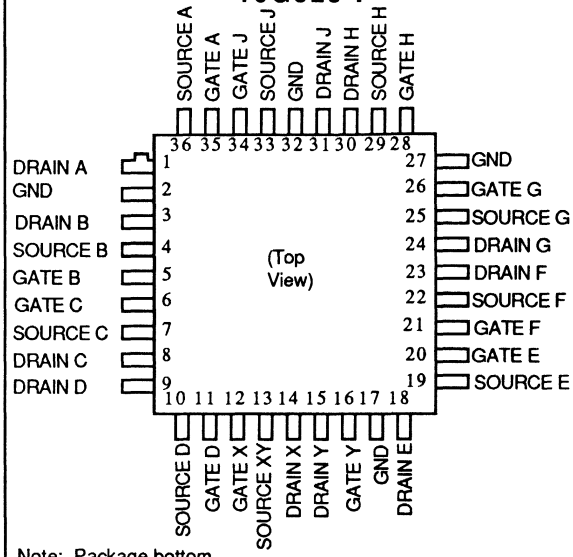
PACKAGE PINOUT DIAGRAM

36 I/O LEADLESS CHIP CARRIER
16G020-L36



Note: Pins 1,7,22 and 32 are internally connected.

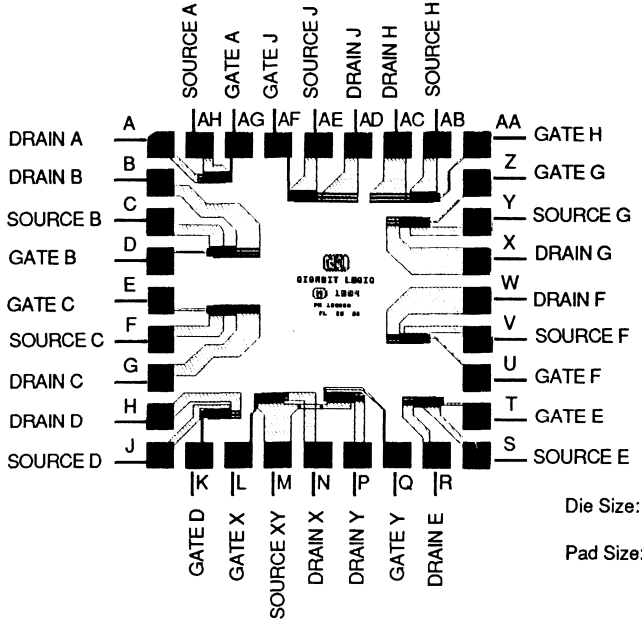
36 LEAD FLATPACK
16G020-F



Note: Package bottom surface and pins 2, 17, 27 and 32 are internally connected .

METALLIZATION AND PAD LAYOUT

16G020-X



Die Size: 1.26 mm x 1.24 mm (0.050" x 0.048")
Pad Size: Top Row 100µm x 75 µm (0.004" x 0.003")
Others 100µm x 100µm (0.004" x 0.003")

Programmable Dual Gate GaAs D-MESFET Array

DISTINCTIVE CAPABILITIES

- 8 dual gate depletion MESFETs on each chip
- f_t =22 GHz frequency response
- -0.9 V pinchoff voltage, 35 mA I_{DSS} (typ)
- Excellent thermal and electrical matching
- Very low feedback Miller capacitance
- High output impedance and reverse isolation
- Available with personalized interconnects in the package for design integration and improved performance
- Available in leadless chip carrier (LCC), flatpack, or die form

APPLICATIONS

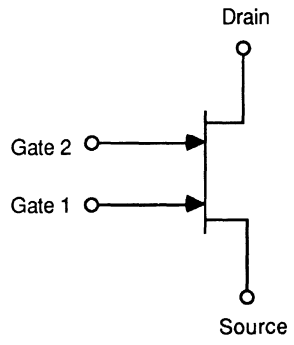
- Low noise amplifiers (broadband, video, IF, RF, or microwave)
- Interface circuitry to digital logic
- Samplers and analog gating circuits
- AGC amplifiers
- RF or microwave dual-gate FET mixers
- Ultra low capacitance buffers
- RF or high speed current sources/ Active load
- Line drivers (digital or analog)

FUNCTIONAL DESCRIPTION

The 16G021 contains 8 dual gate GaAs depletion MESFETs on a single chip. The MESFETs feature a -0.9V pinchoff voltage and very low Miller capacitance, making them ideal for high frequency applications utilizing relatively small signal levels in both digital and analog circuits. The device characteristics of these N-channel, Schottky-gate D-MESFETs are similar to those of silicon N-channel J-FETs. Typical gate1 (gate nearest to the source) voltage ranges between Vg1s = -0.9 V (threshold of drain conductance) to Vg1s = 0.6V (onset of strong gate forward conduction current). The typical gate 2 voltage range is $Vg2D \geq Vg1D + 1.0V$ to $Vg2D \leq Vg1D - 1.0$ V. Vg1 should be no more than 0.6V positive with respect to the source and Vg2 should be no more than 0.6V positive with respect to the drain to avoid strong gate to drain forward conduction. In AGC applications, to reduce gain, Vg2D may be operated near pinchoff (-0.9V). In order to take better advantage of the high frequency characteristics of the FETs in the 16G021, GigaBit offers the option to interconnect FETs and add chip components as necessary inside the package (LCC or Flatpack). Package parasitic capacitance and inductance generally limits the performance of packaged parts. By realizing the interconnects inside the package to form a personalized analog function, the overall effect of package parasitic impedance is reduced since there is less I/O per function.
The 16G021 is fabricated using GigaBit's high volume, GaAs MESFET process technology.

CIRCUIT DIAGRAM

DUAL GATE DEPLETION MESFET
(8 per chip)



ORDERING INFORMATION

PACKAGE TYPE	PART NUMBER
36 I/O Leadless CC	16G021-L36
36 I/O Flatpack	16G021-F
Dice	16G021-X

16G021 FET ARRAY PERSONALIZATION

Please contact factory for special part number.

CIRCUIT DESIGN INTEGRATION USING PERSONALIZED 16G021

GigaBit Logic can integrate certain analog designs by utilizing the 8 dual gate MESFETs in the 16G021. Chip resistors and capacitors can also be added in the package cavity to realize more complex circuits. By interconnecting 16G021 FETs inside the package, GigaBit can offer personalized analog functions with better performance than when the interconnects are external. First, the effect of package and wire bond parasitic capacitance and inductance is reduced since there are fewer I/O per function. Chip capacitors and resistors can be attached close to the die bond pads in order to minimize wire bond length. Secondly, since there are fewer overall I/O per package, it is possible to adopt a Ground-Signal-Ground approach for the pin-out. This lowers cross capacitance between adjacent pins reducing cross talk as well as potential jitter in the device.

PROGRAM FLOW FOR PROTOTYPES

GigaBit will review or propose a circuit schematic to personalize the 16G021 to the desired function. Prototypes are custom wire-bonded during assembly. Chip resistors and capacitors are added in the package as necessary. This approach has two main advantages: no Non-Recurring engineering Expenses (NRE) and a quick turnaround time (2 to 4 weeks). Since there is no NRE, designers have total flexibility to try out a design and modify it if necessary.

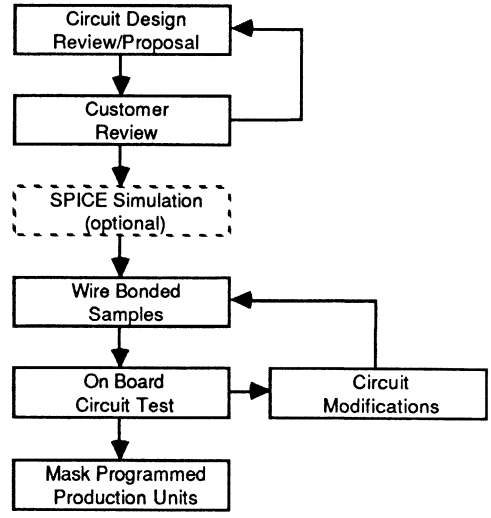
GigaBit can provide, as an option, complete simulation of the circuit utilizing its proprietary spice model.

PROGRAM FLOW FOR PRODUCTION DEVICES

Production devices are customized via mask programming. The interconnects are realized in the IC substrate by changing the top metal layer mask of the 16G021.

Mask programming for production devices is advised to improve reliability and reproducibility compared with wire bonded prototypes. In addition, mask programmed ICs require less assembly work and are lower in cost compared with wire bonded prototypes.

DESIGN INTEGRATION PROGRAM FLOW

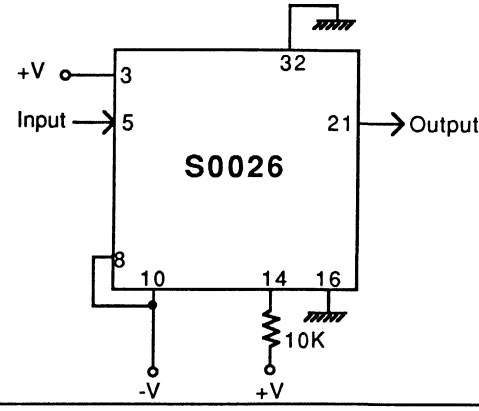


EXAMPLES

Some examples of analog ICs developed using the 16G021 FET arrays are:

- High Impedance Unity Gain Buffer: Rin ≥ 3 MΩ @ DC, input leakage current ≤ 2 nA, input capacitance 0.4pf to 0.7pf (S0026)
- Microwave Mixers
- AGC Amplifiers

High Impedance Unity Gain Buffer



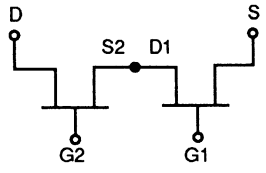
ABSOLUTE MAXIMUM RATINGS
(Beyond which useful life may be impaired)

SYMBOL	PARAMETER	ABSOLUTE MAXIMUM RATINGS
V_{DS}	Drain to Source Voltage	15V
V_{G1S}	Gate 1 to Source Voltage	-15V
V_{G2D}	Gate 2 to Drain Forward Voltage	-15V
V_{ISOL}	Isolation Voltage Between FETs	50V
I_{G1}, I_{G2}	Gate Forward Biased Current	20 mA
I_D, I_S	Continuous Drain/Source Current	60mA
I_D, I_S	Pulsed Drain/Source Current	100mA
P_D	Total Power Dissipation -- Per Chip	1.5W
	-- Per FET	400mW
T_{STOR}	Storage Temperature	- 60°C to + 150°C

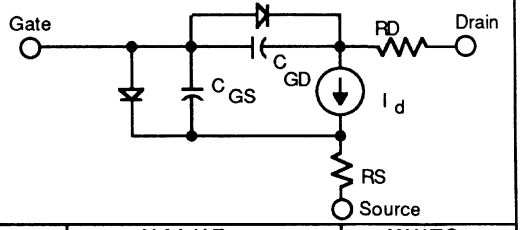
SPICE PARAMETERS

The following parameters may be used as a first order approximation with the Berkeley Spice Version 2 G JFET, Model. All parameters are normalized to 1µm FET width. For the 16G021 FETs: W = 400µm.

DUAL GATE FET EQUIVALENT CIRCUIT



SINGLE GATE FET EQUIVALENT CIRCUIT



SYMBOL	PARAMETER	VALUE	UNITS
VTO	Pinchoff Voltage	-0.90	V
BETA	Gain Coefficient	1.48×10^{-4}	$A/V^2 \times \mu m$
LAMBDA	DC Drain Cond. Coefficient (Note1)	0.05	V^{-1}
RS	Source Resistance	1055	Ω x µm
RS2	Source Resistance of FET 2	100	Ω x µm
RD	Drain Resistance	1055	Ω x µm
RD1	Drain Resistance of FET 1	100	Ω x µm
CGS	Gate-Source Capacitance (Note 2)	1.3×10^{-15}	F/µm
CGD	Drain-Gate Capacitance (Note 2)	0.62×10^{-15}	F/µm
IS	Gate Diode Saturation Current	2×10^{-14}	A/µm
PB	Barrier Height For Capacitance [C(V)]	0.85	V

Notes : 1. Varies Substantially from dc (typically LAMBDA = 0.023 Y^{-1}) to ac operating frequencies (typically LAMBDA = 0.13 V^{-1} for f > 100 KHz).

2. The SPICE JFET model assumes C gs = W x CGS / $\sqrt{1-(Vg-Vs)/PB}$, Cgd = W x CGD / $\sqrt{1+(Vd-Vg)/PB}$ which ignores the fact that both Cgs and Cgd are functions of both Vgs and Vdg. Values calculated for CGS and CGD give average capacitances under typical switching conditions.

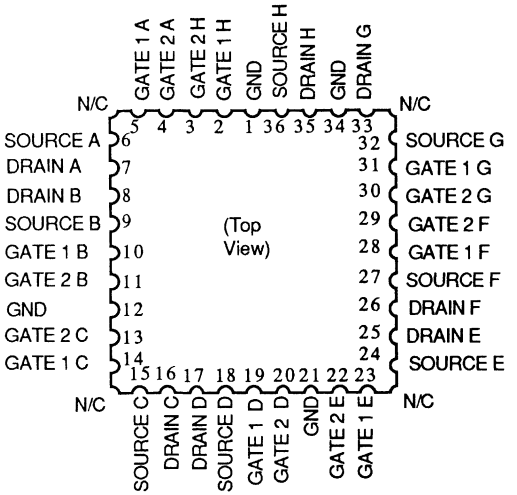
16G021L, 16G021F
ELECTRICAL CHARACTERISTICS (Note 1)

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
V_P	Pinchoff Voltage (Gate 1)	V_{DS} = 3.0V, V_{G2S}=1.5V	-0.7	-0.9	-1.1	V
I_{DSS}	Saturation Current	V_{DS}= 3V, V_{G1S}= 0V,V_{G2S}=1.5V	23	32	50	mA
C_{gs}	Gate -- Source Capacitance (Die) (Note 3)	V_{DS}= 3V, V_{G1S}= 0V,V_{G2S}=1.5V		0.5		pF
C_{g1d}	Gate 1 - Drain Capacitance (Die) (Note 3)	V_{DS}= 3V, V_{G1S}= 0V,V_{G2S}=1.5V		0.05		pF
C_{g2d}	Gate 2 -- Drain Capacitance (Die) (Note 3)	V_{DS}= 3V, V_{G1S}= 0V,V_{G2S}=1.5V		0.2		pF
g_{m1}	Transconductance (Gate 1)	V_{DS}= 3V, V_{G1S}= 0V,V_{G2S}=1.5V	45	63	80	mS
ΔV_P	Gate 1 Vp Match (Between any FETand the average pinchoff voltage of the chip)	V_{DS} = 3.0V, V_{G2S}=1.5V		30		mV
Δg_m	gm Match (Between any FET and the average transconductance of the chip)	V_{DS}= 3V,V_{G1S}=0V,V_{G2S}=1.5V		5		mS
R_{on}	Drain-Source On Resistance	V_{G1S}= V_{G2S}= 0.6V V_{G1S}= V_{G2S}=0V		20 30		Ω Ω
R_s	Source Resistance	I_G =0.8mA		8		Ω
g_{os}	Common Source Output Conductance (Note 2)	V_{DS} = 3.0V, V_{G1S}= 0V V_{G2S}=1.5V , f > 10 MHz		0.3		mS
V_{BRDS}	Drain-Source Breakdown Voltage (Note 4)	V_{G1S}= -1.5V, $I_D \leq$ 0.5mA V_{G2S}=1.5V	11	13		V
F_t	Unity Current Gain Frequency	V_{DS}= 2.5V,V_{G1S}= 0V,V_{G2S}=1.5V		22		GHz
N_F	Optimum Noise Figure	V_{DS}= 2.5V,V_{G1S}= -0.3V V_{G2S}= 1.5V				
		f0 = 1 GHz		.45		dB
		f0 = 2 GHz		.85		dB
		f0 = 4 GHz		1.65		dB

NOTES:
1. Test conditions, unless otherwise stated: TA = 25°C
2. At frequencies below the 10 KHz to 1 MHz range, the common source output conductance is typically at least an order of magnitude lower than the high frequency value given above.
3. For packaged parts, the measured capacitances will be increased by both shunt capacitance (C1G from each pin to ground) and interelectrode capacitance (C12, between adjacent pins). For the flatpack (assuming 0.150" external leads), the shunt capacitance is C1G = 0.25 pf and the interelectrode contribution is C12 = 0.20 pf. In addition, each lead has a series inductance of about 7nH in the flatpack (including the 0.150" Leads). For the leadless chip carrier package these values are C1G = 0.5 pf shunt and C12 = 0.1 pf, with a series inductance of 4nH on each lead. The shunt capacitances are principally to the ground pin on the package, which should be connected to an AC ground to minimize high frequency crosstalk between FETs.
4. Operation at drain source voltages above VBRDS may involve some degradation in output conductance (gos) and some increase in noise (particularly flicker or "popcorn" noise). These factors should not interfere with switching applications at higher VDS voltage levels.

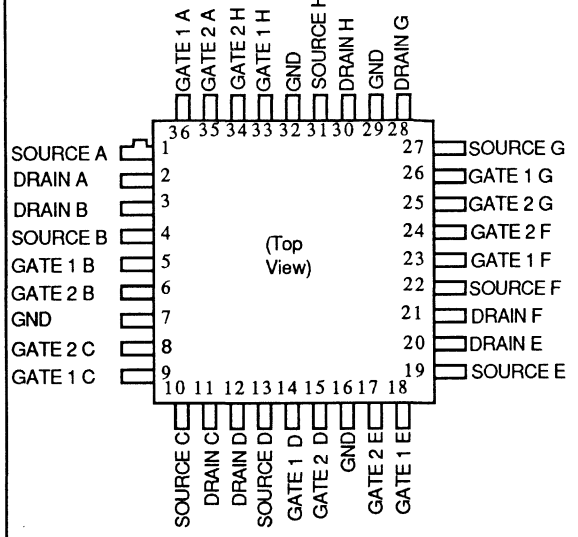
PIN FUNCTION DRAWINGS

36 I/O LEADLESS CHIP CARRIER
16G021-L36



Note: Pins 1, 12, 21, and 34 are internally connected .

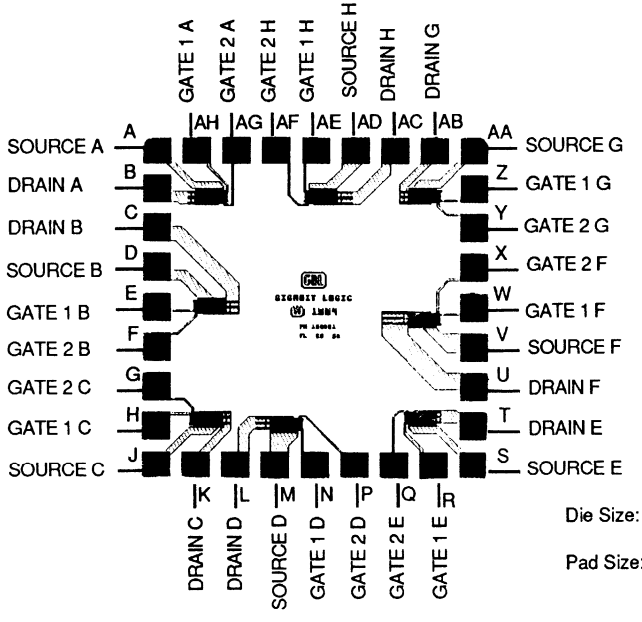
36 LEAD FLATPACK
16G021-F



Note: Package bottom and pins 7, 16, 29 and 32 are internally connected.

METALLIZATION AND PAD LAYOUT

16G021-X



Die Size: 1.26 mm x 1.24 mm
(0.050" x 0.048")
Pad Size: Top Row 100µm x 75 µm
(0.004" x 0.003")
Others 100µm x 100µm
(0.004" x 0.003")

Clock & Data Recovery Circuit
2.0 Gbit/s NRZ Data Rate

DISTINCTIVE CAPABILITIES

- Clock recovery and data retiming and regeneration subsystem on a chip
- 2.0 Gbit/s performance with ext. clock source; 1.0 Gbit/s performance with on-chip VCO
- Pat. pending, self-acquiring PLL GaAs IC design
- On-chip VCO powered separately to allow use of optional external clock source
- Interfaces to 10G041A Time Division DEMUX easily
- Loop bandwidth externally controllable for fast acquisition time
- Availabie in C-leaded or leadless chip carriers, or as unpackaged die
- Demo board available - 90GCDR(-DX)

APPLICATION

- High speed fiber optic and microwave receivers and repeaters

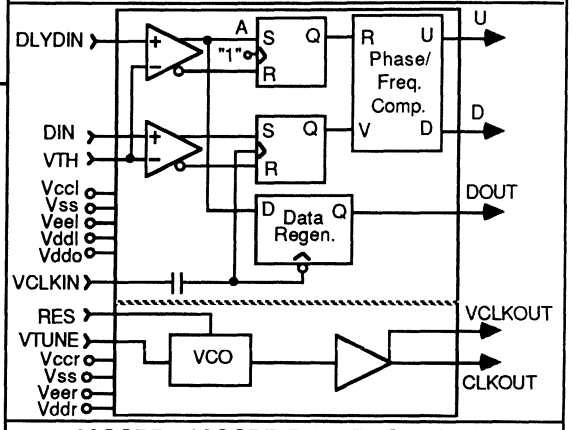
FUNCTIONAL DESCRIPTION

The 16G040 contains the high speed analog and digital circuitry needed to implement a phase locked loop (PLL) for both clock extraction from high speed digital data streams, as well as data retiming and regeneration. All PLL components are on-chip excluding the loop filter. Using the on-chip VCO as a clock source, the 16G040 can be operated from >10 Mbit/s to 1.0 Gbit/s. Performance with an external clock source extends to >2.0 Gbit/s. The 16G040 is available in four forms:

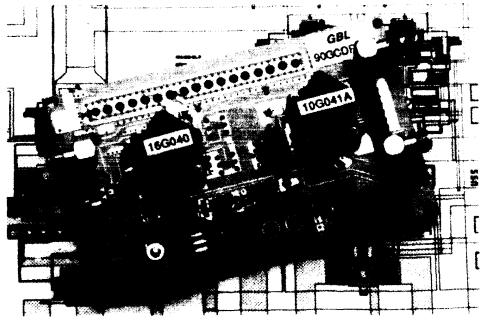
1. The 16G040-2C and 16G040-2L are packaged in GigaBit's standard 40 I/O C-leaded and leadless ceramic chip carrier packages, respectively.
2. Unpackaged dice (16G040-2X).
3. As a demonstration board: part number 90GCDR user tunable from ~150 Mbit/s to 1.0 Gbit/s .
4. As in "3" but with a 10G041A-4 1:8 DEMUX incorporated on the board: part number 90GCDR-DX.

Unlike other clock and data recovery approaches which first filter the clock component from incoming data and then retimes it using the extracted clock, the16G040 is capable of synchronizing an on-chipVCO or external clock source directly to an incoming digital data stream, while simultaneously retiming and regenerating the data stream. In operation, the 16G040-based PLL is capable of unaided frequency acquisition, eliminating the need for special circuits to "pull" the loop into lock when the incoming data rate differs from the initial frequency of the clock source. Also, compared with other approaches to clock recovery, the 16G040 offers the advantages of an IC-based PLL approach including lower power, low cost and high reliability.

16G040 BLOCK DIAGRAM



90GCDR, 90GCDR-DX DEMO BOARD



ORDERING INFORMATION

Package/Product	Part No. (Speed, min. @ 25°C)
C-leaded CC	16G040-2C (≤1.0 Gbit/s)
Leadless CC	16G040-2L (≤1.0 Gbit/s)
Dice	16G040-2X (≤2.0 Gbit/s)
Demo board	90GCDR (tunable .15 to 1.0 Gbit/s)
Board w/DEMUX	90GCDR-DX (tunable .15 to 1 Gbit/s)

Because the device is implemented as a PLL, the center frequency can be tuned over a wide range and if an external loop filter and clock source are used, their parameters can be chosen to realize extremely fast acquisition time loops. All power supplies to the on-chip VCO are separate so that it can be powered down to decrease power dissipation when the 16G040 is used with an external clock source.

The 16G040 requires an external resonator when the on-chip VCO is used. This resonator is implemented as a 1/4 wavelength tunable microstrip stub on the 90GCDR (-DX) board. Other resonators can be used with the packaged device or unpackaged die. The 16G040 also requires a fixed external delay (non-critical, between 1/4 and 1/2 bit period) between inputs DIN (Data In) and DLYDIN (Delayed Data in). GigaBit Application Note 7, titled "Application of the 16G040 Clock and Data Recovery Circuit" provides necessary background material and should be carefully reviewed.

A key subcircuit included in the 16G040 is the phase/frequency comparator. This component is also available as a stand-alone product, the 16G044, with a detailed datasheet which supplements the information contained in this datasheet.

The 16G040 is a member of GigaBit's family of components for high speed fiber optic and microwave communications which include the 10G040A time division multiplexer, the 10G041A time division demultiplexer and the16G044 phase/ frequency comparator. The 16G040 utilizes GigaBit's production proven GaAs MESFET process technology.

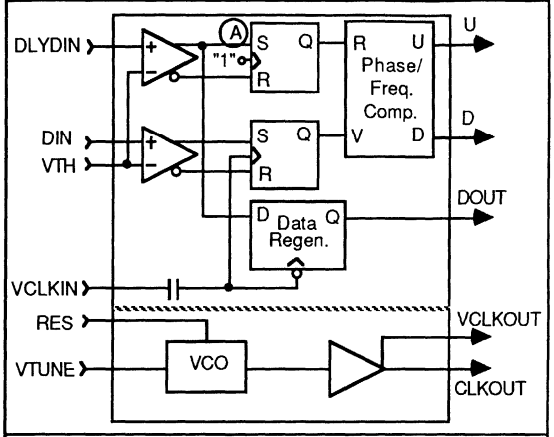
16G040 PLL OPERATION

When interconnected to form a phase locked loop as shown in the Typical PLL Circuit diagram (Fig. 2), two modes of operation are possible: 1) the VCO frequency is equal to the input data rate; that is, the loop is in frequency lock but is not phase locked; 2) the initial VCO frequency is unequal to the input data rate but the data rate is within the loop capture range.

PHASE OFFSET OPERATION

When the loop is in frequency but not phase lock, the outputs of the phase/frequency comparator (PFC) will produce pulses which, when low pass filtered and subtracted, provide an error signal that is applied to the Vtune input of the VCO to correct the phase offset. With reference to the 16G040 block diagram (Fig. 1), the signal on the PFC "V" input leads the signal on the"R" input when the rising edge of the clock applied to the clocked S-R latch leads the rising edge of the delayed data input applied to the transparent S-R latch ("A" in the block diagram). "V" lags" R" when the rising edge of the clock input lags the signal at A .

Fig. 1: 16G040 BLOCK DIAGRAM



PIN DESCRIPTIONS

DIN	High speed, serial data input.
DLYDIN	Delayed data input.
VTH	The threshold bias control to the input comparators. -1.3V≤Vcm≤0V.
VCLKIN	AC-coupled clock input, typically driven from the VCLKOUT pin.
RES	1/4 wavelength stub resonator connection. The stub is tuned by shorting along its length to VCCR (+5V).
VTUNE	DC tuning voltage input to the VCO. Nom. tuning voltage range is -2.5V to +2.5V.
U, D	Phase error outputs of the phase/freq. comparator.
VCLKOUT, CLKOUT	The VCO output pins. These pins are interchangeable.
DOUT	Reclocked, regenerated data output.
Vccl,Vccr	+5.0V power supply connections.
Vss	-3.4V power supply.
Veel,Veer	-5.2V power supply pins.
Vddl,Vddr	Ground connections.
Vddo	Output driver ground connection for data regenerator and phase/freq. comparator.

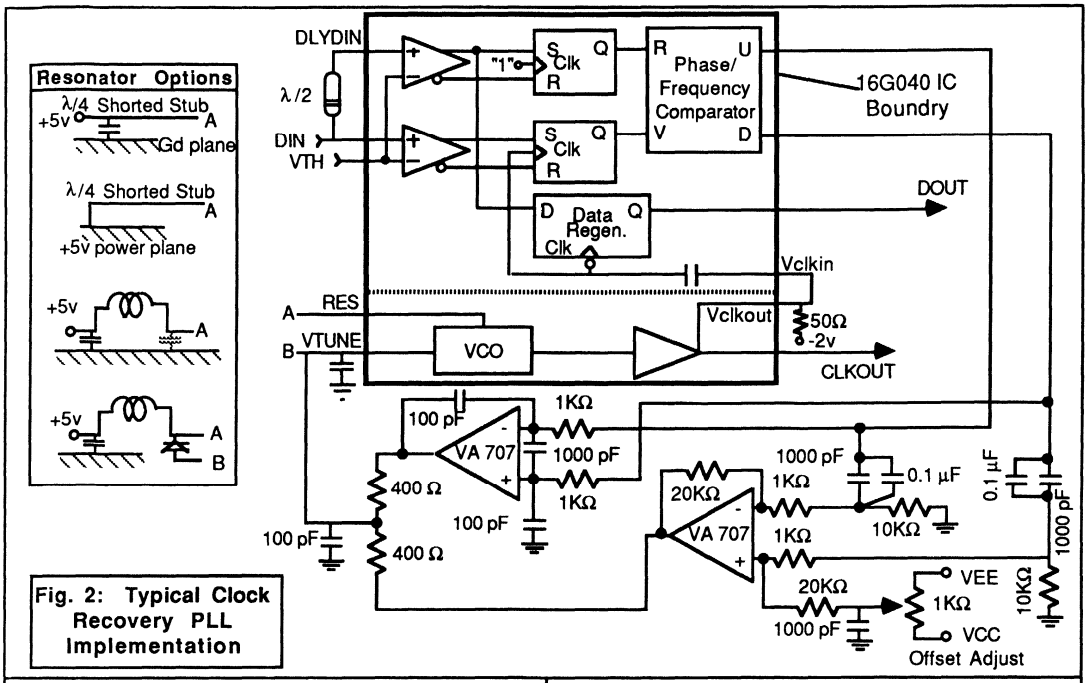


Fig. 2: Typical Clock Recovery PLL Implementation

The relative phase of "V" with respect to "R" is sensed by a phase/frequency comparator. The phase/ frequency comparator is an edge-triggered digital device which produces pulses in "U" when "R" leads "V" and in "D" when "R" lags "V". The width of these pulses is equal to the amount by which "R" leads or lags "V". Only one output is active at a time. The difference between the "U" and "D" outputs is fed back to the VCO through an appropriate loop filter, which then "servos" the VCO in the direction necessary to correct this phase offset. When the loop is in lock, the rising edges of "A" are exactly lined up with the rising edges in "CLK". This ensures that the falling edge-triggered D- type flip-flop, which is used as a "decision circuit" to detect the digital data, is clocking precisely in the middle of the data bit, and thus has maximum timing margin to prevent jitter-induced bit errors.

When the loop is phase locked, then both the PFC "U" and "D" outputs are low, resulting in a zero error voltage being applied to the loop filter. Therefore, the tendency is for the loop to hold its frequency once it is locked. This condition also occurs in the absence of any rising edges (often called "missed transitions") in the input data.

When the loop is locked, missing transitions will not cause loss of lock as long as the frequency of transitions exceeds 10 times the loop filter cutoff frequency, as a rule of thumb. However, during

DEFINITION OF TERMS

LOOP CAPTURE RANGE

The frequency range centered about the initial VCO free-running frequency over which the loop can acquire lock with the input signal. The capture range is a measure of how close the input signal must be in frequency to that of the VCO to acquire lock. The "capture range" can assume any value within the lock range and depends primarily upon the band edge of the low pass filter together with the closed loop gain of the system.

LOOP LOCK RANGE

The frequency range centered about the initial VCO free-running frequency over which the loop can track the input signal once lock has been achieved. The lock range is limited by the range of error voltage that can be generated by the loop filter and the corresponding VCO frequency deviation produced. The lock range is essentially a dc parameter and is not affected by the band edge of the low pass filter.

LOOP ACQUISITION TIME

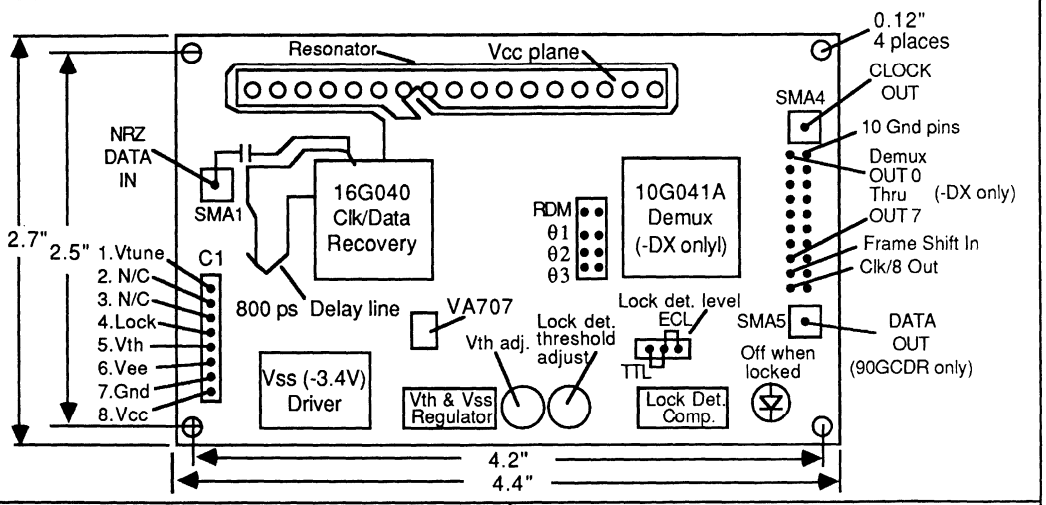
The total time taken by the PLL to establish lock is called the acquisition time. Acquisition time depends on the initial frequency and phase differences between the two signals as well as on the overall loop gain and the low pass filter bandwidth.

acquisition, long strings of "1's" and "0's" will cause an increase in loop acquisition time since these strings of constant data present no phase information to the loop. In this case, the effective phase detector gain factor (Kd) is reduced, according to: Kd effective = Ptr X Kd where Ptr is given by (number of transitions) ÷ (number of bits). This factor can be called the "probability of transitions", or more accurately, the "transitions ratio" and is a measure of the spectral richness at the clock frequency of a digital data stream. A lower Kd (all other factors constant) lowers the closed loop gain of the PLL, resulting in a longer acquisition time.

FREQUENCY ACQUISITION

When the initial VCO frequency is unequal to the input data rate, the phase/frequency comparator produces "beat notes" which drive the VCO in the direction which will correct the frequency error. This acquisition process is highly complex and does not lend itself to simple mathematical analysis. The capture range of the loop is a function of the standard PLL parameters such as the phase detector gain, loop filter bandwidth, VCO control gain and the delay between the DIN and DLYDIN pins.

Fig. 3: 90GCDR (-DX) CLOCK & DATA RECOVERY DEMONSTRATION BOARD



Introduction

The 90GCDR/90GCDR-DX is a duroid on glass-epoxy PCB which contains the 16G040-2L clock and data recovery GaAs IC configured to form a complete PLL for clock recovery from, and retiming/regeneration of, an incoming NRZ format high speed data stream. The 90GCDR contains only the 16G040 clock/data recovery IC; the 90GCDR-DX contains the 16G040 as well as a 10G041A-4 1:8 time division demultiplexer IC. The board features a user-tunable 1/4 wavelength microstrip stub resonator which is used to set the center frequency (Fc) of the VCO by shorting along its length to VCC. The resonator is designed to allow a minimum Fc of approximately 150 MHz (corresponding to 150 Mbit/s) up to a maximum Fc of approximately 1000 MHz (corresponding to 1 Gbit/s). Lower data rates may be accomodated only if a supplementary fixed capacitor or varactor is installed on the board or if a coax delay line is used to supplement the length of the on-board resonator. The selected center frequency can be varied by moving the VCC short to another location along the resonator. The "Vtune" pin is connected to the loop filter op-amp output. This pin can be used to monitor the action of the loop filter in closed loop or to measure the VCO gain constant when the loop is open. The board also provides a visual lock detect signal as well as a selectable ECL or TTL logic level lock detect signal on pin "Lock". The threshold level of the 16G040 input comparators can also be varied under user control over a -1.0V to -1.5V range through application of the

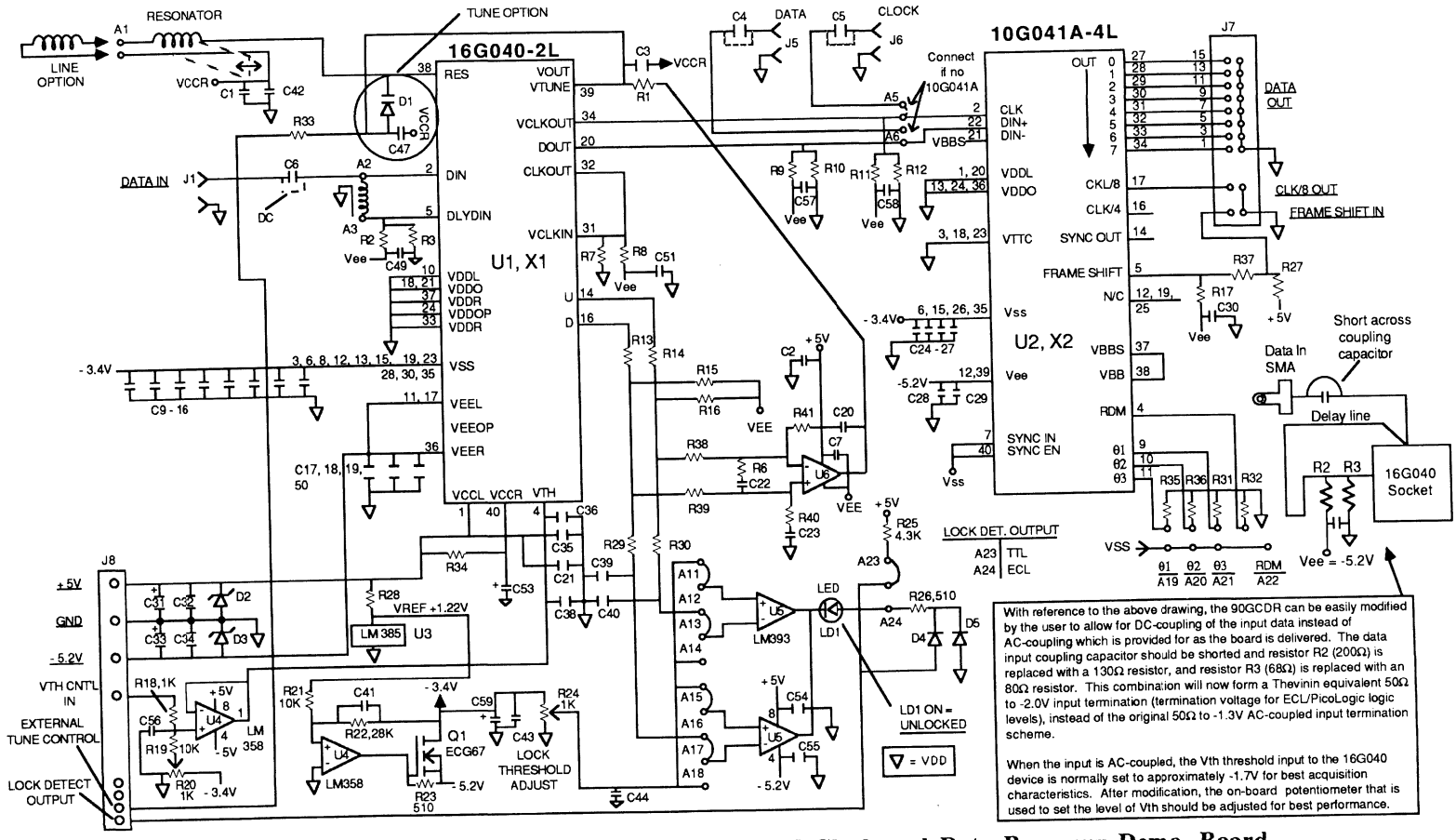
desired voltage on pin "Vth" (otherwise Vth defaults to approx. -1.3V via an on-board regulator). The Vth input can also be used to gate the incoming data (setting Vth equal to either Gnd or Vss (-3.4V) will disable the input data) to provide one means to assist in measuring capture time characteristics. The 90GCDR(-DX) requires -5.2V (pin "Vee") and +5.0V (pin "Vcc") power supplies.

90GCDR (-DX) Operation

The resonator is pre-tuned prior to shipment to a frequency in the range of 600 to 650 MHz and the length of the delay line in the delayed data input path is set to just under 1/2 bit period at 600 MHz. The length of the delay line in picoseconds is not critical, although delays close to 1/2 bit period provide the maximum capture range and delays longer than 1/2 bit period are not recommended since the phase/frequency comparator response will be distorted and the loop will not lock. If the resonator is user-tuned to a higher frequency, it may be necessary to shorten the length of the on-board microstrip delay line by cutting and reconnecting it to a shorter total length. Power is applied by providing -5.2V (Vee) on pin 6, Gnd on pin 7 and +5.0V (Vcc) on pin 8 of the 8 pin connector C1 shown in the diagram. The Vth adjust pot. is set to provide approx. -1.3V to the 16G040 Vth input pin (sets the threshoid voltage of the two input comparators; proper setting of this pot is important for achieving optimum capture range) and the Lock detector threshold adjust pot. is set so that the LED is off when lock is achieved. The lock detect LED may also be off when incoming data is removed. NRZ format high speed data is applied to the board via SMA connector number 1. The recovered, phase locked clock is available on SMA4 and the retimed, regenerated data is available on SMA5. The data input, clock output and data output are all AC-coupled. The clock and data outputs (SMA 4 and 5) can be directly connected to the 50Ω input of a high speed oscilloscope terminated to ground for monitoring purposes. SMA5 (data output) is not installed on the 90GCDR-DX board. The 16G040's input comparators are typically sensitive to as small as a 300 mVp-p input data swing at maximum operating frequency. The 10 pin connector adjacent to the Demux. provides the 8 data outputs as well as the clock ÷ 8 output and the frame shift signal input. Reference should be made to the 10G041A datasheet for complete Demux operational details. The 4 pairs of jumpers adjacent to the Demux for the ripple data mode control (RDM) and the clock ÷ 8 phase control bits (phi 1,2,3), are designed to default to the logic high state and are set to logic lows when the jumper connects the horizontally adjacent pins.

User Notes

1. The loop filter design implemented at delivery is optimized for a center frequency in the range of approximately 600 to 650 Mbit/s. If Fc is significantly altered by the user by moving the resonator shorting bar, it may be necessary to modify the loop filter design for proper performance at the new Fc. As noted previously, it may also be necessary to modify the length of the data input delay line.
2. The (90GCDR-DX) data and CLK/8 outputs from the DEMUX to the 8 square pin edge connector are ECL level compatible. This means that these signal lines must be terminated through a termination resistance (normally 50Ω) to a pull-down voltage (normally -2.0V). The edge connector is not terminated on the board. Once properly terminated, these outputs can be viewed using a standard high impedance oscilloscope plug-in since they are relatively low speed, bearing in mind that the edge rates are much faster than a low frequency scope will be able to show. The bandwidth of the scope should exceed 1.5 times the data rate if the true edge rates are to be displayed (scope bandwidth should encompass the third harmonic of the data output waveform).
3. It is important to remember, when first testing the board, that a 300 MHz sinewave data input is equivalent to a 600 Mbit/s NRZ data stream - not a 300 Mbit/s NRZ stream.
4. The circuit is designed to capture as data is turned on at a frequency within the capture range, and will not necessarily capture if the signal is swept in and out of the lock range. This is consistent with its intended use as a clock recovery circuit in fiber optic networks where capture must occur when data is provided and the data frequency does not vary outside of the capture or acquisition window.
5. Some additional cooling is recommended (e.g. 50 lfm of forced air) to assure long term reliability.
6. The data input to the 90GCDR is normally AC coupled. Bit error rate performance may be improved when the data input is DC coupled. Simple instructions for this modification are noted on the 90GCDR schematic.



With reference to the above drawing, the 90GCDR can be easily modified by the user to allow for DC-coupling of the input data instead of AC-coupling which is provided for as the board is delivered. The data input coupling capacitor should be shorted and resistor R2 (200Ω) is replaced with a 130Ω resistor, and resistor R3 (68Ω) is replaced with an 80Ω resistor. This combination will now form a Thevinin equivalent 50Ω to -2.0V input termination (termination voltage for ECL/PicoLogic logic levels), instead of the original 50Ω to -1.3V AC-coupled input termination scheme.

When the input is AC-coupled, the Vth threshold input to the 16G040 device is normally set to approximately -1.7V for best acquisition characteristics. After modification, the on-board potentiometer that is used to set the level of Vth should be adjusted for best performance.

Electrical Schematic - 90GCDR & 90GCDR-DX Clock and Data Recovery Demo. Board

90GCDR & 90GCDR-DX COMPONENTS LISTING

Scht. No.	Description	Scht. No.	Description
U1	16G040-2L (GBL)	J1,J5,J6	SMA connector, PCB, Rt. angle
U2	10G041A-4L (GBL)	J7	2 X10 pin strip
U3	LM385BZ1.2	J8	1 X 8 pin strip
U4	LM358	D1	MMBV 210X Varactor
U5	LM393	D4-8	1N4148
U6	VA707P5	D2,D3	1N5232B
Q1	IRFZ12	LD1	T1 red LED

Schematic No.	Description
C32,34,39,40,41,44,54,55,56,59	100 nF mono, 50V
C2,4,6,7	100 nF chip 0805, 50V
C1	1,000 pF, NPO, chip 0403, 50V
C3	100 pF, NPO, chip 50V
C5,9-18,21,24-29,30,35,36,42,47,49 50-53,57,58	1,000 pF, chip 0805, 50V
C31,33,43	10 mF, 10V
C38	1,000 pF, mono, 50V
C20,22,23	2 nF, chip 0805, 50V
R34	51Ω, 1/8 W, 5%, chip 1206
R3*,R7*,5	68Ω, 1/10W, 5%, chip 0805 (* for AC coupled)
R3,7,10,12	82Ω, 1/10W, 5%, chip 0805 (DC coupled)
R2,8,9,11 **	130Ω, 1/10W, 5%, chip 0805 (DC coupled) ** R8 = 360Ω, 1/10W, 5%, chip 0805, if R7 is deleted.
R2*,R8*,4,6	200Ω, 1/10W, 5%, chip 0805 (* for AC coupled)
R38,R39	3.3KΩ, 1/8W, 5% chip 1206
R23,R26	510Ω, 1/8W, 5%, CF
R13,R33	510Ω, 1/10W, 5% chip 1206
R14	330Ω, 1/8W, 5%, 1206 chip
R18,R28	1KΩ, 1/8W, 5%, CF
R25	4.3KΩ, 1/8W, 5%, CF
R31,32,35,36,40,41	1KΩ, 1/8W,5%,1206 chip
R21	10KΩ, 1/8W, 1%, MF
R19	10KΩ, 1/8W, 5%, CF
R20,24	1KΩ, 1/4W, 5% 1/4"D, 1T POT
R22	28KΩ, 1/8W, 1%, MF
R27,31,32,35,36,37	510KΩ, 1/8W, 5%, 1206 chip
R29,R30	20KΩ, 1/8W, 5%, CF
R15,R16	5.1KΩ, 1/8W, 5%, 1206 chip
R1	200Ω, 1/8W, 5%, chip 1206
A1	Pads to connect external coax for resonator extension
A2,A3	Pads to connect data input delay coax (micro-coax)
A5,A6	Pads to connect J5 and J6 if the 10G041A Demux is not connected
A11-18	Future alternate use
A19-22	3 X 2 pad matrix to control Demux CLK/8 output phase (defaults high)
A25,A26	1 pad pair to control Demux RDM input (defaults high)
A23,A24	1 X 3 pins for selecting logic level (ECL/TTL) of lock detect ouput
X1,X2	High speed sockets, GBL P/N 90GSKT-40L

16G040 ABSOLUTE MAXIMUM RATINGS

(Beyond which useful life may be impaired) (Notes 1, 4)

SYMBOL	PARAMETER	ABSOLUTE MAXIMUM RATINGS	NOTES
TSTOR	Storage Temperature	- 65 °C to + 150 °C	
TJ	Junction Temperature	- 55 °C to + 150 °C	
TC	Case Temperature Under Bias	- 55 °C to + 125 °C	2
VDDO	Output Driver Supply Voltage	VSS to + 1.0 V	
VCC	Supply Voltage	+1.0 V to +7.0 V	
VSS	Supply Voltage	- 4.0 V to + 0.5 V	
VEE	Supply Voltage	- 7.0 V to VSS + 0.5 V	
VIN	Voltage Applied to Any Input; Continuous VSS = - 3.4 V, VEE = - 5.2 V	- 4.0 V to + 0.5 V	
IIN	Current Into Any Input; Continuous	- 0.5 mA to 1.0 mA	
VOUT	Voltage Applied to Any Output	-4.0V to + 7.0 V	3
IOUT	Current From Any Output; Continuous	-100 mA	
PD	Power Dissipation Per Output POUT = (VDDO-VOUT) x IOUT	100 mW	
VTT	Load Termination Supply	-6.0 V to VDDO + 6.0 V	

Notes:
1. All voltages specified with VDDL= VDDR = Gnd. Positive current is defined as current into the device.
2. TC is measured at case top.
3. Subject to IOUT and power dissipation limitations.
4. Power supply sequencing is not necessary, but since the VEE supply is used to bias off the normally-on depletion mode transistors, sustained (>5 secs.) application of VSS in the absence of VEE may result in excessive power dissipation and damage to the device.

16G040 RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN	NOM	MAX	UNITS	NOTES
TC	Case Operating Temperature	0	25	85	℃	1
VDDL,R	Ground Connections		Gnd		V	
VDDO	Output Driver Supply Voltage	-0.8	Gnd	1.0	V	
VCCL,R	Supply Voltage	4.75	5.0	5.25	V	
VSS	Supply Voltage(common in L,C pkgs)	- 3.5	- 3.4	- 3.3	V	
VEEL,R,	Supply Voltage	- 5.5	- 5.2	- 5.1	V	
VTT	Load Termination Supply Voltage	VSS	- 2.0	- 2.0	V	2
RLOAD	Output Termination Load Resistance	25	50	100	Ω	2

Notes:
1. Tcase measured at case top. **HEATSINKING IS REQUIRED.** See GigaBit Application Note 3, "Thermal Management of PicoLogic and NanoRam GaAs Digital IC Families" for a complete discussion of all aspects of device thermal management. Heatsinks are available from GigaBit. See page 8, notes 6 and 7.
2. The RLOAD and VTT combination used is subject to maximum output current and power restrictions.

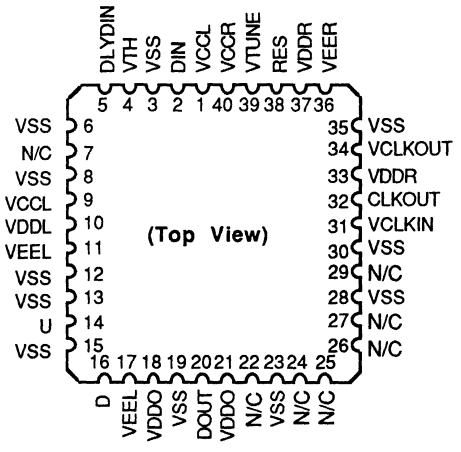
16G040 OPEN LOOP SPECIFICATIONS						
Symbol	**Parameter**	**Min**	**Typ**	**Max**	**Units**	**Test Conditions**
Data Inputs						
VIH	Input high voltage	-1.1		0.0	V	Vth = -1.3V
VIL	Input low voltage	-2.0		-1.5	V	Vth = -1.3V
CMR	Common mode range	-1.8		-0.8	V	
IIN	Input current			300	µA	Vin = VIH max to VIL min
Clock Input						
Vckdc	DC voltage bias	-1.3		0	V	
Pck	Input power	0		13	dBm	
Phase/Frequency Comparator Output						
Kd	Large signal gain constant	500/π	600/π		mV/rad	Alternating 1,0 pattern
kd	Small signal gain constant	125/π	300/π		mV/rad	Alternating 1,0 pattern
VOH	Output peak voltage			-0.4	V	100Ω to Vtt = -2.0V term.
VOL	Output low level voltage	Vtt	-1.9	-1.7	V	100Ω to Vtt = -2.0V term.
Data and Clock Outputs						
VOH	Output high level voltage	-0.8	-0.5	-0.3	V	50Ω to Vtt = -2.0V term.
VOL	Output iow level voltage	Vtt	-1.8	-1.7	V	50Ω to Vtt = -2.0V term.
tdD	Clock output falling edge to data output delay		TBD		ps	
VCO Characteristics						
Kv	VCO gain constant		4		MHz/V	@600 MHz, 1/4 λ stub res.
Δfv	VCO freq. drift vs. temp.	-30		-60	KHz/°C	@400 MHz inclu. resonator
Vin	Vtune input voltage	-5.0		2.5	V	
Cres	Resonator input capacitance		1.5		pf	Package cap. to adjacent leads
Power Supply Currents						
ICCL	Loop components supply		63		mA	
IEEL	currents		-128		mA	
ICCR	Resonator & VCO supply		14		mA	
IEER	currents		-30		mA	
ISS	Common VSS supply current		-121		mA	

TYPICAL 90GCDR (-DX) DEMO BOARD CLOSED LOOP SPECIFICATIONS						
Symbol	**Parameter**	**Min**	**Typ**	**Max**	**Units**	**Notes & Test Conditions**
fc	VCO center frequency	150	600	1000	MHz	Resonator set at 600 MHz at shipment
fd	Input NRZ data rate	150	600	1000	Mbit/s	
Δfc	Loop capture range		fc±8		MHz	@600 MHz
fl	Loop lock (tracking) range		fc±10		MHz	@600 MHz
tacq	Loop acquisition time		250		µs	@600 MHz, 2exp7-1 pseudorandom data
tj	Clock output RMS jitter in lock		50		ps	
n	Max. run length of consecuitve 1s or 0s to maintain lock		23		bits	@600 MHz, 2exp23-1 pseudorandom data
Vin	Input data level to maintain lock	200	300		Vp-p	@600 MHz

NOTES: Ta = 25°C, Vcc = 5.0V, Vee = -5.2V, Vth = -1.3V. Data input is 2exp7-1 psuedorandom bit stream, 300 mVp-p.

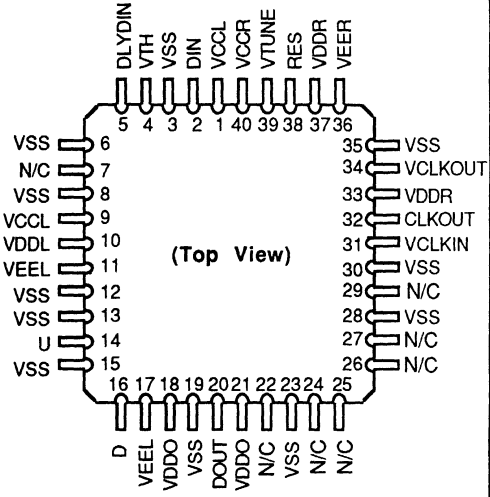
PIN FUNCTIONS - PACKAGE TYPES "L" AND "C"

40 I/O LEADLESS CHIP CARRIER



NOTES:
Pin 1 is marked for orientation. N/C = no connection.

40 I/O C-LEADED CHIP CARRIER



NOTES:
Pin 1 is marked for orientation. N/C = no connection.

Phase/Frequency Comparator 1GHz Input Frequency

DISTINCTIVE CAPABILITIES

- Rising edge-triggered design
- Continuous duty cycle output response vs. input phase difference for $-\pi < \theta < \pi$
- Constant duty cycle output indicating direction of error for unequal frequency inputs
- High reference frequency rejection
- Improved reference suppression compared with MC12040
- -122 dBc/Hz phase noise @ 1 KHz offset
- High speed, adjustable threshold comparator inputs for low level analog inputs
- AC - coupled or ECL/10G PicoLogic™ input compatibility
- Available in C - leaded or leadless chip carriers or in die form

APPLICATIONS

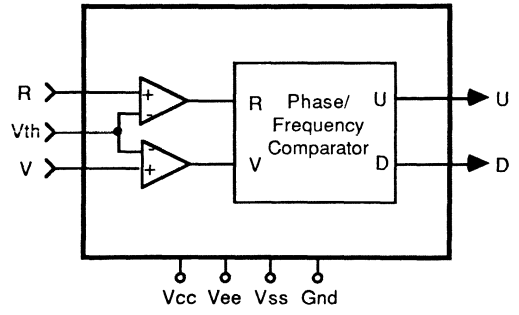
- Stable acquisition phase locked loops
- Frequency synthesizers (with 10G070 Variable Modulus Divider and 10G061 prog. counter)
- Frequency discriminators
- High speed PSK and FSK demodulators
- High resolution time delay measurement

FUNCTIONAL DESCRIPTION

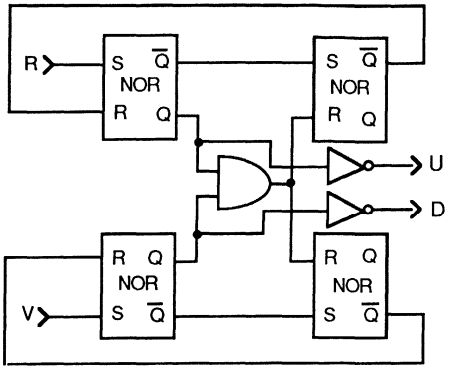
The 16G044 is a rising edge-triggered phase/frequency comparator with sensitive differential amplifier inputs capable of accepting input signals up to 1GHz in frequency. Functionally, it is similar in operation to the MC4044 or 11C44 although much faster and with much greater reference frequency rejection. When the R (Reference) and V (VCO) inputs are unequal in frequency and/or phase, the differential outputs U (Up) and D (Down) are pulse streams which when subtracted and integrated provide an error voltage for control of a VCO. This contrasts with an analog mixer or exclusive - OR based phase detector which does not produce explicit frequency error information. Use of the 16G044 in a PLL makes frequency acquisition more stable by comparison.

The 16G044 is fabricated using GigaBit's high volume, production proven GaAs MESFET process technology.

BLOCK DIAGRAM



EQUIVALENT LOGIC DIAGRAM



16G044 ORDERING INFORMATION

PACKAGE TYPE	SPEED (Min. @ 25°C)	
	1GHz	750 MHz
C-Leaded CC	16G044-2C	16G044-3C
Leadless CC	16G044-2L	16G044-3L
Dice		16G044-3X

16G044 Operation

The operation of the 16G044 is best explained with reference to Figure 1 which plots the average value of U, D, and U - D versus the phase or frequency difference between the R and V inputs.

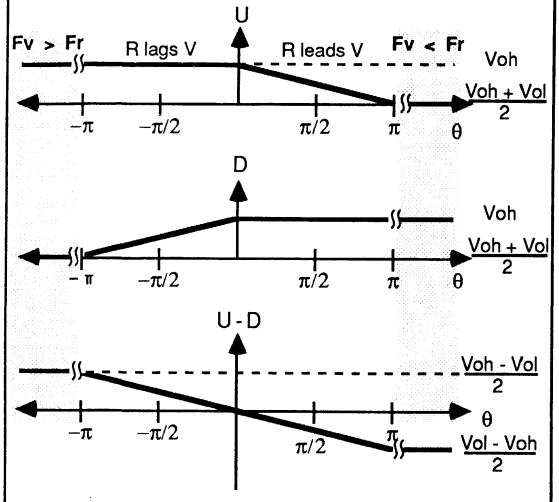


Figure 1: 16G044 Operation

Four relationships between R and V are possible: R lags or leads V in phase and Fr is less than or greater than Fv.

1. R lags V in phase

When the R and V inputs are equal in frequency but R lags V in phase, the U output is pegged high (at VOH) and the D output pulses low with a duty cycle that is proportional to the phase difference between R and V, reaching a minimum of 50% for 180° phase difference. Therefore, the average value of D varies between VOH (0° phase difference) and (VOH + VOL)/2 (180° phase difference). The signal on D indicates that the VCO frequency should be decreased to bring the loop into lock.

2. Fv > Fr

When the V input frequency exceeds that of the R input, the behavior of the 16G044 is the same as described in 1. above except that the D output duty cycle is constant at approximately 50%. The average value of D is constant at (VOH + VOL)/2 as shown in Figure 1. As above, the signal on D indicates that the VCO frequency should be decreased to establish lock.

3. R Leads V in Phase

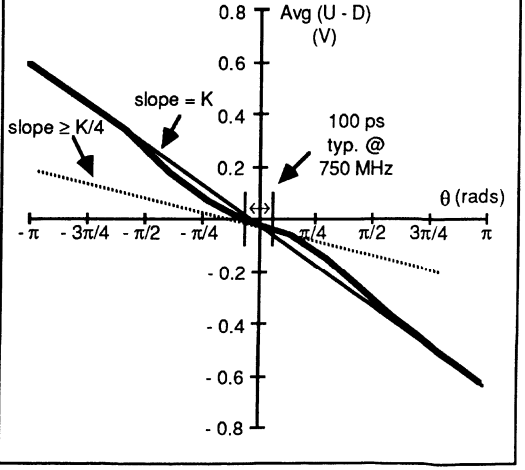
When the R and V inputs are equal in frequency but R leads V in phase, the D output is held high (at VOH) and the U output pulses low with a duty cycle that is proportional to the phase angle between R and V, reaching a minimum of 50% for 180° phase difference. The average value of U varies between VOH (0° phase difference and (VOH + VOL)/2 (180° difference). The signal on U indicates that the VCO frequency should be increased to establish lock.

4. Fv < Fr

When the V input frequency is less than the R input signal frequency, the 16G044 operates as described in 3. above except that the U output duty cycle does not vary, but is constant at approximately 50%. Therefore the average value of U is constant at (VOH + VOL)/2 as shown in Figure 1. Again, the signal on U provides information used to increase the VCO frequency to establish loop lock.

Note that when R and V are equal in frequency and phase, i.e. when the loop is locked, the average value of U - D is zero, meaning that the action of the 16G044 is to maintain the loop in lock status.

Figure 2: 16G044 Transfer Characteristic at 750 MHz (see Fig. 4)



16G044 Operation (continued)

Figure 2 plots the transfer characteristic of the 16G044 with equal frequency R and V inputs at 750 MHz. The slope of the curve drawn as the solid straight line is the comparator gain constant, K, and is typically 600 mV/π radians or 0.19 V/rad. The reduction in K in the vicinity of zero phase difference is of particular interest to PLL system designers. The 16G044 is designed to minimize this decrease in gain to ≥ K/4 and to limit the range of flattening to less than 100ps or 27° (± 13.5°) of phase at 750 MHz.

Figure 3 describes the logical I/O characteristics of the 16G044 which is useful for purposes of testing the device at low speed.

Figure 3: 16G044 State Table

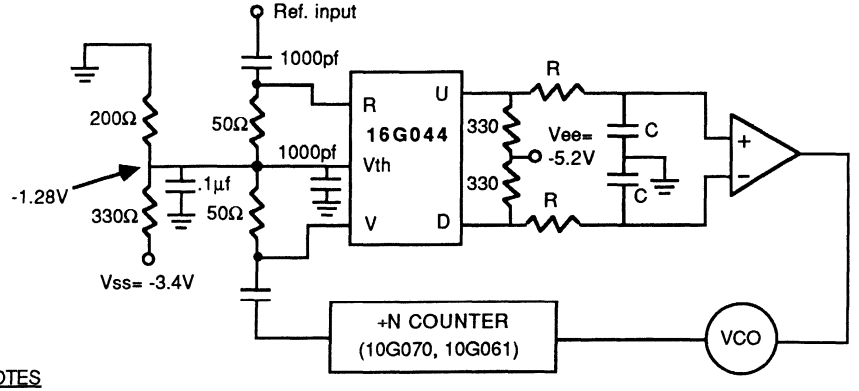
	Inputs		Outputs		Notes
	R	V	U	D	
R leads V	0	0	1	1	A
	↓	0	0	1	
	X	↓	1	1	
R lags V	0	0	1	1	A
	0	↓	1	0	
	↓	X	1	1	

Note A: This table assumes that the 0, 0 input state shown was preceded at some time with a falling edge (1—> 0) transition in both R and V.

PIN DESCRIPTIONS

R	Reference signal input
V	VCO signal input
U	The "Up" (R leads V) output
D	The "Down" (R lags V) output
Vth	Threshold voltage input for the input comparators. Must be in the range - 1.8V ≤ Vth ≤ - 0.8V
VCC	+ 5.0V supply pin
Gnd	Ground connection
VSS	- 3.4V supply pin
VEE	- 5.2V supply pin

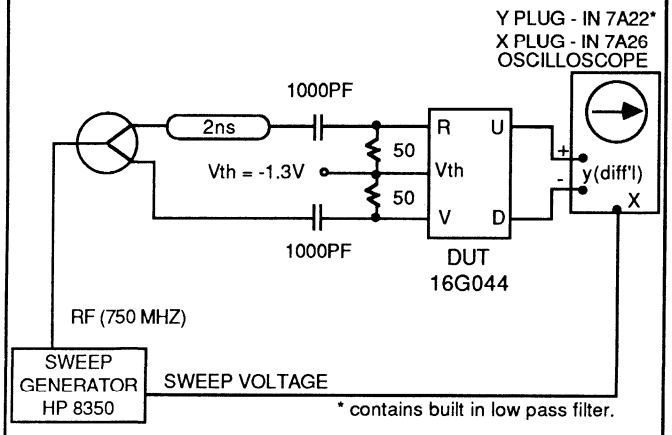
16G044 Application in a Simple Phase Locked Loop



NOTES

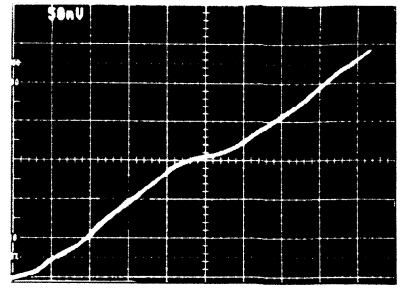
1. The transfer characteristic of the simple loop filter shown is 1/(1 + sT) whereT = RC. Typically R should be chosen to be >1KΩ. The connections to the op-amp assume a negative VCO gain constant. These connections should be reversed if a VCO with a positive transfer characteristic is used.

Figure 4. Test setup for high speed measurement of phase detector transfer characteristic.

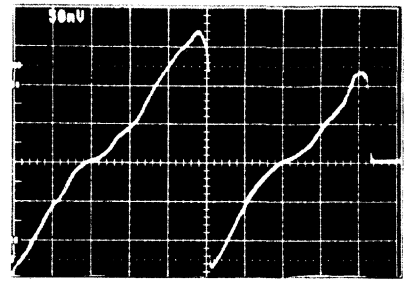


This test setup creates a delay line frequency discriminator which enables accurate linearity measurements of the phase detector. The resulting discriminator has zero output voltage at 500MHz and 1 GHz.

Figure 4 Oscillographs (0 dBm Input)



(Y = 250 mV/div., X = 250 to 750 MHz)



(Y = 250 mV/div., X = 300 to 1300 MHz)

ABSOLUTE MAXIMUM RATINGS

(Beyond which useful life may be impaired) (Notes 1, 4)

SYMBOL	PARAMETER	ABSOLUTE MAXIMUM RATINGS	NOTES
TSTOR	Storage Temperature	- 65 °C to + 150 °C	
TJ	Junction Temperature	- 55 °C to + 150 °C	
TC	Case Temperature Under Bias	- 55 °C to + 125 °C	2
VCC	Supply Voltage	0V to + 7.0V	
VSS	Supply Voltage	- 4.0 V to + 0.5 V	
VEE	Supply Voltage	- 6.0 V to VSS + 0.5 V	
VIN	Voltage Applied to Any Input; Continuous VSS = - 3.4 V, VEE = - 5.2 V	- 4.0 V to + 0.5 V	
IIN	Current Into Any Input; Continuous	- 0.5 mA to 1.0 mA	
VOUT	Voltage Applied to Any Output	-4.0V to +0.5 V	3
IOUT	Current From Any Output; Continuous	-40 mA	
PD	Power Dissipation Per Output POUT = (-VOUT) x IOUT	50 mW	

Notes:
1. All voltages specified relative to Gnd. Positive current is defined as current into the device.
2. TC is measured at case top.
3. Subject to IOUT and PD limitations.
4. Power supply sequencing is not necessary. However, sustained (>5 secs.) application of VSS in the absence of VEE could result in excessive power dissipation and damage to the device.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN	NOM	MAX	UNITS	NOTES
TC	Case Operating Temperature		+25		℃	1
Gnd	Ground connection		0		V	
VCC	Supply Voltage	4.75	5.0	5.25	V	
VSS	Supply Voltage	- 3.5	- 3.4	- 3.3	V	
VEE	Supply Voltage	- 5.5	- 5.2	- 5.1	V	

Notes: 1. TC measured at case top. User attention to device thermal management is recommended. See GigaBit Application Note 3 for a detailed treatment of thermal management considerations.

DC CHARACTERISTICS (1, 2)

TC =25°C, VCC = 4.75V to 5.25V, VSS = - 3.3V to - 3.5V, VEE = - 5.1V to - 5.5V

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	TEST CONDITIONS	NOTES
CMR	Input common mode range	- 1.8		- 0.8	V		
VIH	Input voltage high	- 1.1		Gnd	V		
VIL	Input voltage low	VTT		- 1.5	V		
IIN	Input current			300	µA	Vin = - 1.0V to - 1.6V	
VOH	Output voltage high	- 0.8	- 0.6	-0.3	V	Outputs terminated	
VOL	Output voltage low	- 2.0	- 1.9	- 1.8	V	100Ω to VTT = - 2.0V.	
IOH	Output high current		- 25	-20	mA		3
ICC	VCC supply current		45	57	mA		
ISS	VSS supply current		75	92	mA		
IEE	VEE supply current		95	116	mA		
PD	Power dissipation		1.0	1.2	W		4

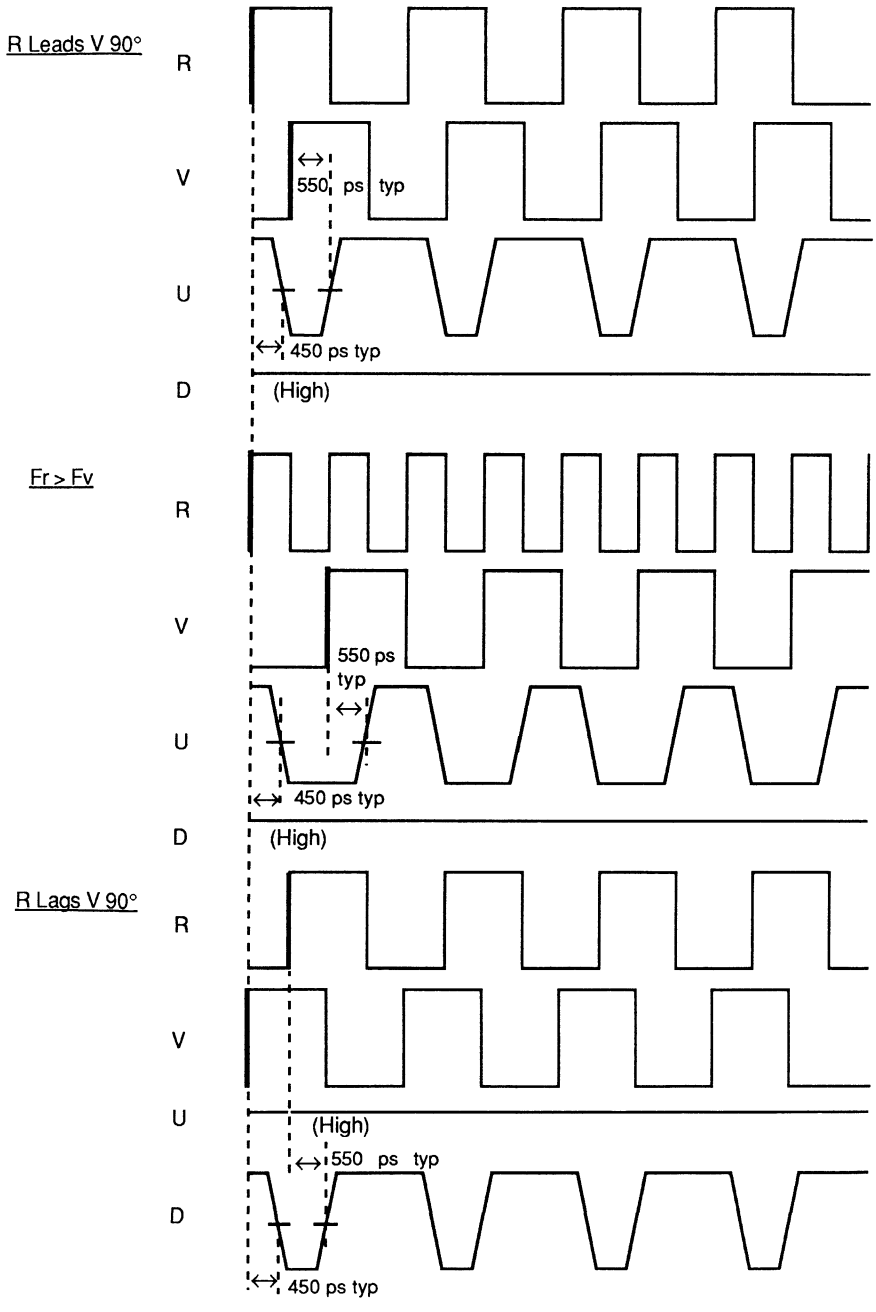
Notes:
1. These characteristics are applicable from DC to ~ 500 MHz.
2. Vth = - 1.3V
3. IOH is the available output current at VOH = - 0.8V.
4. At nominal power supply voltages and 50% output duty cycle.

AC CHARACTERISTICS

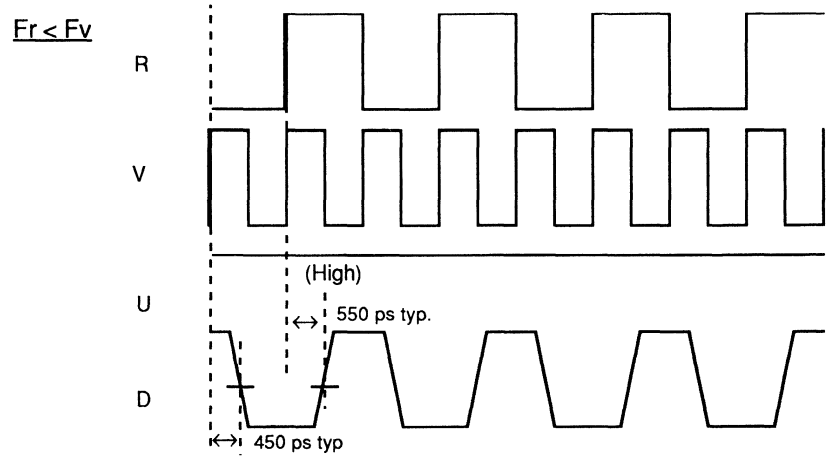
Vth = - 1.3V, VCC = 4.75V to 5.25V, VSS = - 3.3V to - 3.5V, VEE = - 5.1V to - 5.5V, outputs terminated in 100Ω to Vtt = -2.0V

SYMBOL	PARAMETER	TC=0°C		TC = 25°C			TC = 85°C		UNITS	TEST CONDITIONS
		Min	Max	Min	Typ	Max	Min	Max		
VIH	Input voltage high			- 1.0		-0.3			V	
VIL	Input voltage low			VTT		- 1.6			V	
Kd	Large signal gain constant			500/π	600/π				mV/rad	
kd2	Small signal gain constant (16G044 - 2)			125/π	300/π				mV/rad	f = 1GHz
kd3	Small signal gain constant (16G044 - 3)			125/π	300/π				mV/rad	f = 750 MHz

AC WAVEFORMS

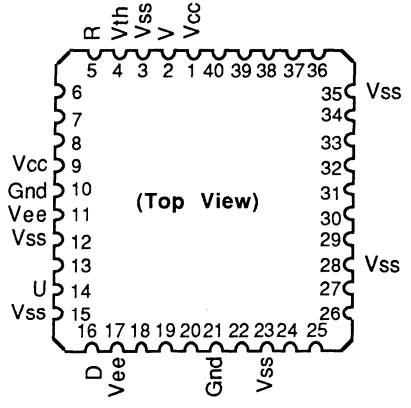


AC WAVEFORMS cont.



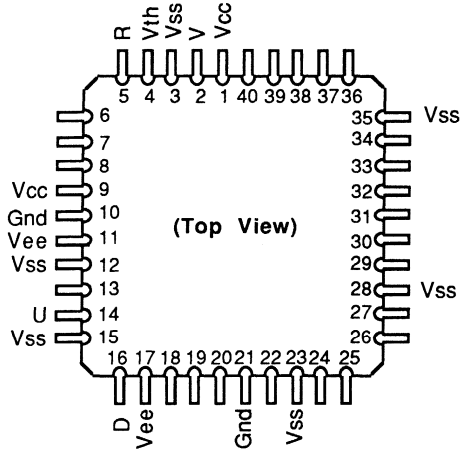
PACKAGE PINOUT DIAGRAMS

PACKAGE TYPE "L"



NOTES: Pin 1 is marked for orientation; all unmarked pins are unused.

PACKAGE TYPE "C"



NOTES: Pin 1 is marked for orientation; all unmarked pins are unused.

Time Delay Generator
2 To 20 ns Programmable Delay/1 ps Resolution

DISTINCTIVE CAPABILITIES

- Voltage-programmable edge delay and pulsewidth
- Single-ended D inputs select true or inverted output
- ECL and 10G PicoLogic compatible I/O
- Temperature and voltage compensated using VBB threshold reference input
- On-chip VBBS (-1.2V) reference voltage supply
- GHz switching rate between programmed timing sets
- Wire-OR output capability
- Available in C- leaded or leadless chip carrier or dice form
- Packages contain internal decoupling capacitors for optimum high frequency performance

APPLICATIONS

- Clock system deskew
- Precision pulse generation
- Time Delay Vernier
- HS timeset formatter

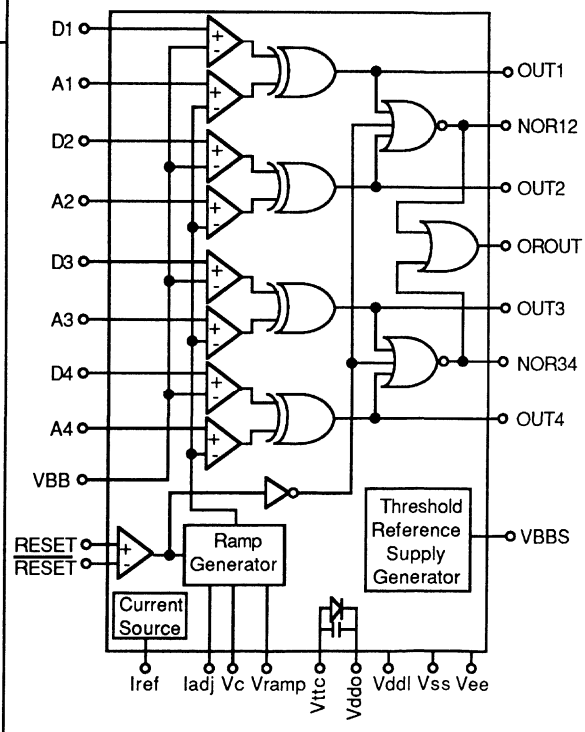
FUNCTIONAL DESCRIPTION

The 16G060 is an ECL or 10G PicoLogic compatible high resolution time delay generator. Because of its sensitive differential amplifier and linear ramp generator circuitry, the 16G060 can produce voltage ramp-based time delays with picosecond resolution over nanosecond ranges. The outputs can be inverted under control of the D (digital) inputs. Outputs OUTn are pulse outputs equal to the Reset input pulse width but with the leading edge delayed by the amount of delay programmed. The two NOR outputs provide pulses with both leading and trailing edge delay programmability. The OR output can provide up to two pulses with independent delay programmability of all leading and trailing edges. The device features a nominal -1.2V GaAs/ECL threshold reference supply voltage output on pin VBBS. Output transition times are typically 150ps.

The 16G060 features a reference level current source output (Iref) which when connected to the ramp generator adjust input (Iadj) configures an 8 to 10 ns total ramp delay. Shorter or longer delays can be programmed by externally setting the current into Iadj using a resistor to ground (Vddl).

The 16G060 is fabricated using GigaBit's high volume, production proven GaAs MESFET process technology.

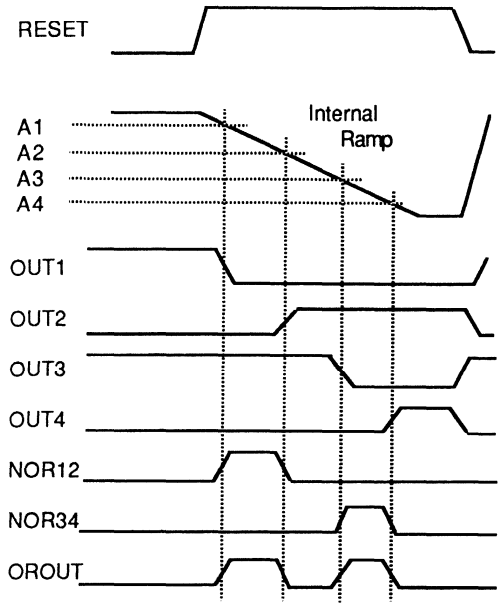
BLOCK DIAGRAM



16G060 ORDERING INFORMATION

Package Type	Part Number
C-Leaded chip carrier	16G060-2C
Leadless chip carrier	16G060-2L
Unpackaged dice	16G060-2X

FUNCTIONAL DESCRIPTION (cont.)



The diagram above shows one possible timing setup for the 16G060. The analog inputs A1 thru A4 are configured with DC voltages such that A1>A2>A3>A4 and the digital inputs D1 thru D4 are set to provide delayed falling edges (D = '1') or rising edges (D = '0'). (In this case D1 = D3 = '1' and D2 = D4 = '0'.) The delayed edge outputs OUT1 thru OUT4 behave as shown. The NOR12 output is a pulse with rising edge determined by A1 and falling edge determined by A2. The NOR34 output is a pulse similarly determined by A3 and A4. The OROUT output is simply the logical OR of NOR12 and NOR34.

By changing the logical states of D1 thru D4 , other combinations of true and inverted edge delay outputs can be generated. The pulse outputs can be made to produce or not produce pulses. This leads to the very useful ability to use the OROUT output or an external wire-OR of OUT1 -4 to produce different pulse or edge delays between firings of the ramp. For a total ramp time setting (using ladj) of 2 ns, the cycle rate of the device would be once every 2.75 ns (0.75 ns required for ramp reset). This means that preset timings could be switched at a 360 MHz rate.

PIN DESCRIPTIONS

D1 to D4	Data inputs
A1 to A4	Analog voltage delay programming inputs
OUT1 - 4	Delayed edge outputs
NOR12	Pulse output controlled by D1,A1,D2,A2
NOR34	Pulse output controlled by D3,A3,D4,A4
OROUT	NOR12 + NOR34
$\overline{\text{RESET}}$, RESET	Differential ramp reset/start control
ladj	Ramp-rate control current input
Iref	Current source output for ramp-rate control
VDDO	Output driver ground (0V)
VDDL	Internal logic ground (0V)
VSS	-3.4V power supply
VEE	-5.2V power supply
Vramp	-7.0V supply to the ramp generator
VTTC	VDDO internal decoupling capacitor return. VTTC is brought into the 16G060 package as the AC return lead for the internal VDDO output driver decoupling capacitor. It is not brought onto the16G060 die. VTTC is typically equal to VTT (nominally -2.0V).
Vc	-2.0V supply to ramp generator and analog input termination voltage.
VBB	Threshold reference level input. Provided to allow direct tracking of the driving logic family's output threshold voltage. Connect to VBBS when the 16G060 is driven from PicoLogic. When driving from ECL or other GaAs families, connect to that family's threshold voltage. This pin may not be left unconnected.
VBBS	PicoLogic threshold reference voltage output. Nominally equal to -1.2V with a 40Ω source impedance. Connect to VBB when interfacing with PicoLogic. ΔVBBS/ΔTemp. = 0.6mV/°C, ΔVBBS/ΔVSS = 200mV/V.

Functional Description (continued)

The detailed operation of the 16G060 is described by the following tables:

For outputs OUT1 thru OUT4,

Dn	OUTn
0	An
1	An

Edges are defined by Input An

For output NOR12 , (assuming A1 > A2),

D1	D2	NOR12
0	0	A1, A2
0	1	(Low)
1	0	
1	1	

Reset High Pulsewidth

Output NOR34 is similar, (assuming A3 > A4),

D3	D4	NOR34
0	0	A3, A4
0	1	(Low)
1	0	
1	1	

Reset High Pulsewidth

For output OROUT, (assuming A1 > A2 > A3 > A4), a variety of output waveforms can be produced, many of which will be the same as one or the other of the NOR outputs. This results from setting one of the NOR outputs to 'Low' with the (0,1) D-input combination so that OROUT is determined by the other NOR output, or from masking one NOR waveform with the

Additional output waveforms are shown below.

D1	D2	D3	D4	OROUT
0	1	x	x	NOR34
x	0	0	0	NOR34
x	x	0	1	NOR12
1	1	1	x	NOR12
0	0	1	0	A1, A2, A3, A4
0	0	1	1	
1	0	1	0	
1	0	1	1	
1	1	0	0	

Reset High Pulsewidth

By setting the analog voltage inputs A1 thru A4 to desired levels and switching the D1 thru D4 inputs between ramp cycles, useful combinations of timing waveforms can be generated at high speed. For example:

D1	D2	D3	D4	OROUT
0	0	0	1	A1, A2=A3, A4
1	0	0	1	
0	1	1	0	
0	1	0	0	

Reset High Pulsewidth

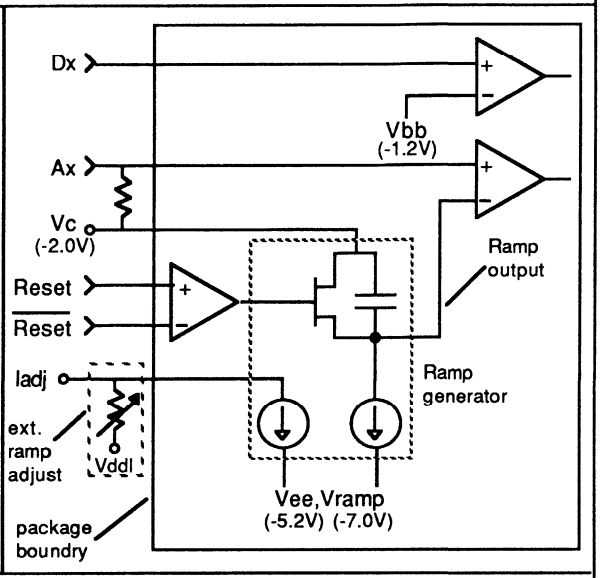
Since D1 thru D4 can be operated at GHz speeds, a sequence of timing changes can be executed at a maximum speed determined by the ramp cycle rate used, rather than by the speed of the DAC's used to provide analog inputs A1 thru A4.

16G060 APPLICATIONS INFORMATION

The diagram to the right shows more detail of the ramp generator circuit. Note that the proper termination point for the analog inputs is the Vc pin in order to minimize the effect of any Vc supply noise on the switching threshold of the ramp voltage comparator.

The total ramp period is adjustable from approximately 2 to 20 ns via application of between 1 and 5 mA into the ladj pin. This current can be provided using a resistor to Vddl (Gnd) in the range of from 3500Ω to 700Ω. The Iref current output of approximately 3 mA provides for a total ramp period of about 4 to 5 ns when Iref is strapped to the ladj input.

It is also possible to operate the 16G060 with Vramp = Vee = -5.2V. In this case, the total ramp delay is reduced to approximately 3 to 4 ns and the ladj input will have no adjustment control.



ABSOLUTE MAXIMUM RATINGS

(Beyond which useful life may be impaired) (Note 1)

SYMBOL	PARAMETER	ABSOLUTE MAXIMUM RATING	NOTES
TSTOR	Storage Temperature	- 65 °C to + 150 °C	
TJ	Junction Temperature	- 55 °C to + 150 °C	
TC	Case Temperature Under Bias	- 55 °C to + 125 °C	2
VDDO	Output Driver Supply Voltage	VSS to + 1.0 V	
VSS	Supply Voltage	- 4.0 V to + 0.5 V	
VEE	Supply Voltage	-7.0 V to VSS + 0.5 V	
VRAMP	Supply Voltage	-7.5 V to VSS + 0.5 V	
VIND	Voltage Applied to Digital Inputs, Continuous (Vss = -3.4V, Vee = -5.2V, Vramp = -7.0V)	- 4.0 V to + 0.5 V	
VINA	Voltage Applied to Analog Inputs, Continuous (Vss = -3.4V, Vee = -5.2V, Vramp = -7.0V)	-5.7 V to -1.5 V	
VADJ	Voltage Applied to Iadj Input	-5.7 V to -1.5 V	
IIN	Current Into Any Input; Continuous	- 0.5 mA to 1.0 mA	
VOUT	Voltage Applied to Any Output	-4.0V to +7.0 V	3
IOUT	Current From Any Output; Continuous	-100 mA	
PD	Power Dissipation Per Output POUT = (VDDO-VOUT) x IOUT	100 mW	
VBB	Threshold Reference Input Voltage	-4.0V to +0.5V	
IBB	Input current (from interfacing family)	-0.5mA to +1.0mA	
VTTC	VDDO Internal Decoupling Cap. Return	-6.0 V to VDDO	
VTT	Load Termination Supply	-6.0 V to VDDO + 6.0 V	

Notes:

1. All voltages specified with VDDL defined as ground. Positive curent is defined as current into the device. Power supply sequencing is not necessary, but since the VEE supply is used to bias off the normally-on depletion mode FETs, sustained (>5 secs.) application of VSS in the absence of VEE may result in excessive power dissipation and damage to the device.
2. TC is measured at case top. 3. Subject to IOUT and PD limitations.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN	NOM	MAX	UNITS	NOTES
TC	Case OperatingTemperature		25		℃	
VDDL	Logic Supply Voltage		Gnd		V	1
VDDO	Output Driver Supply Voltage	-0.8	Gnd	1.0	V	
VC	Ramp Supply Voltage	-2.2	-2.0	-1.8	V	
VSS	Supply Voltage	- 3.5	- 3.4	- 3.3	V	
VEE	Supply Voltage	- 5.5	- 5.2	- 5.1	V	
VRAMP	Ramp Supply Voltage	- 7.5	- 7.0	- 6.5	V	
VTTC	VDDO Internal Decoupling Return	VSS	VTT	VDDO	V	2
VTT	Load Termination Supply Voltage	VSS	- 2.0	- 2.0	V	2
RLOAD	Output Termination Load Resistance	25	50	100	Ω	

Notes: 1. Tcase measured at case top. User attention to appropriate device thermal management is recommeded. See GigaBit Application Note 3, "Thermal Management of PicoLogic and NanoRam GaAs Digital IC Families" for a complete discussion of device thermal management. Heatsinks are available from GigaBit. See page 8, notes 6 and 7.

2. The RLOAD and VTT combination used is subject to maximum output current and power restrictions.

DC CHARACTERISTICS (Notes 1,2)

VSS = -3.5V to -3.3V, VEE =-5.2V, Vramp = -7.0V, Vc = -2.0V, VDDL=VDDO = 0V, unless otherwise indicated.

Symbol	Parameter	16G060			Units	Test Conditions	Notes
		Minimum	Typical	Maximum			
VOH	Output Voltage High	- 0.8	-0.4	-0.3	V		
VOL	Output Voltage Low	- 2.0	-1.9	- 1.8	V		
IOH	Output Current High		-70	-60	mA	VOH = -0.8V	3
VIH	Input Voltage High	- 1.0		VDDL	V		6
VIL	Input Voltage Low	VSS		- 1.6	V		6
IIN	Input Current	-500		500	uA	VIN = -1.0V to -1.6V	6
VAin	A1 -A 4 Input Voltage	- 4.0		- 2.4	V		
Iref	Ref. Current Output		2.0		mA		
VBBS	Thresh. Ref. Voltage		-1.2		V		4
Iadj	Ramp Rate Control	1.0	2.0	5.0	mA		
Ic	Vc Supply Current		20		mA		
Iramp	Vramp Supply Current		20		mA		
ISS	Power Supply Current		200		mA		
IEE	Power Supply Current		50		mA		
PD	Power Dissipation		1000		mW		5

Notes:

1. These characteristics are applicable from DC to 500 MHz.
2. Test conditions unless otherwise indicated: VBB = -1.3V, VTT = -2.0V, VTTC = VTT, Rload = 50Ω to -2.0V.
3. IOH is the available source follower output current at VOH = -0.8V.
4. Nominally equal to -1.2V with a 40Ω source impedance. The range of VBBS at 25°C is -1.05V to -1.3V. ΔVBBS/ΔTemp. = +0.6mV/°C; ΔVBBS/ΔVSS = +0.2mV/mV.
5. Measured at nominal supply voltages and 50% output duty cycle. Excludes VDDO output source follower power (typically 15 mW per loaded output) .
6. Digital inputs only (Reset, Reset, D1, D2, D3, D4).

AC CHARACTERISTICS (Note 1)

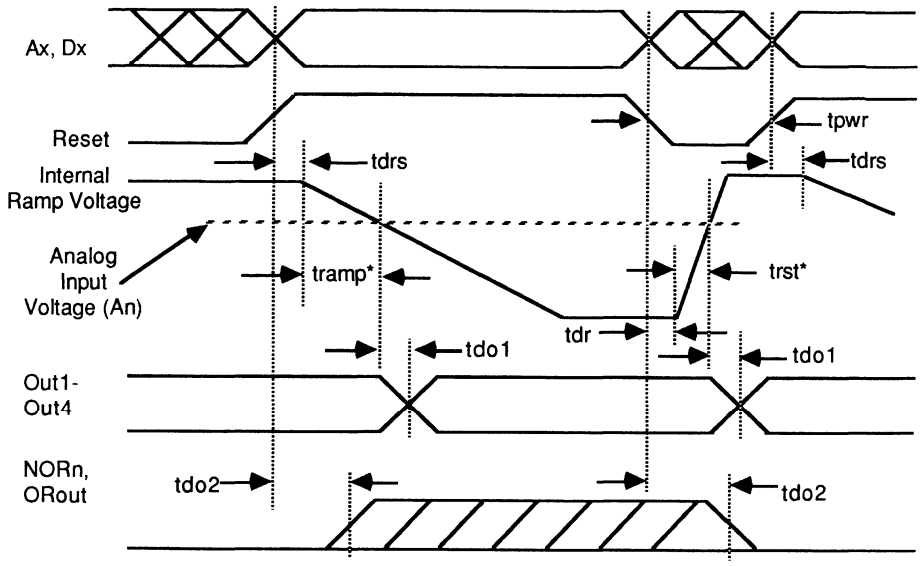
VSS = -3.5V to -3.3V, VEE =-5.2V, Vramp = -7.0V, Vc = -2.0V, VDDL=VDDO = 0V, unless otherwise indicated.

SYMBOL	PARAMETER		Tc = +25°C				UNITS	NOTES
			MIN	TYP	MAX			
tr, tf	Output rise/fall times			125	175		ps	2
tpwr	Reset pulse width		750	600			ps	
tdr	Reset delay			150			ps	
tdrs	Ramp start delay			150			ps	3
tdo1	Output delay (OUTn)		400	500	600		ps	
tdo2	Output delay (OR/NOR)		400	450	550		ps	
Linearity	Analog voltage to delay time linearity			1.0			%	
Δe	Edge placement accuracy			Tbd			ps	

NOTES:

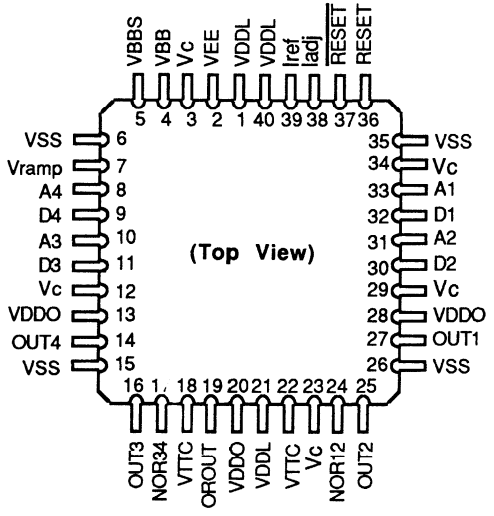
1. Test conditions unless otherwise indicated: VBB = -1.2V, VTT = -2.0V, VTTC = VTT, RLOAD = 50Ω to VTT, VIH = -0.7V, VIL = -1.7V, VOH ≥ -0.7V, VOL ≤ -1.7V, VAin = -2.7V to -3.7V. Input signal rise and fall times ≤ 200 ps.
2. Rise and fall times are measured at the 20% and 80% points of the transition from Vol max to Voh min.
3. Measured with A input at -2.4V.

SWITCHING WAVEFORMS



* tramp and trst are delays determined by the ramp rate and analog input voltage set by the user.

PIN FUNCTION DRAWING - PACKAGE TYPES "L" AND "C"



NOTES: Pin 1 is marked for orientation.

GigaBit Logic

16G061
ADVANCE

Dual High Speed Pin Driver
1.5 GHz Operating Frequency

FEATURES

- DC to 1.5 GHz operation
- 600 ps propagation delay (ECL/GaAs)
- 150 ps output rise and fall times (ECL/GaAs)
- 200 ps output rise and fall times for up to 5Vp-p
- Selectable slow output edge rates for TTL/CMOS: 2ns rise and fall time at 5Volts peak to peak
- Programmable output voltages up to 5Vp-p over -2V to +5V range
- High impedance, three state output capability
- 100 mA output current drive capability
- High speed differential inputs, GaAs and ECL level compatible
- On chip VBBS (-1.2V) reference voltage
- Available in C-leaded or leadless chip carriers or in die form
- Packages contain internal decoupling capacitors for optimum high frequency performance

APPLICATIONS

- ATE pin driver
- Switch Driver
- CRT preamplifier
- Laser driver
- Level comparator
- General purpose driver
- Differential Line Receiver
- Precision Pulse Generator

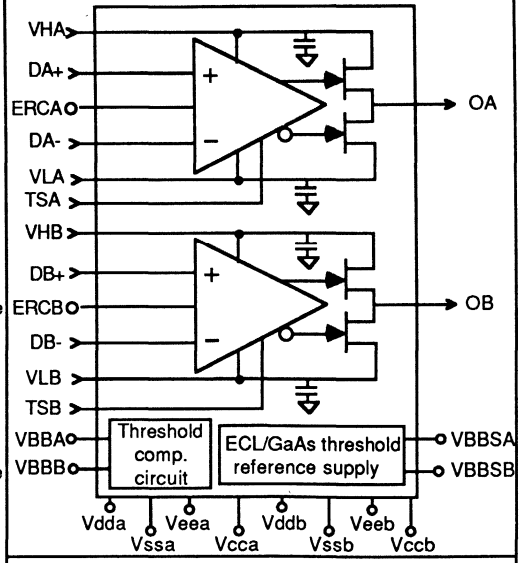
FUNCTIONAL DESCRIPTION

The 16G061 is a dual pin driver designed for use in very high speed GaAs/ECL as well as TTL/CMOS logic test systems. Each of the 16G061 driver is electrically independent and has separate power supplies. Under control of the differential inputs, the output is switched between the levels provided on the VH (V High) and VL (V Low) inputs. The differential inputs can be driven with ECL or GaAs levels. The 16G061 has an on-chip threshold voltage generator (VBBS). When VBBS is connected to the D- inputs, the D+ inputs of the 16G061 can be driven single-ended. The VHigh output level is adjustable from -1.1V to +5.0V and the VLow output level can be adjusted from -2.0V to +1.5V. The output amplitude extends to 5Vp-p. Controls are provided (TSA, TSB) to force the outputs into a high impedance, three state condition. An external series output resistor of typically 42Ω is recommended so that, in combination with the output MESFET on resistance (about 8Ω), the output impedance is 50Ω. External unity gain amplifiers such as the LM324 or higher current operational amplifiers such as the LM759 can be used to buffer the VHigh (VH) and VLow (VL) inputs when driven from DACs.

The 16G061 features an output Edge Rate Control (ERCA and ERCB) to vary the output rise and fall times. Rise and fall times are typically 150 ps for a 1V peak to peak output (GaAs/ECL) and 200 ps for a 5V peak to peak output when Edge Rate Control (ERC) is biased at VCC. This translates to a slew rate of 6.5V/ns for a 1V output and 25V/ns for a 5V output. Rise and fall times can be increased to 2ns for a 5V peak to peak output by connecting ERC to VEE. This translates to a slew rate of 2.5V/ns for a 5V output. System timing requirements are achieved through a specified 500ps driver propagation delay for ECL/GaAs levels, 600 ps delay for fast edge rate TTL/CMOS levels and 1.5 ns delay for slow edge rate TTL/CMOS levels.

The 16G061 is fabricated using GigaBit's high volume GaAs MESFET processing technology.

BLOCK DIAGRAM



Package Type	Speed (Min. 25°C) 1.5 GHz
C-leaded CC	16G061-2C
Leadless CC	16G061-2L
Die	16G061-2X

ABSOLUTE MAXIMUM RATINGS

(Beyond which useful life may be impaired) (Notes 1, 4)

SYMBOL	PARAMETER	ABSOLUTE MAXIMUM RATINGS	NOTES
TSTOR	Storage Temperature	- 65 °C to + 150 °C	
TJ	Junction Temperature	- 55 °C to + 150 °C	
TC	Case Temperature Under Bias	- 55 °C to + 125 °C	2
VDD	Output Driver Gnd Supply	VSS to + 1.0 V	
VSS	Supply Voltage	- 4.0 V to + 0.5 V	
VEE	Supply Voltage	- 7.0 V to VSS + 0.5 V	
VCC	Supply Voltage	+0.5 V to +10.0V	
VIN	Voltage Applied to Any Input; Continuous VSS = - 3.4 V, VEE = - 5.2 V	- 4.0 V to + 0.5 V	
IIN	Current Into Any Input; Continuous	- 0.5 mA to 1.0 mA	3
VOUT	Voltage Applied to Any Output	VL to VL+7.0 V	5
IOUT	Current From Any Output; Continuous	-100 mA	
PD	Power Dissipation Per Output POUT = (VDDO-VOUT) x IOUT	100 mW	
VBB	Threshold Reference Input Voltage	-4.0V to +0.5V	
IBB	Input current (from interfacing family)	-0.5 mA to +1.0 mA	
VTTC	VDD Internal Decoupling Cap. Return	-6.0 V to VDD	
VTT	Load Termination Supply	-6.0 V to VDD + 6.0 V	

Notes:

1. All voltages specified with VDD defined as Gnd. Positive current is defined as current into the device.
2. TC is measured at case top.
3. Subject to IOUT and power dissipation limitations.
4. Power supply sequencing is not necessary, but since the VEE supply is used to bias off the normally-on depletion mode transistors, sustained (>5 secs.) application of VSS in the absence of VEE may result in excessive power dissipation and damage to the device.
5. Voltage applied through a 42Ω series resistor.

RECOMMENDED OPERATING CONDITIONS (Note 3)

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
TC	Case Operating Temperature	0	25	85	°C	1
VDD	Supply Voltage		Gnd		V	
VCC	Supply Voltage	+3	VH + 2	7.5	V	
VSS	Supply Voltage	-3.5	-3.4	-3.3	V	
VEE	Supply Voltage	-5.5	-5.2	-5.1	V	
VH	High level set voltage	-1.1		5	V	
VL	Low level set voltage	-2.0		+1.5V	V	
VH - VL	Output voltage amplitude	0		5	V	2

Notes:

1. Tcase measured at case top. **User attention to device thermal management is recommended.** See GigaBit Application Note 3, "Thermal Management of PicoLogic and NanoRam GaAs Digital IC Families" for a complete discussion of all aspects of device thermal management. Heatsinks are available from GigaBit.
2. For series terminations. For shunt termination: $Voh = VH \times \left(\frac{Rt}{Rt+Ron}\right)$; $Vol = VL \times \left(\frac{Rt}{Rt+Ron}\right)$; Rt: termination resistance.
3. Max. safe voltage applied to any output through a 42Ω series resistor is limited to VL to VL + 7.0V.

DC CHARACTERISTICS (DC to 500 MHz - Note 1)

Tc = 0°C to 85°C, Vss = -3.5V to -3.3V, Vee = -5.5V to -5.1V, Vcc = 2.0V (ECL) or 7.0V (TTL), Vdd = Gnd

Symbol	Parameter	Min	Typ	Max	Units	Test Conditions	Notes
Vih	Input voltage high	- 1.0		Vdd	V		
Vil	Input voltage low	Vss		- 1.6	V		
Vcm	Common mode Vin	-1.9	VBB	- 0.5	V		
Iin	Input current	- 100		100	µA	Vin = - 0.5V to - 1.9V	
Vbbs	Threshold Ref. voltage (ECL/GaAs)		- 1.2		V		3
Voh	Output voltage high	VH - .02	VH	VH	V	No DC load	
Vol	Output voltage low	VL	VL	VL + .02	V	No DC load	
Ioh	Output drive current	100			mA		2
Ron	Driver FET on rest.	7	8.5	10	Ω	At Voh, Vol	
Voffset	Input Offset Voltage		50		mV		
ICC	Supply Current		120		mA		
IEE	Supply Current		140		mA		
ISS	Supply Current		65		mA		
PdE	Power Dissipation		1.2		W	VCC = 2.0V (ECL)	4
PdT	Power Dissipation		1.8		W	VCC = 7.0V (TTL)	4
Izl	Three state output leakage		20		µA	@40°C	
Izls	Three state output leakage		40		µA	@40°C ; ERC = VEE	

Notes:
1. Test conditions unless otherwise indicated: -D input = -1.30V.
2. Test Conditions: VH - Vout ≥ 1V; VL - Vout ≤ - 1.0V.
3. Source impedance = 40Ω nominally. ΔVBBS/ΔTemp. = +0.6mV/°C; ΔVBBS/ΔVSS = +0.2mV/mV.
4. Measured at nominal supply voltages, 50% output duty cycle and both drivers powered.

AC CHARACTERISTICS (Note 1, 2)

Tc = 0°C to 85°C, Vss = -3.5V to -3.3V, Vee = -5.5V to -5.1V, Vcc = 2.0V (ECL) or 7.0V (TTL), Vdd = Gnd

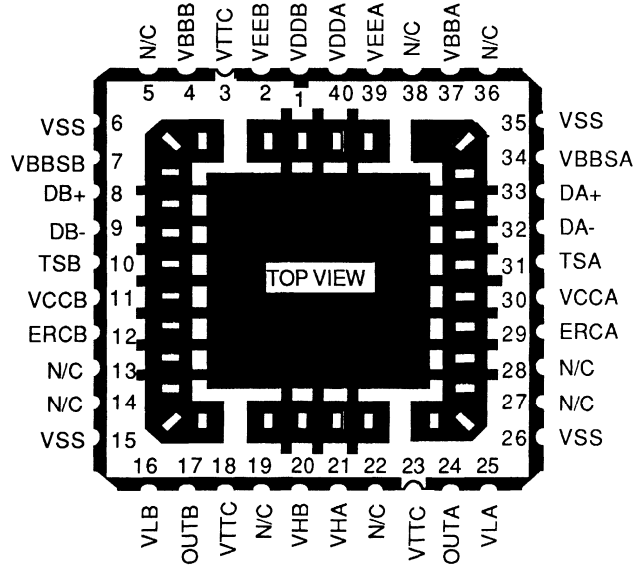
		ECL/GaAs Output Levels			TTL Output Levels					
Symbol	Parameter	Min	Typ	Max	Min	Typ	Max	Units	Test Cond.	Notes
F	Operating frequency	1000	1500		300	500		MHz		
td	Propagation delay		600			700		ps	ERC = VCC	
tds	Prop. delay, slow edge rates		1500			1500		ps	ERC = VEE	
td3	3-state delay		750			850		ps	ERC = VCC	
td3s	3-state delay, slow edge rates		1500			1500		ps	ERC = VEE	
Δtdm	Prop. Delay match; H-L, L-H		50	100		50	100	ps	ERC = VCC	
Δtdms	ΔProp.Delay match,slow mode		300			300		ps	ERC = VEE	
Δtd/Δdc	Δ Prop. delay with duty cycle			100			100	ps	ERC =VCC	
Δtd/ΔT	Prop. delay temp. coeff.		± 1.0			± 1.0		ps/°C	or VEE	
T	Output slew rate		7			25		V/ns	ERC = VCC	3
Tr,f	Output rise and fall times		150			200		ps	ERC = VCC	
Ts	Slow Output slew rate		0.7			2.5		V/ns	ERC = VEE	3
Tsr,sf	Slow Output rise and fall times		1500			2000		ps	ERC = VEE	
Tset	Settling time to 0.05 (Voh - Vol)		0.2	1.0		0.2	1.0	ns		
W	Output crosstalk		.05(Voh-Vol)			.05(Voh-Vol)		V	@ 100MHz	

Notes:
1. VBB = -1.20V, Vih = -1.0V, Vil = -1.6V.
2. ECL Vp-p output = 1.0V; TTL Vp-p output = 5.0V.
3. Output rise and fall times are measured at 10% and 90% points.

PIN DESCRIPTIONS

DA+, DA-	Differential data inputs A.
DB+, DB-	Differential data inputs B.
OA, OB	Output A, Output B.
VLA, VLB	Output Low level set voltages.
VHA, VHB	Output High level set voltages.
TSA, TSB	Three-State output controls. Output, OA or OB, is forced into a high impendance condition when TSA or TSB respectively is high.
ERCA, ERCB	Edge Rate Controls. Edge rates are slowed down when ERC is tied to VEE. Fast edge rates are obtained when ERC is tied to VCC.
VDDA, VDDB	Ground Pins (0V).
VSSA, VSSB	- 3.4V power supplies.
VEEA, VEEB	- 5.2V power supplies.
VCCA, VCCB	Positive power supplies. Nominally VH + 2V.
VTTCA, VTTCB	AC return pin for package internal decoupling capacitor tied to VH (VHigh) and VL (VLow) pins. VTTC is not brought onto the 16G061 substrate, and is typically tied to D.U.T. ground.
VBBA, VBBB	Reference input to the 10G061's input threshold compensation circuit. Connect the VBB supplied from ECL when driving from ECL. Otherwise connect to corresponding VBBS pin.
VBBSA, VBBSB	Picologic Threshold reference output voltage. Connect to VBB when driving form PicoLogic Δ VBBS/Δ Temp = 0.6mV/°C, Δ VBBS/ΔVSS = 0.2 mV/mV.

Pin Function Drawing
Package Types "L" and "C"



90G PROTOTYPING AND SUPPORT PRODUCTS

TABLE OF CONTENTS

GigaBit Logic

90GKIT-40

90GUPB 90G101
90GPPS 90G102

High Speed Prototyping Kit

DISTINCTIVE CAPABILITIES

- Complete kit for prototyping and testing GigaBit's PicoLogic™, NanoRam™, and NanoRom™ GaAs ICs
- 90GUPB printed circuit board contains 8 sites for GigaBit's 36 or 40 pin packages and 8 sites for .300" or .400" DIP ICs.
- Supports signals with 100 ps rise and fall times and up to 3 GHz clock rates
- Low cost, quick turnaround solution to initial device performance testing and evalutation needs
- 90GPPS mating power supply board provides for all necessary voltages and can support a fully populated board
- Kit components available separately for expanded applications.

FUNCTIONAL DESCRIPTION

The 90GKIT-40 prototyping kit provides an easy, quick, an inexpensive way to build and test circuits with up to eight GigaBit Logic GaAs 36 or 40 pin surface mount ICs and up to eight 300 or 400 mil wide DIP ICs. The kit features a printed circuit board (90GUPB) with 4 power planes and a power supply board (90GPPS) capable of supporting the fully populated prototyping board. The 90GKIT-40 kit consists of the following components:

- One **90GUPB** 16-site printed circuit board with 8 sites for surface mounting of GigaBit's 36 or 40 pin components and 8 sites for .300" or .400" wide DIP ICs, up to 24 pins;
- Two **90G101**s, containing five each 90°, PCB-mount SMA connectors for input and output signal connections;
- One **90G102** components package, containing twenty 50Ω chip resistors, twenty 1000pF chip capacitors, and 2.5 feet of .034" semi-rigid 50Ω coaxial cable;
- One **90GPPS** mating power supply card to the 90GUPB printed circuit board with connector and standoffs. The 90GPPS provides a simple power interface to PicoLogic™, ECL, TTL, and CMOS, generating six regulated voltages from a single laboratory supply.
- One **90GSKT-40L**, containing 5 surface mount sockets for the type "L" package only;
- Five type **"90GHS40B"** heatsinks.

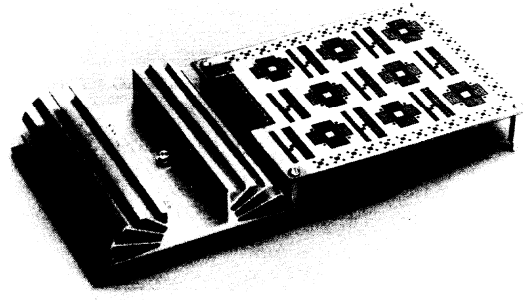


Figure 1: 90GKIT-40

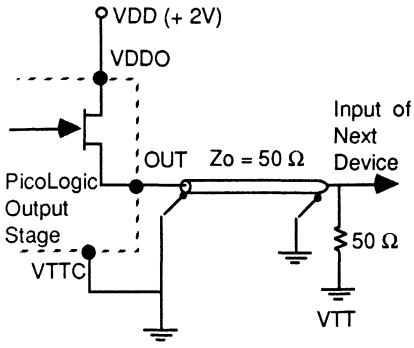
ORDERING INFORMATION

COMPLETE PROTOTYPING KIT

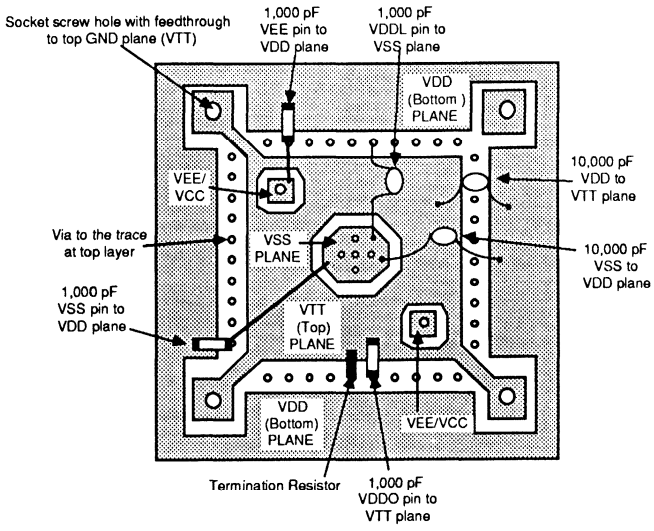
Part No.	Description
90GKIT-40	Contains: 1 - 90GUPB 1- 90GPPS 1- 90G102 2- 90G101 1- 90GSKT-40L (Pkg. of 5 sockets) 5- heatsinks (type "90GHS40B")

KIT ACCESSORIES

Part No.	Description
90GUPB	16-site PCB; 8 for GigaBit's 36 and 40 I/O pkgs, 8 for .300" and .400" DIP pkgs.
90GPPS	Power Supply Board
90G101	Pkg. of 5 90° PCB mount SMAs
90G102	20 - 50Ω chip resistors; 20 -1,000pF chip capacitors, 2.5 ft of 0.034" semi-rigid coax. cable
90GSKT-40L	Pkg. of 5 high-speed sockets for 40 I/O type "L" pkg.
90GHS40B	Pkg. of 10 heatsinks

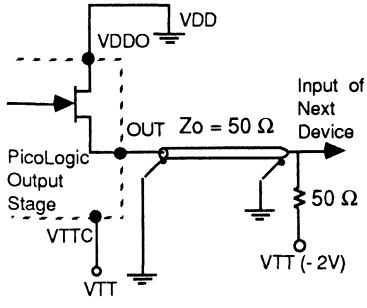


a. Output circuit configuration when VTT = GND

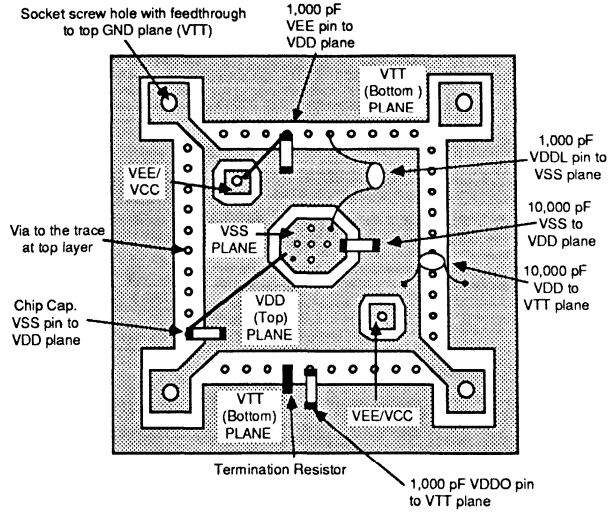


b. Bottom view of the GaAs IC site with examples of capacitor, resistor, and biasing wire connection

Figure 2. Circuit configuration when VTT = GND and VDD = +2V

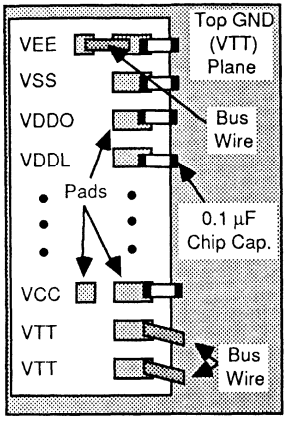


a. Output circuit configuration when VDD = GND

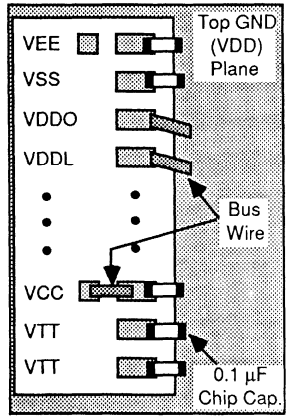


b. Bottom view of the GaAs IC site

Figure 3. Circuit configuration when VDD = GND and VTT = - 2V



a. Input DC power connection configuration for VDD = +2V (Bottom plane) and VTT = GND (Top plane) at the top of the 90GUPB. Bus VDDO and VDDL to the bottom plane at the bottom of the 90GUPB. VEE on layer 3.



b. Input DC power connection configuration for VDD = GND (Top plane) and VTT = -2V (Bottom plane) at the top of the 90GUPB. Bus VTTs to the bottom plane at the bottom of the 90GUPB. VCC on layer 3.

Figure 4. Power supply connections at top of 90GUPB

90GUPB BOARD

The 90GUPB is a 5" X 6", 4-layer glass epoxy PCB with each layer dedicated to a DC voltage source:

Layer 1 (TOP):	VDD or VTT (selectable)
Layer 2:	VEE or VCC (selectable)
Layer 3:	VSS
Layer 4:	VDD or VTT (selectable and opposite of layer 1)

Internal layers 2 and 3 are accessible on the board bottom in specific areas. The 90GUPB's footprints can accept either the GigaBit 36 or 40 I/O package, leadless or leaded. Figure 1 shows the top view of the 90GUPB.

PicoLogic™ ICs are soldered or socketed (using the 90GSKT-40L socket for the type "L" package only) onto the 90GUPB top layer footprints with signals interconnected using supplied 0.034" coaxial cable which is soldered between devices at the footprint traces. The eight footprints for soldering .300" or .400" wide DIP ICs support up to 24 leads for use with a variety of TTL, CMOS, and 10K or 100K ECL ICs.

The depletion mode PicoLogic™ family of GaAs ICs operates with two DC power supplies: VEE = -5.2V and VSS = -3.4V (VDD=GND). E-D (Enhancement Depletion) devices have been designed to utilitze VEE = - 5.2 V and VSS = - 2.0 V as the primary supplies. VTT= -2 V is used for output termination and certain 12G and 16G family devices need VCC= +5 V. Therefore, different power planes are provided in the 90GUPB board. These power planes can be reached through certain areas of the top or bottom side of the board within close proximity to the IC sites. PicoLogic™, NanoRam™ and NanoRom™ devices that are installed on the 90GUPB can be easily used in two different system ground configurations as is shown in Figures 2a and 3a. In both of these schemes it is necessary to maintain the top plane (whether VDD or VTT) at Ground (GND) potential since the shield of the coaxial cable and the outer shell of the SMA connector are electrically connected at the board end to this top plane, and at the other end to the grounded case of interfacing test equipment or to the ground of another subsystem. This also facilitates probing of the signal traces from the top of the board which requires proper grounding of the probe shield very close to the signal point.

SYSTEM GROUND CONFIGURATIONS:

VTT = GND

This configuration (refer to Figure 2 and 4a) is normally used in test environments where the output is driving an oscilloscope with 50Ω input impedance to GND. In this configuration, pins 12 and 13 (VTT) are assigned to the top plane of the 90GUPB board by using bus wire between the two VTT board inputs and the top plane as shown in Fig 2 and 4a. Pins 3 and 4 (VDDO and VDDL respectively) are assigned to the bottom plane by bussing the VDDO and VDDL input pads on the board bottom to the bottom plane of the 90GUPB. VTT is now system ground since the outer shell of the SMA connector is connected to the top of the 90GUPB (VTT) and to the ground of the scope via the shield of the coaxial cable. With VTT = GND, then VDD = +2.0 V, VEE = -3.2 V, VSS = -1.4 V.

VDD = GND

The second configuration (Figure 3 and 4b), which is used when ECL levels must be maintained, shows PicoLogic™ devices used in an all-negative ECL voltage environment. Pins 3 and 4 (VDDO and VDDL respectively) of the

90GUPB board are connected to the top plane by using bus wires as shown in Fig 4b and pins 12 and 13 (VTT) are connected to the bottom plane by bussing the VTT pads on the board bottom to the surrounding plane. With VDD = GND, VTT = -2.0 V, VSS = -5.2 V, and VEE = -3.4 V.

USING A DC GROUND BLOCK

Another method of interconnecting the 90GUPB board to a system with a different ground reference is by using a DC ground block. A DC ground block (see Fig. 5) is a board that divides one side into two conducting planes separated by a small gap. The planes are AC coupled by an array of chip capacitors and the shell of the SMA connectors are soldered to them. In this manner, through the shell of the SMAs, one plane will be AC-coupled to the system reference of the 90GUPB board and the other end to the different system reference of the next sub-system or test equipment. On the opposite side of the board, 50Ω microstrip or coax lines are used to connect the center conductors of the SMAs. A simple DC ground block can be easily built as shown in Figure 5.

Figures 2b and 3b show detailed pictures of one footprint with bypass chip capacitors and line termination chip resistors mounted on the bottom layer of the 90GUPB. The DC power leads of the IC's may easily be bypassed to the VTT or VDD plane with chip capacitors at the bottom of the board. The perimeter area external to each site represents the VTT or VDD plane (whichever is user-programmed to be ground) as explained above.

Layers 2 and 3 of the 90GUPB are dedicated respectively to the VEE (or VCC) and VSS power supply voltages. The VEE and VCC power entry points on the top of the PCB (pads on the left edge of the board) can be wire soldered as shown in Figure 6a or 6b to connect layer 2 to VEE (-5.2V) or VCC (+5V). The freedom to select what DC supply layer 2 represents is very useful, especially in some applications where analog GaAs, NanoRam™, or TTL/CMOS devices are used. In these applications, if the current requirement for VCC far exceeds the requirements for VEE, or the need for a low impedance DC source is much greater for VCC than VEE, then plane 2 is connected to VCC rather than VEE. The VEE/VCC power plane is accessible through the bottom of the PCB inside the IC footprints at two corners of each site. VSS is accessible on the bottom layer of the board inside the small center area of each chip site. The supply voltages can be connected to the IC inputs at the bottom of PCB by soldering short wires to the footprint vias. It should be noted that since plane 3 is the VSS supply and provides the return path for the microstrip on the board, it is essential to provide good capacitive coupling between the top plane (VDD or VTT) and the VSS plane. This may best be accomplished by decoupling all VSS pins to the VTT plane in Fig. 2 or to the VDD plane in Fig. 3. As is shown in Figures 2b and 3b, the VSS plane at the bottom center of the IC site is bypassed with a capacitor to the plane just surrounding it which is always connected to the top plane. This will aid in maintaining the 50Ω characteristic impedance of the footprint traces at the top of the board. Two feedthrough holes, which are connected to the 2nd layer, are located next to pins 8 and 18 (14) of the 24 (20) pin DIP IC sites so that in case ECL devices are installed in these sites, their VEE pins can easily be connected to the VEE plane through these points, or, TTL devices may derive their power from the VCC plane.

It is essential to plan the circuit and the lengths and routing of the coaxial cables, assuming minimum cable bending diameter of 0.25", before attempting to build the circuit. Figure 7 shows an example of the top view of a GaAs IC footprint. Note the different manner in which the 36 and 40 - lead packages will register on the footprint. The figure shows a coaxial cable connection to one of the traces as an example. Plated-through holes are provided at each trace so that all IC leads are also accessible at the bottom of the board. If all IC sites are not used, the designer is advised to disperse the IC's on the board liberally to help with coax routing, unless propagation delay is an issue. Caution must be exercised when passing the coax through either the DIP or chip carrier sites to avoid shorting the power plane access points to the metal shield of the coax.

The IC's can be easily soldered to the top footprint traces, or the user can socket PicoLogic GaAs IC's using a high speed socket for the type "L" leadless package only (P/N

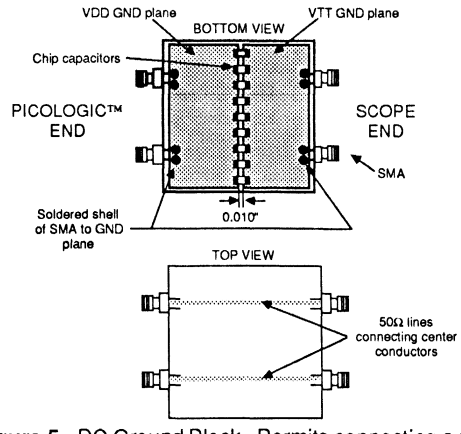
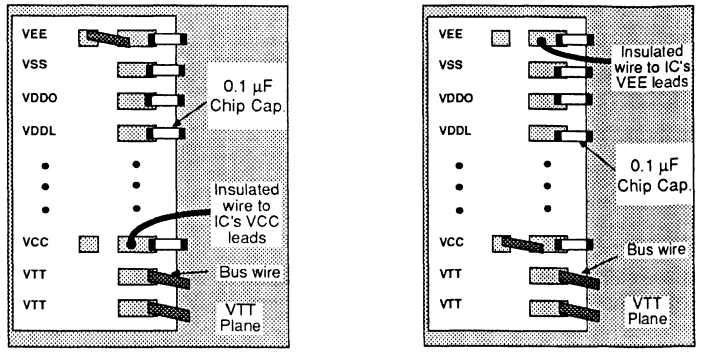


Figure 5. DC Ground Block. Permits connecting a scope to -2 V (VTT) although the system ground is VDD.

90GSKT40) available from GigaBit. These sockets use gold-on-elastomer contact technology and therefore must be pressure contacted to a gold-plated surface for repeated reliable contact. This is the only reason that the 90GUPB top surface is gold plated. If the user does not intend to socket devices, solder-plated 90GUPB boards can be ordered at moderate cost savings from GigaBit under P/N 90GUPB-SP. The inevitable oxidation of solder plated boards with time rules out their use with the high speed socket.



a. Layer 2 = VEE

b. Layer 2 = VCC

Figure 6. VEE and VCC connections at their top layer board entry points

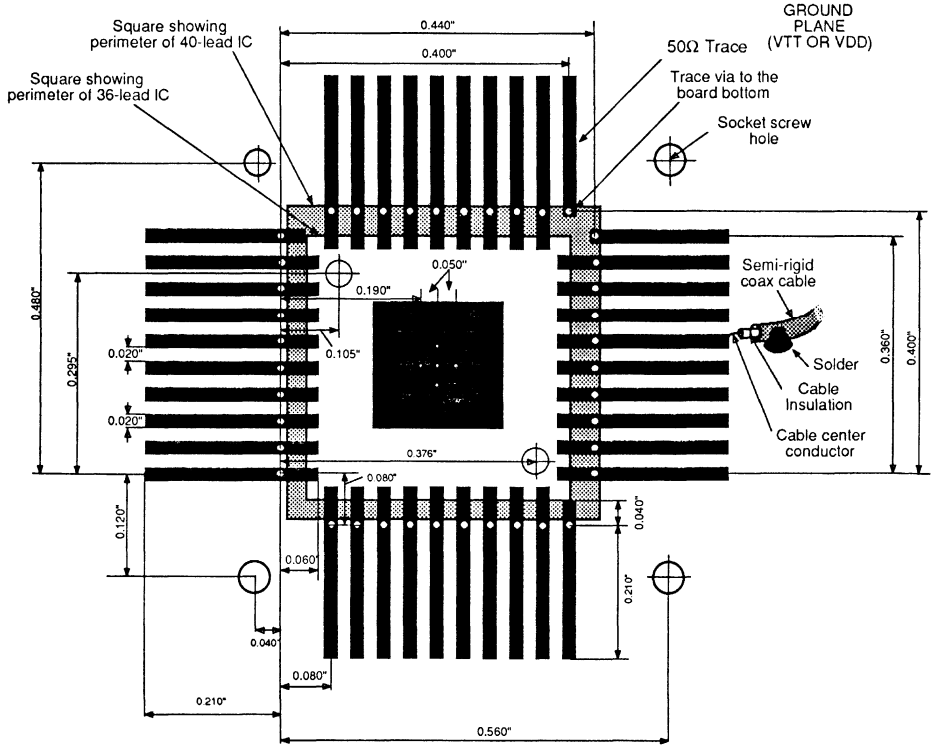


Figure 7. Top view (component side) of a 90GUPB Gaas IC footprint showing an example coax cable connection. The mounting position and boundary of a 36 and 40 I/O IC are shown. The 4 small leads on each side are not contacted when 36 pin packages are mounted.

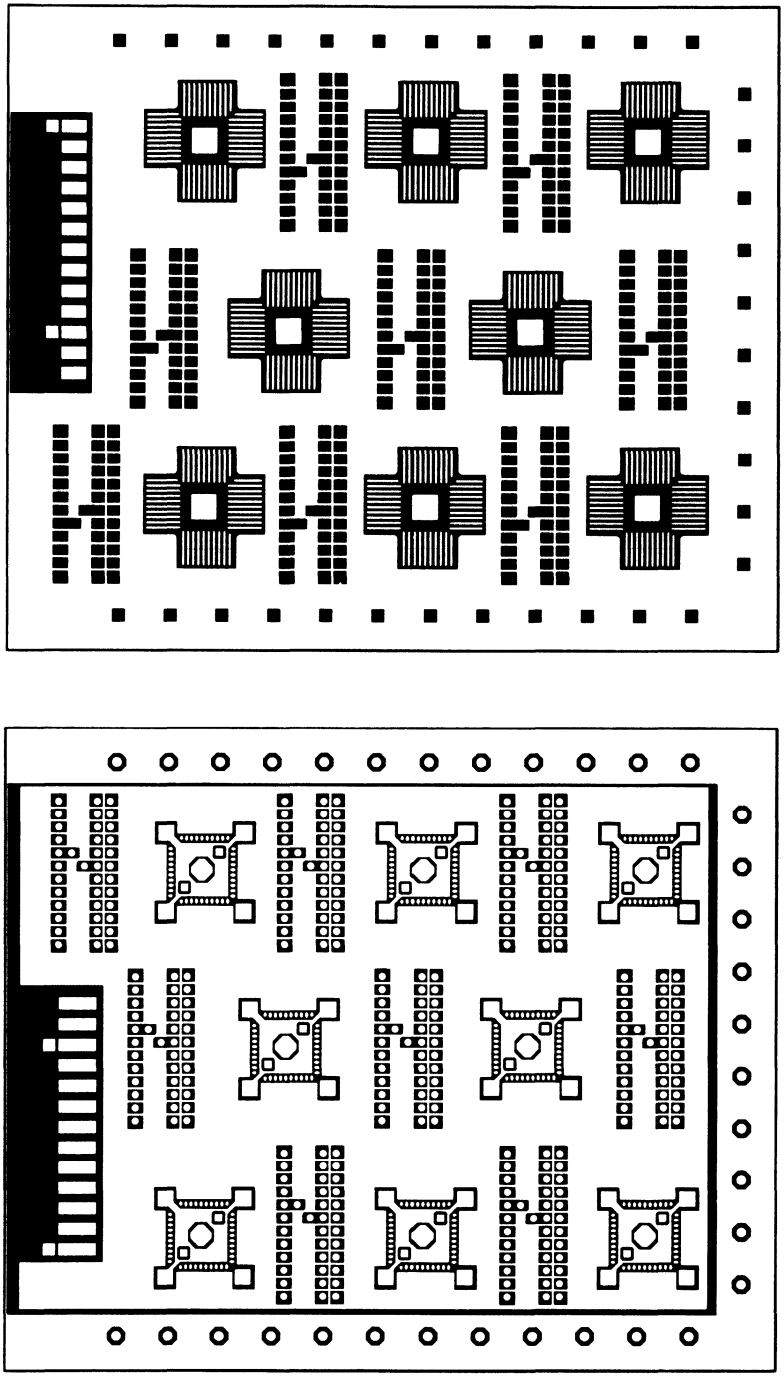


Figure 8: 90GUPB Layout

90GPPS POWER SUPPLY ASSEMBLY

The 90GPPS low-voltage power supply is designed to provide a simple power interface to PicoLogic™, ECL, TTL and CMOS circuits on the prototyping board. It generates the following six regulated voltages: two low-current bias supplies **VREF** and **VBBS**; a medium-current, current sinking supply **VSINK**; and the three primary supplies **VEE, VSS**, AND **VTT**; from a single laboratory supply set to 8 V.

The positive terminal of the laboratory supply should be connected to the black banana jack identified as **VDD** and the negative terminal should be connected to the white banana jack identified as **-E**. The positive output of this laboratory supply may be strapped to ground if VDD is going to be used as system ground. Otherwise, it **MUST** be left floating. For those devices requiring a supply 5 volts more positive than VDD, a second lab supply may be connected to the red banana jack labeled **VCC.** This voltage will pass directly through the prototyping board to the standard connector. The -E laboratory supply should have its current limits set to a level greater than the sum of IEE, ISS and ITT currents.

For additional information, refer to the 90GPPS datasheets.

90GPPS SPECIFICATIONS

OUTPUTS

Supply	Vmax (V)	Vmin (V)	Imax (A)[1]	Regulation[2] Load + Line
VBBS	-0.5	-1.8	+0.20, -0.40	<2%
VREF	-0.5	-1.8	+0.20, -0.40	<2%
VSINK	-0.7	-2.5	-0.200	<2%
VEE	-4.5	-6.0	-3.0*	<2%
VSS	-2.7	-3.7	-4.5*	<2%
VTT	-1.9	-2.5	-1.0*	<2%

INPUTS (Measured with respect to VDD)

Supply	Vnom (V)	
VCC	+5	
-E	-7.5 to -10 V	Maximum current capability with -8.0 V

Board Material: Glass Epoxy
Board Thickness = 0.062"
Board Dimensions: 5" X 6"
[1] Negative currents are currents sunk by the power supply.
[2] Load and Line regulation given for 5% to 100% load
* Output currents may be adjusted to 5 Amp. CAUTION: Overall power dissipation capability of the heat sink (≤40W) should not exceeded.

90GKIT-40 ASSEMBLY AND APPLICATIONS

90GUPB ASSEMBLY:

1. Carefully assign the placement and orientation of ICs and the signal and power routing;
2. Configure the top and bottom planes of the 90GUPB (VTT or VDD);
3. Configure layer #2 for VEE or VCC;
4. Solder a jumper wire on the board bottom between all VSS trace vias and the VSS plane (see Figure 2 and 3 for location of VSS plane on the IC site);
5. Solder all necessary chip decoupling capacitors and chip terminating resistors to the board bottom;
6. Using the supplied 0.034" semi-rigid coax cable, interconnect all high frequency signals on the top of the board;
7. Solder the ICs or install sockets to the board top footprints;
8. Install the SMA connectors;

Each of these assembly steps will be discussed in detail in the following paragraphs. Figure 9 below shows one footprint site as defined on the 90GUPB bottom layer with the location of the power planes.

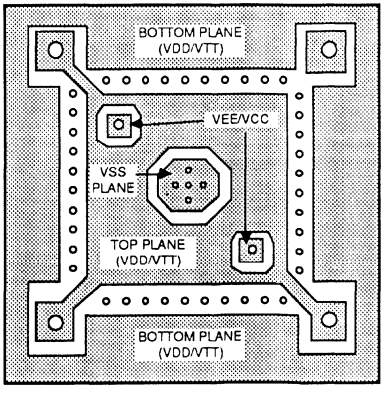


Figure 9. Power planes location at IC site of the 90GUPB

1. Board Layout
Component location and orientation on the board should be carefully assigned to facilitate high frequency interconnect and to maintain equal signal path lengths where necessary. Coaxial wirings delays of approximately 50 ps/cm (120 ps/in.) must be considered when deriving timing diagrams. Since none of the GaAs IC footprints have commited traces, it is possible to mount each of hte ICs in any orientation. The DIP IC (24 or less) pin sites have two feedthrough holes, which are connected to the third layer of the 90GUPB, located next to pins 8 and 18. This facilitates the connection of the VEE pins to the VEE plane for 10K or 100K ECL devices, or, if so configured, VCC to TTL or CMOS parts.

2. See discussion on page 3 and 4.

3. Chip Capacitor and Resistor Placement:
The 90GUPB provides VDD, VTT, and VSS planes at board bottom in close proximity to vias from the upper footprint signal traces so that high frequency chip capacitors and chip resistors can be easily solder mounted as required. If you are providing your own capacitors and resistors, good quality high frequency components should be employed. Chip capacitors and resistors can be mounted either on their side or on their top/bottom, depending on their size and space restrictions.

Chip capacitors and resistors should be placed as follows (see Figures 2, 3 and 10 for details):

At the IC site:
- VEE pins should be decoupled to the VDD plane with 1,000 pF chip capacitors.
- VSS pins should be decoupled to the VDD plane with 1,000 pF chip capacitors.
- VDDL pins should be decoupled to the VSS plane with 1,000 pF leaded capacitors.
- VDDO pins should be decoupled to the VTT plane with 1,000 pF chip capacitors.
- The VBB pin should be decoupled to the ground plane (VDD or VTT) with a 1,000 pF chip capacitor.
- The VSS plane should be decoupled to the VDD plane with a 10,000 pF leaded or leadless capacitor.
- The VDD plane should be decoupled to the VTT plane with a 10,000 pF leaded capacitor.
- A 50Ω chip resistor should be soldered between the terminus point of all high frequency signal lines (whether daisy-chained or not) and the VTT plane.
- For ECL or TTL devices, a 0.01μF leaded ceramic capacitor should be soldered between the high and low power supply rails.
- For devices that utilize a VCC of +5 V, a chip capacitor should decouple the VCC trace vias to the ground plane.

At the board connectors (power entry point):
- All supplies (VEE, VSS, VCC, VTT/VDD)should be decoupled to the top ground plane with 10,000 pF chip capacitors.
- The VSS plane should be decoupled to the VDD plane with a 10,000 pF chip capacitor if VTT is the top ground plane.

For more information on decoupling and termination, please consult Application Brief #3, "Decoupling and Termination Recommendations for PicoLogic™ and NanoRam™ GaAs ICs".

4. & 5. See discussion on page 3 and 4.

6. High Speed Signal Interconnections:
Using the semi-rigid coax provided, wire from each output to succeeding inputs employing the daisy-chain approach. Since PicoLogic™ and NanoRam™ GaAs IC families can drive 25 ohms, it is possible to drive two parallel 50Ω lines from a single source. The coax high speed lines are critically important to the successful microwave frequency operation of the configured board. For this reason, a good deal of care in this portion of the assembly process is necessary. To prepare ends of the coax, score the outer shield and inner dielectric with a sharp wire cutter 0.25 cm (0.1 inches) from each end. A gentle twisting of the wire stripper will cause the shield to be penetrated and permit the cutter to cut through the dielectric. Do not leave any unshielded dielectric exposed. The coax should be placed such that the edge of the outer shield is as close as possible to the microstrip footprint trace without contacting it. The coax center conductor is soldered to the 50Ω microstrip trace emanating from the IC. The outer coax shield must be soldered to the top ground plane at both ends of its length to establish good, local grounds.

7. Soldering Technique:
The following material has been excerpted from Application Note 2 "Guidelines for the Use of Digital GaAs ICs" by Carl Deierling.

Due to the small geometries and low capacitance inherent in high speed devices, the sensitivity to electrostatic discharge is increased. Therefore, handling and soldering precautions similar to those observed with ECL or CMOS devices should be followed when working with GigaBit

Logic components.

This section provides the user with proven successful techniques for manual LCC and C-Leaded attachment and removal.

a. Place the board on a grounded work station and ground the operator with an appropiate wrist or ankle wrap.
b. Apply a thin layer of resin flux on the PC board footprint to be soldered.
c. Place the LCC on the flux coated footprint and visually align all four sides.
d. Holding the part in position with one finger, apply a temperature controlled (550° F to 625° F) fine tip soldering iron and a small amount of 63/37 resin core solder to one corner until the solder flows between the LCC and the board (approx. 1 second).
e. Tack down the opposite corner using the same procedure.
f. Feed solder and the iron tip along all four sides of the package and its interface with the board as fast as the solder will flow (one of two seconds per side). Visually verify and touch up as needed.
g. Remove any excess solder and clean the board using an appropriate solvent.
h. Inspect the assembly for a clean fillet and the absence of any soldering bridging.

TIP: To prevent solder from flowing through the via holes and contaminating the gold traces, place a piece of scotch tape over the via holes on the top of the 90GUPB.

Manual LCC and C-Leaded Package Removal:

a. Place the board on a grounded work station and ground the operator with a wrist or ankle strap.
b. Apply a thin layer of resin flux around the perimeter of the part to be removed.
c. Preheat the removal tool for approximately 10 minutes.
d. Grasp the LCC with the preheated removal tool for approximately 2 seconds applying a gentle twisting motion to ascertain when the solder ha liquefied.
e. When loose, immediately lift the part and place it on a work surface to cool.
f. Examine the board for any lifted pads and repair them as necessary.
g. Remove excess solder and clean the board to remove flux and debris with an appropriate solvent.

8. Installation of SMA connectors:

The 90° SMA connectors should be inserted into the bottom of the board in the desired locations and the four ground lugs soldered into position. The plane surrounding the SMA sites is connected to the top plane of the 90GUPB. In this manner, the shell of the SMAs is at system ground. Make sure the flange on the connector is not so wide that it touches the adjacent plane.

Right angle connectors were chosen so that I/O cables could enter the 90GUPB parallel to its surface, thereby avoiding interference with the mating 90GPPS power supply card below it. Depending upon user requirements, another type of PC board mount SMA connector could be used as long as it fits properly.

INTERFACING THE 90GUPB PROTOTYPING BOARD AND THE 90GPPS POWER SUPPLY CARD:

The 90GPPS voltages are brought up to the 90GUPB board as follows (Pin # 1 on the 90GPPS is the one closest to the banana jacks):

Connector Pin #	90GPPS Outputs	90GUPB Input Labels
1	VEE	VEE
2	VSS	VSS
3	VDD	VDDO
4	VDD	VDDL
5	VBBS	VLCL
6	VREF	VLCH
7	**	VDCL
8	VSINK	VDCH
9	VSINK	VICL
10	VCC	VICH
11	VCC	VCC
12	VTT	VTT
13	VTT	VTT

** This output may be used for generating a -4.5 V VEE for 100K ECL. Consult the 90GPPS datasheet for details.

Recommended assembly sequence:

1. Install the supplied 13 pin connector on the 90GPPS power suppy card.

2. Install the standoff on the assembled 90GUPB board.

3. Insert the 13 pin connector installed on the 90GPPS into the respective holes on the 90GUPB. Pin #1 on the 90GPPS (the one closest to the banana jacks) corresponds to the VEE input on the 90GUPB. Note that the pins of the connector protrude approximately 0.3" on top of the 90GUPB. Solder the pins in place.

COMPONENT SOURCES

90° SMA Connentors	- Omni Spectra 2064-0000-00 - Sealectro Corp. 050-653-0000-310
0.034" Semi-rigid coax	- Precision Tubes CE50034
50Ω Chip resistors	- Mini Systems WA47PG50R0F
1,000 pF chip capacitors	- Johanson Dielectrics 500-R09-B-102-ZP4

Extractor tool for 36 or 40 pin pkgs.
- Nu-Concept Systems Inc. Pak-XTrac DM Series (for 36, 40, or 68 pin packages)

RECOMMENDED READING

1. **AN-2** Application Note 2. "Guidelines for the Use of Digital GaAs ICs"
2. **AN-4** Application Note 4. "Interfacing PicoLogic™ and NanoRam™ ICs to other Logic Families".
3. **AB-3**: "Decoupling and Termination Recomendations for PicoLogic™ and NanoRam™ GaAs ICs".

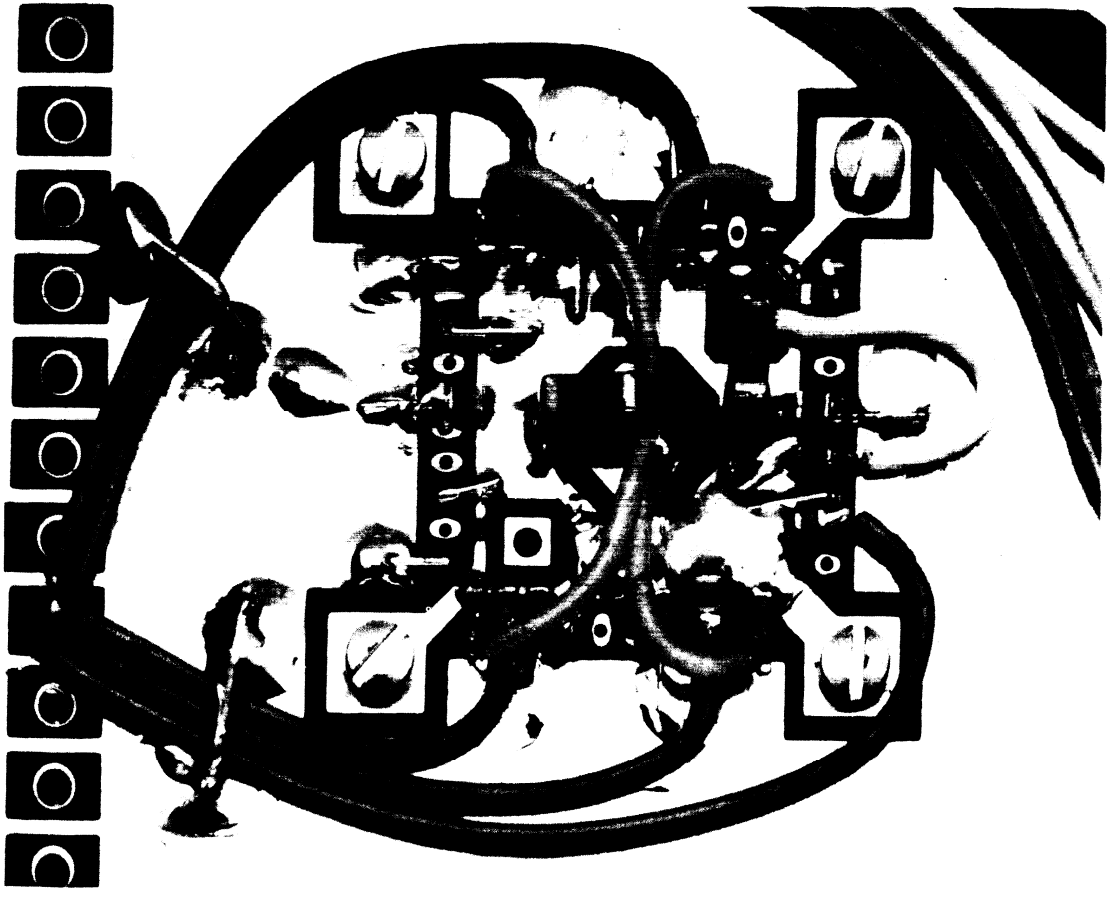


FIGURE 10: Close-up view of a 90GUPB bottom footprint site showing decoupling capacitors, termination resistors and DC supply wiring in place.

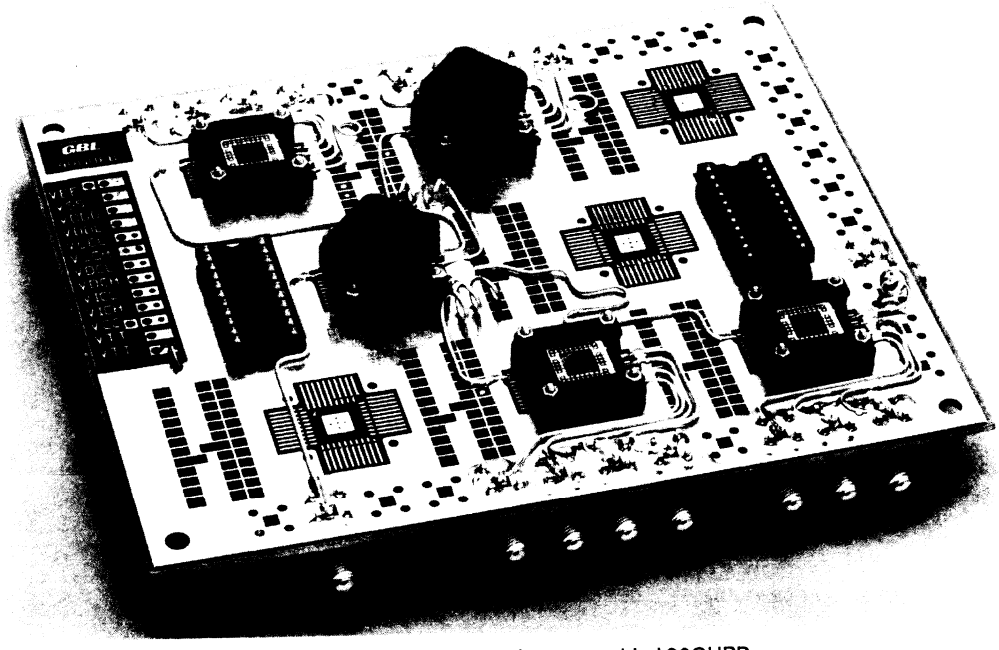


FIGURE 11: Top view of an assembled 90GUPB

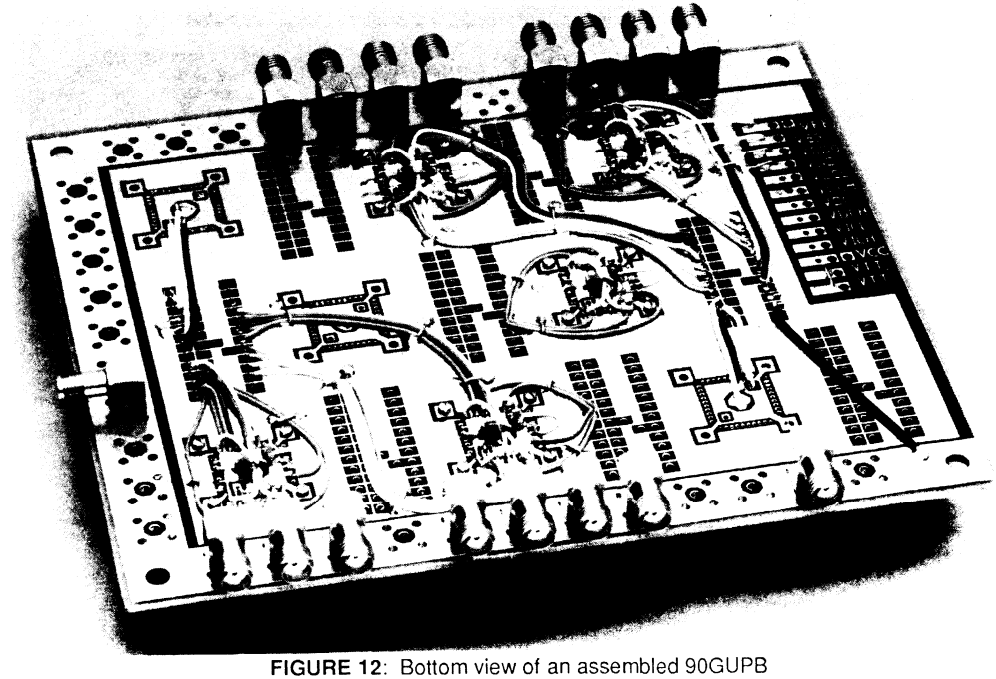


FIGURE 12: Bottom view of an assembled 90GUPB

High Speed Leadless Chip Carrier Socket (For 40 I/O "L" Package)

FUNCTIONAL DESCRIPTION

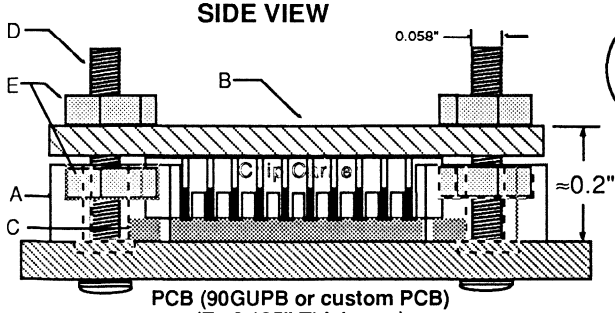
The solderless Socket 90GSKT-40L has been designed to provide a socket useable to 2.5 GHz for the 40 I/O leadless chip carrier package (part number suffix "L") widely used by GigaBit Logic for standard products as well as low pin count standard cell based ASIC designs. Although it is difficult to precisely specify the r.f. characteristics of the 90GSKT-40L since these are somewhat dependent upon the pin functions of the socketed device, use of the socket results in minimum discontinuities and loss of performance for nearly all applications. Applications Brief 1, available from GigaBit, shows that the 90GSKT-40L is capable of preserving the very fast (~100 ps) output edges of the 10G012B driver/comparator.

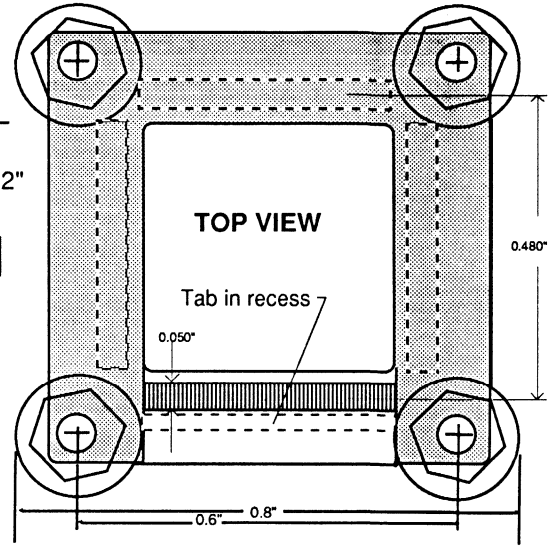
The 90GSKT-40L is only specified for use with the L-suffix 40 I/O leadless chip carrier package and not with the "C"-leaded version of this package. Use with the C-lead package may cause lead deformation.

ASSEMBLY INSTRUCTIONS

The four elastomeric connectors (P/N 90GSKT40L-3) should be inserted into the four slots in the socket base (P/N 90GSKT40L-1) with the tabs that extend from the connectors placed into the recessed areas on the bottom of the socket base towards the edges. This is best accomplished by laying the connectors on a flat surface and carefully placing the socket on them, locating them as necessary with a thin sheet of cardboard. Caution should be used when handling the connectors since the fine gold wires that form the contact can be damaged if handled with tweezers or fingers. After the connectors are placed into the socket base, place the base on the PCB aligning the four socket screw holes to mating holes in the PCB. Insert the four screws (P/N MS 16996-4) from the bottom of the PCB through the base as shown in the drawing. Use four supplied hex nuts (P/N NAS-671-C0) placed in the cavities in the top portion of the base to tighten the socket base to the board. Some caution must be exercised until the base is securely fastened to the board to insure that the elastomeric connectors are not dislodged. Once these screws are tightened, the elastomeric contacts are held rigidly in place.

The socket is now ready to accept the IC package, which is then held in place with the 90GSKT40L-2 lid, and four additional hex nuts. A heatsink, if employed may be epoxied either before or after mounting in the socket. If the 90GHS40B large heatsink (available from GigaBit) is used, it should be rotated 45° to provide clearance for the screws.





BILL OF MATERIALS

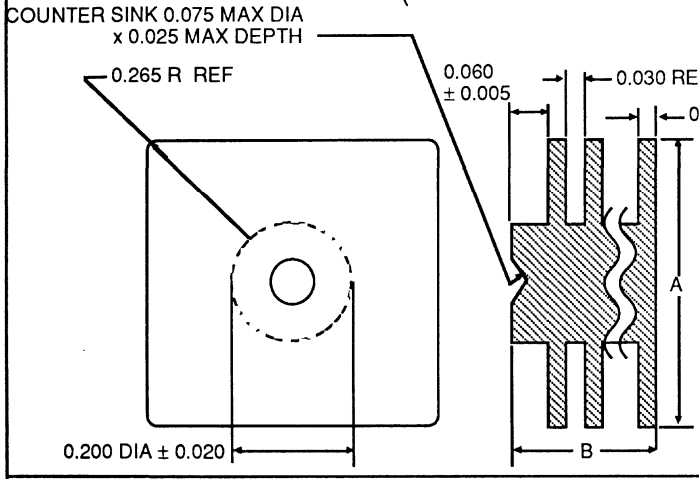
ITEM	DESCRIPTION	DWG #/PART #	QTY
A	Molded socket base (Ryton)	90GSKT40L-1	1
B	Socket lid (Ryton)	90GSKT40L-2	1
C	Elastomeric connector (.047 by .400 lg)	90GSKT40L-3	4
D	#0-80 x .375" screw (stainless)	MS 16996-4	4
E	#0-80 hex nut (stainless)	NAS-671-C0	8

GigaBit Logic

90GHS36A
90GHS40A
90GHS40B

Heatsinks for 40 I/O (L and C) and 36 I/O (F and L36) Packages

HEATSINKS PRIMARILY FOR 40 I/O PACKAGES (90GHS40A AND 90GHS40B)

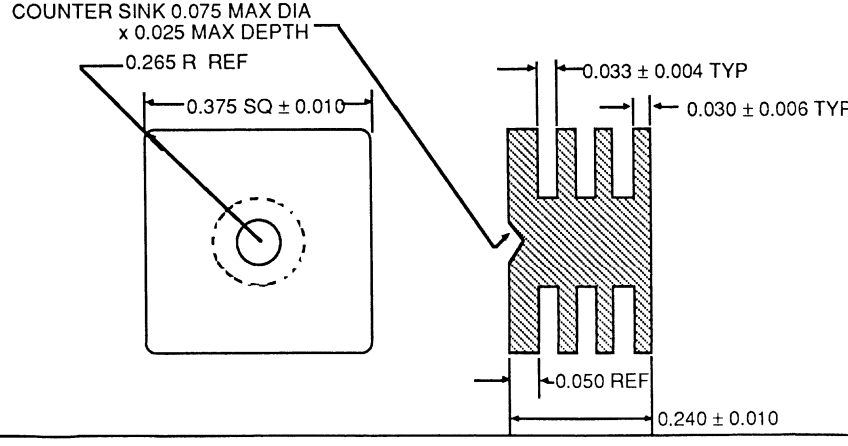


DIMENSIONS

GBL P/N	90GHS40A	90GHS40B
A	0.500 ± 0.010	0.625 ± 0.010
B	0.270 ± 0.010	0.330 ± 0.010
# OF FINS	4	5

Thermally conductive, electrically non-conductive epoxy is recommended for heatsink attachment. Examples are Ablestick 789-4 or 561K, or Thermalloy Thermalbond™ or equivalent.

HEATSINK FOR 36 I/O PACKAGES (90GHS36A)



STANDARD CELL LIBRARY

TABLE OF CONTENTS

SC5000
GaAs STANDARD CELL LIBRARY

DISTINCTIVE CAPABILITIES

- Automated GaAs circuit design
- Wide selection of pre-designed cells
- Optimized for 1 - 2 GHz operation
- Low power dissipation of 1-2 mW per gate
- Typical loaded gate delays of 50 - 150 ps
- Configured for auto place and route
- Production proven process technology
- Guaranteed AC and DC specifications
- ECL, TTL and CMOS I/O capability
- High density circuit technology
- 0°C to +85°C operating temperature range
- Military temperature range available
- Superior radiation tolerance
- Packaging and test support included

PROGRAM DESCRIPTION

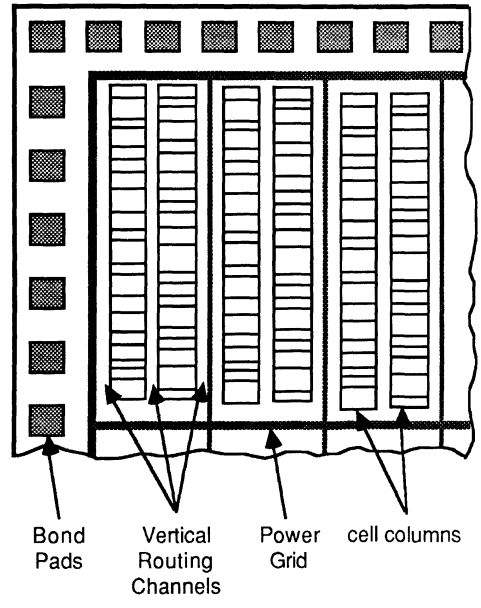
GigaBit Logic's SC5000 GaAs Standard Cell Library contains a variety of pre-designed, pre-characterized cells which provide an automated and straightforward approach to high speed, low power integrated circuit design. The circuit designer utilizes the electrical and functional description of the handcrafted cells to construct his device schematic in an automated CAD environment, thus avoiding transistor level detail design. The cell library softwareand design manual available from GigaBit is supported on commercially available CAD workstations.

The cells are based upon GigaBit's production proven Gallium Arsenide metal-semiconductor field effect transistor (MESFET) process and follow the ECL I/O standards and GaAs power supply voltages established by the PicoLogic™ family of GaAs components. Each cell has been optimized to offer ultra-fast operation at minimum power levels.

Standard cell design techniques offer the performance, design flexibility, and low production costs normally associated with full custom design while, at the same time, minimizing development time, cost, and risk. The front end design implementation is identical to a gate array approach, however, unlike gate arrays, standard cell designs use only those cells and interconnections actually needed to complete the design, resulting in higher performance, smaller die sizes, and lower power dissipation.

GigaBit Logic is an industry leader in the design and manufacture of GaAs digital circuits, static RAMs, and prototyping tools. GigaBit also offers complete foundry and design services.

DEVICE TOPOLOGY



DESIGN KIT

- Standard Cell Library Software
- Comprehensive Design Manual
- Detailed Cell Datasheets
- Full Day on Location Training Course
- Design and Applications Support

RECOMMENDED PROGRAM FLOW

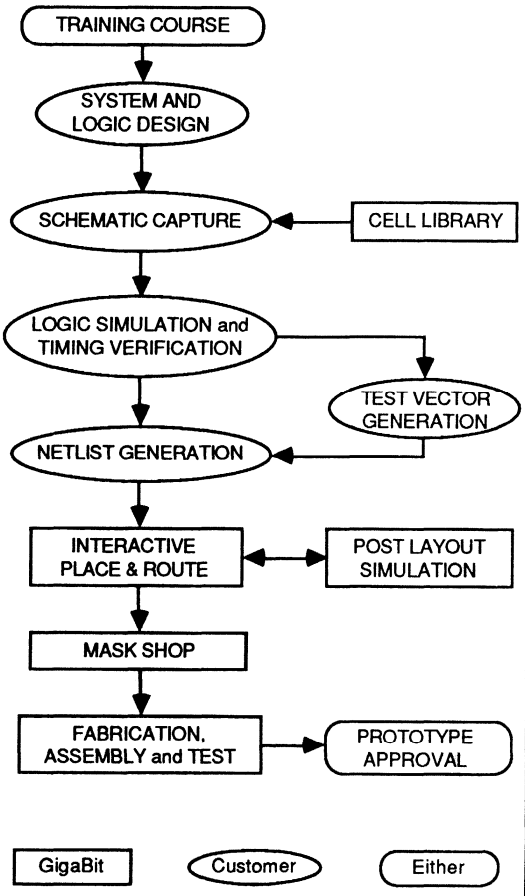
First time standard cell customers are invited to host a full day training seminar at their location or attend one of the quarterly GaAs design courses at GigaBit's facilities.

The recommended design flow requires the customer to complete circuit schematic capture utilizing GigaBit's cell library. The circuit functionality is verified and performance estimated by performing logic simulation and timing verification. The customer then transfers the verified netlist, along with the initial die floorplan, preliminary pinout diagram, and test vectors to GigaBit.

Utilizing in-house experts and an extensive CAD facility equipped with highly interactive design tools, GigaBit performs circuit layout in accordance with the circuit information contained in the netlist. The final layout is optimized by GigaBit to achieve maximum speed and minimum die size. Actual circuit fan-outs, wire-lengths and associated capacitances are used for post-layout simulation to provide highly accurate performance projections. GigaBit then generates masks and fabricates the device wafers using it's production proven process technology.

The final packaged devices are tested for functionality utilizing customer generated test vectors. High speed performance is tested to the customer's specification by GigaBit and guaranteed over temperature. Prototypes that pass all of these tests are shipped to the customer for approval. Volume production is supported.

GigaBit offers a complete range of software tools and design services to accomodate a customer's particular development needs. In all cases, GigaBit's commitment to quality assures efficient, fast- turn, error free prototypes.



CUSTOMER TRANSFERS TO GIGABIT

- VERIFIED NETLIST
- DEVICE FUNCTIONAL DESCRIPTION
- DEVICE TIMING SPECIFICATIONS
- PRELIMINARY FLOORPLAN
- SUGGESTED PINOUT
- FUNCTIONAL TEST VECTORS
- SIMULATION FILES

TYPICAL GIGABIT MILESTONES

• CIRCUIT LAYOUT:	4 to 8 weeks
• BACK-ANNOTATED SIMULATION:	2 to 4 weeks
• MASK SET:	2 weeks
• FABRICATION:	6 to 8 weeks
• ASSEMBLY AND TEST:	2 to 4 weeks
• DELIVERY OF FINAL PROTOTYPES:	16 to 26 weeks after receipt of schematic

SC5000 STANDARD CELL REFERENCE GUIDE

GigaBit's cell library provides the design engineer with a collection of proven building blocks. The cell library software and design manual contain complete information on each cells logic symbol, logical function, timing characteristics, input capacitance, power dissipation, and geometry. Below is a summary of cell attributes.

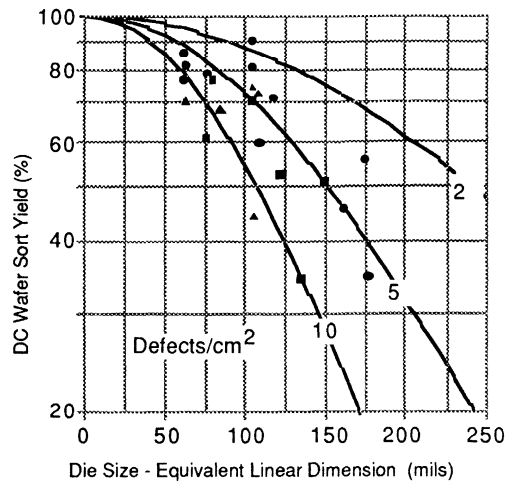
CELL NAME	FUNCTIONAL DESCRIPTION	TpLH/TpHL (ps)F.O.=1	CLOCK FREQ.	POWER (mW)
I/O CELLS				
BICB	ECL DIFF. INPUT (COMPL. OUTPUTS)	104/83		35
BII	ECL INVERTING INPUT BUFFER	92/41		8
BIICK	ECL INVERTING CLOCK BUFFER	125/46		42
BIIT	TTL INVERTING INPUT BUFFER	80/33		8
BINR	ECL THREE INPUT NOR GATE	136/56		13
BOFDMS	M-S D FLIP FLOP OUTPUT BUFFER	323/313	2.0 GHz	40
BOI	INVERTING OUTPUT BUFFER	106/85		21
INTERNAL CELLS				
ACC2	2 BIT ACCUMULATOR	465/208	1.2 GHz	85
AOI	TWO INPUT AND-OR-INVERT	93/61		3
CPG1	CLOCK PULSE GENERATOR	200	1.6 GHz	46
DIFF1	DIFFERENTIAL LINE DRIVER	200/150		11
DIV2A	DIVIDE BY 2 PRESCALER	172/214	2.2 GHz	25
DTGL1	TOGGLE D FLIP FLOP (edge triggered)	351/335	2.3 GHz	80
DTGL2	TOGGLE D FLIP FLOP (master-slave)	285/310	2.75 GHz	50
FDC	D FLIP FLOP WITH COMPL. INPUTS		1.0 GHz	11
FDC2	D FF (COMPL. INPUTS, PRESET, CLEAR)	323/280	2.2 GHz	52
FDMSR	M-S D FLIP FLOP with RESET	192/315	1.1 GHz	10
FDMSS	M-S D FLIP FLOP with SET	315/191	1.1 GHz	10
FDRH	D FLIP FLOP (RESET & OUTPUT ENABLE)		1.6 GHz	23
FDRHM2	DUAL INPUT D FLIP FLOP		1.6 GHz	23
FDM2A	D FLIP FLOP with MULTIPLEXED INPUTS	399/302	1.25 GHz	17
FDM2B	D FLIP FLOP with MULTIPLEXED INPUTS	228/316	2.1 GHz	63
IV	INVERTER	89/48		2
IVB	INVERTER BUFFER	75/35		2
LD1	D TYPE LATCH ELEMENT (COMPL. INPUTS)	250/150		5
LD2	D TYPE LATCH ELEMENT	335/160		4
ND2	TWO INPUT NAND GATE	93/53		3
NIV	NON-INVERTING BUFFER	18/9		11
NR2	2 INPUT NOR GATE	105/52		2
NR2B	2 INPUT NOR GATE BUFFER	90/39		2
NR3	3 INPUT NOR GATE	120/57		2
NR4	4 INPUT NOR GATE	134/60		2
NR5	5 INPUT NOR GATE	148/64		2
XN2	2 INPUT EXCLUSIVE NOR GATE	132/130		4
XO2	2 INPUT EXCLUSIVE OR GATE	132/131		7

PRACTICAL DESIGN CONSIDERATIONS

GigaBit Logic's commitment to commercial high volume integrated circuit manufacturing has resulted in industry leading yield results for ultra-fast LSI complexity devices. The figure to the right represents actual wafer sort yields (functional and parametric) for logic and memory devices manufactured at GigaBit during the past year as a function of the square root of the device die area. The three dashed lines represent the expected yield by the Murphy model given different fab defect levels.

Using the Murphy model interpretation, it can be seen that the defect densities of GigaBit's process fall in the 5 defects per square centimeter range. These results indicate excellent process control and yields in parity with silicon devices.

As the leader in the design and fabrication of digital and analog GaAs ICs GigaBit has focused on manufacturing quality and reliability and a commitment to meet or exceed our customer's requirements.



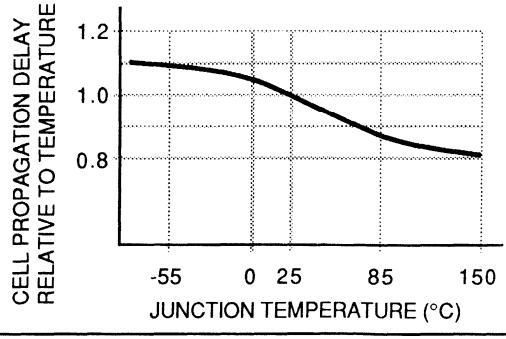
• = Actual device yield results

PROPAGATION DELAYS

Propagation delays of GigaBit cells are a function of several factors including:

- intrinsic cell delay
- fan-out capacitance
- interconnection capacitance
- junction temperature
- supply voltage
- processing tolerance

The cell library software from GigaBit contains timing equations which take these factors into account during the timing verification process. The figure to the right depicts typical cell performance over an extended temperature range.



CUSTOMER ON-SITE TRAINING SEMINAR

GigaBit offers a full day training seminar and software installation session for standard cell program customers. The seminar takes place at the customer's facility to allow hands-on design experience and maximum participation. The lecture portion is presented by a GigaBit Logic Application Engineer and covers GaAs and Standard Cell technology and design considerations. The remainder of the session involves software loading and demonstration. This session provides a sound platform for initiating high speed GaAs cell based design. More extensive training seminars covering GaAs custom circuit design are available for foundry customers. For non-domestic customers GigaBit offers the training session on a quarterly basis at its Newbury Park, Ca. facilities.

FOUNDRY SERVICES

TABLE OF CONTENTS

Gallium Arsenide Foundry Services

DISTINCTIVE CAPABILITIES

- Depletion and Enhancement/Depletion mode MESFET processes
- All "dry" processing - 1μm design rules
- High yield DSW lithography
- Fully implanted active layers
- Planar metal and via interconnects
- Two level metal interconnect standard
- Three level metal interconnect available
- Proven high volume production
- Demonstrated yield and reliability
- 3 inch LEC GaAs wafers
- Typical gate delays of 50 to 150 ps
- Digital logic to 4 GHz
- Static RAM to 1 ns access time
- Analog/RF to 5 GHz
- Proprietary SPICE models

AVAILABLE SERVICES

- Corporate design training seminars
- Technology transfer includes design rules, SPICE models, and process description
- CAD support and verification services
- Mask set composition and generation
- Prototype or production wafer runs
- Wafer saw and die processing
- Die assembly in JEDEC outline 40 and 68 pin high speed packages
- Functional and DC parametric test on die or packaged units
- Reliability testing and environmental screening facilities
- Standard Cell and Device Libraries

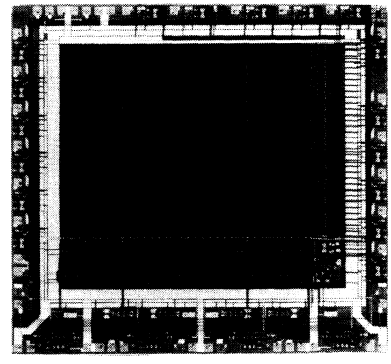
For high speed integrated circuit applications well above the maximum frequency range of silicon bipolar IC's, GigaBit Logic's one micron (1μm) depletion or enhancement/depletion mode MESFET gallium arsenide (GaAs) processes are ideal.

GigaBit's state-of-the-art GaAs wafer processing technology utilizes the most advanced equipment in an ultra-clean Class 10 environment. High volume standard device production experience allows GigaBit customers to take advantage of rapid improvements in both yield and performance. In-house training seminars by GigaBit experts enable customers to quickly move up the GaAs IC design learning curve.

More than just a foundry service, GigaBit is a complete IC company offering design, development, manufacturing, testing, and reliabilty services in a commercial production environment.

Design techniques encompassing a broad range of speed-power objectives are accommodated. The process supports both digital and analog/RF IC design. Proven design examples are available.

Complete testing and packaging facilities support GigaBit's volume shipments of standard and custom products.



GigaBit's LSI complexity 4K-bit registered SRAM

CUSTOM DESIGN KIT

- Extensively documented design rules
- Fully correlated SPICE models
- Process and Device Characteristics
- PCM test patterns and specifications
- Optional design training seminars

PROCESS DESCRIPTIONS

GigaBit offers a full selection of production proven MESFET process options. Customers have four process options to choose from, and with help from GigaBit experts can select the best technology for their specific circuit requirements. The available processes and associated typical device parameters are listed below.

- Depletion mode MESFET (D)
- Low Power Depletion mode MESFET (LPD)
- High Margin Enhancement/Depletion mode MESFET (HME/D)
- Enhancement/Depletion mode MESFET (E/D)

TYPICAL DEVICE PERFORMANCE PARAMETERS

DEVICE PARAMETER	PROCESS:	D	LPD	HME/D		E/D	
	FET TYPE:	D-MESFET	D-MESFET	E/D	D	E	D
Pinchoff Voltage, Vp (Volts) (note 1)		-0.6, -1.0 (note 2)	-0.5	-0.25	-0.6	+0.15	-0.5
Current (Vds = 2.5V)							
IDSS (mA/50μm), Vgs=0V		2.0, 5.0	2.2	----	2.8	----	2.2
IDS (mA/50μm), Vgs=0.6V		----	8	5.6	9	2.2	8
Ke-value (external) ($\mu A/V^2 \cdot \mu m$) (note 3)		115, 105	145	165	140	195	145
Transconductance (external)							
Gme (mS/mm), Vgs=0V		125, 155	140	----	160	----	140
Gme (mS/mm), Vgs=0.6V		----	245	235	255	180	245
SPICE Parameters (note 4)							
Ki (internal) ($\mu A/V^2 \cdot \mu m$)		150, 145	220	225	200	320	220
Source Resistance, Rs ($\Omega \cdot \mu m$)		2000, 1750	1150	1300	1050	1500	1150
f_τ (GHz) Peak current gain-bandwidth product		>15	>18	>18	>18	>18	>18
Gate Length (μm)		<1.0	<1.0	<1.0	<1.0	<1.0	<1.0
Number of Masks Levels		9	9	11		11	

Notes:
1. Vp is analagous to VTO in the SPICE JFET model.
2. D-mode pinchoff voltage can be customer specified from -0.6V to -1.0V.
3. Ke is useful for estimating Ids (Ids = Ke [Vgs(ext) - Vp] ^{2} ; it is lower than the Ki (or SPICE BETA) value because of source resistance degeneration.
4. Ki is analagous to BETA and Rs to RS and RD in the SPICE JFET model.

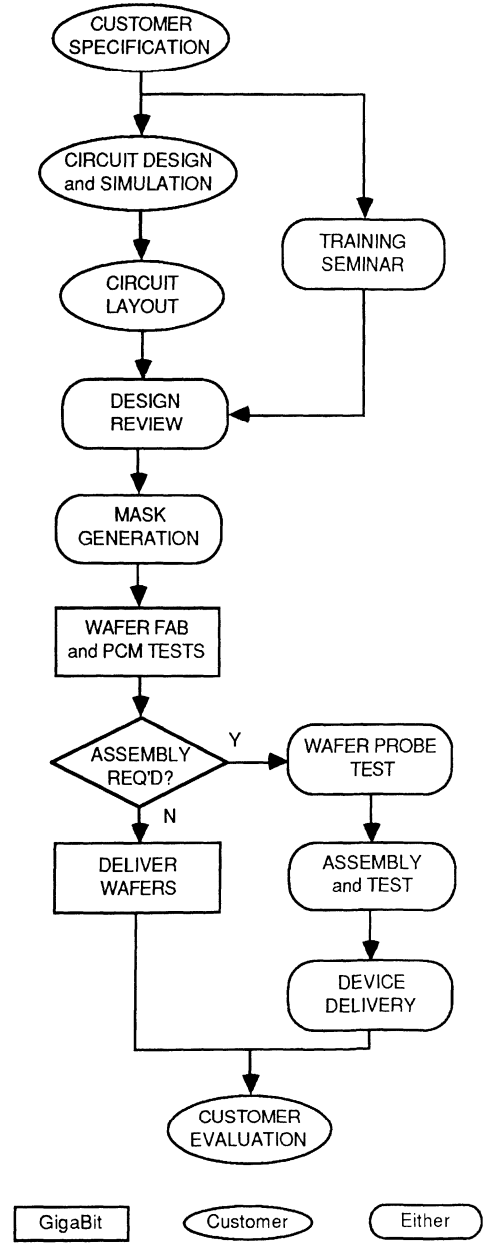
TYPICAL FOUNDRY PROGRAM FLOW CHART

GigaBit's foundry services and training seminars are offered in a flexible plan which allows a customer to structure design and support activities to best suit their project.

An optional training program can wrap-around the customer's first design. Utilizing the design and technology information transferred from GigaBit, the customer performs circuit design, simulation and layout. After circuit verification, the circuit layout data in GDSII magnetic tape form or actual masks can be sent to GigaBit for device fabrication. GigaBit's mature process ensures high performance and reproducible device characteristics.

Wafers are tested for conformance to PCM specifications and visually inspected for quality assurance. As an option, DC parametric and functional probed wafers or tested packaged components can be delivered to the customer's requirements. High speed test development is also available as an option.

GigaBit has the facilities, resources, and expertise to participate in any of the development phases to accomodate customers with various resource and experience levels.



CAD SERVICES

A complete set of proven CAD tools and services are available to speed the design process. GigaBit's extensive standard product design and development experience has put several years of enhancement and refinement into it's circuit design tools.

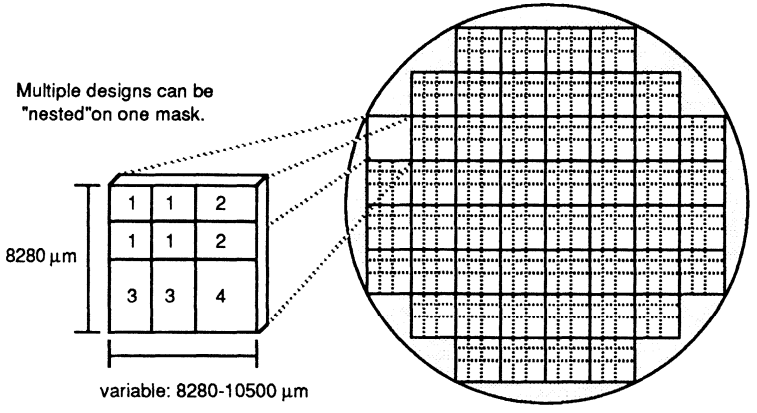
For instance, GigaBit's proprietary SPICE circuit simulation model provides highly accurate predictions of actual device performance allowing the customer to quickly move from design to production. GigaBit's SPICE model is fully correlated with actual device performance over operating temperature and supply voltage ranges and includes accurate models for hysteresis.

Other CAD tools and services include:

- Complete software for design verification: Layout versus Schematic, Electrical Rule Checking, and Design Rule Checking
- Layout database translation (CIF to Calma GDSII)
- Standard Cell Library
- Proprietary logic simulator
- Graphics post processor for SPICE signal analysis
- Mask shop tape preparation
- CAD system time rental

MULTI-PROJECT WAFERS INCREASE DESIGN PRODUCTIVITY

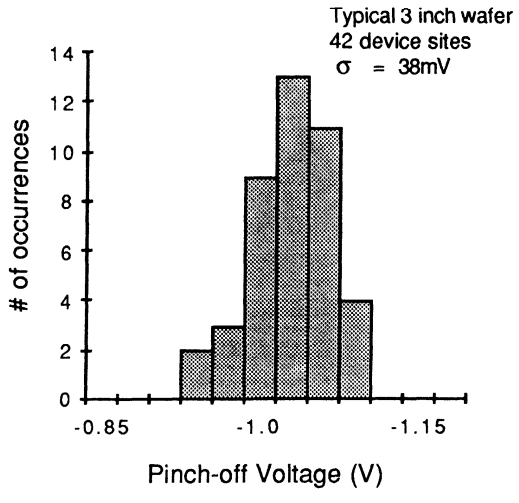
Using advanced wafer stepper technology and flexible manufacturing techniques a corporate multi-project chip (MPC) can be easily created. By combining several designs or devices on one mask, unit cost and development time can be dramatically reduced.



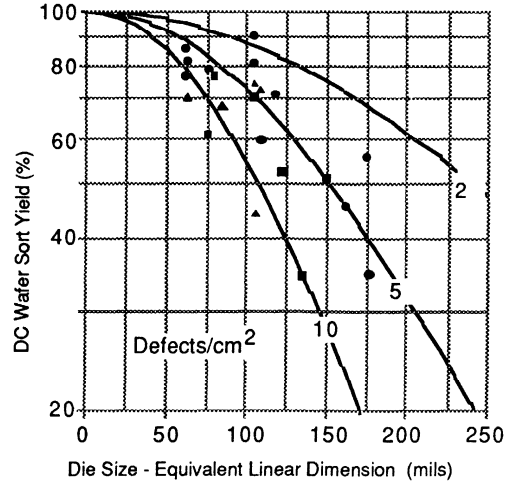
GigaBit uses only 3" LEC GaAs substrates to maximize productivity and yield.

GigaBit's state-of-the-art 1µm photolithographic process uses advanced 10X (reticles are ten times the actual feature size) wafer steppers. Direct step on wafer (DSW) reticles are used to "step" the device image in repeated exposures across the wafer. The reticle size can be varied in dimension to accomodate a die floor plan that produces the desired die counts of each device type. GigaBit's experience with dozens of MPC reticle sets guarantees a smooth transition into die test and assembly operations.

Threshold Voltage Uniformity



Device Yield Characteristics



• = Actual device yield results

DESIGNER'S GUIDE

TABLE OF CONTENTS

Guidelines For The Use Of Digital GaAs ICs

Application Note #2. By: Carl Eggert Deierling

I. INTRODUCTION

Digital GaAs IC's, after twenty years of R&D activity, have become a manufacturing reality, with several manufacturers completely dedicated and others having a division dedicated to their commercial supply. Recent advances in material quality precipitated by the LEC (Liquid Encapsulated Czochralsky) crystal growing process and advances in fine line processing techniques have led to the maturation of this high speed technology, evolving from the laboratory environment to a volume producible commodity product.

Circuits could be designed with GaAs MESFET's (Metal-Semiconductor Field Effect Transistors) and Schottky Diodes to operate at the I/O levels of any existing logic family, or levels unique to itself. Due to the fact that GaAs is designed to provide speed in critical timing applications, it will serve to release the bottleneck in high speed systems where ECL is presently used. For this reason GigaBit Logic GaAs IC's are designed to operate with ECL I/O levels. The system design and layout rules which are applicable to ECL are generally applicable to GaAs, but they must be tightened and more rigidly enforced. A good background in designing with ECL, and reference to design guides available from major ECL logic manufacturers[1,2] will prove highly beneficial. This application note will not attempt to replicate the information contained in these manuals, but will supplement them in those areas unique to the even higher speeds of GigaBit's IC's.

Packaging issues and trade-offs will be discussed first. **Section III** will evaluate the suitability of various board materials, with particular emphasis on the use of glass epoxy for multi-gigahertz signals and surface mount packages with relatively high power dissipation. **Section IV** covers signal interconnection options for higher speed logic, emphasizing the necessity to treat all signal paths as transmission lines instead of simple conductors. **Section V** describes the options available to increase device fanout to greater than unity. **Section VI** illustrates the effects of capacitive loading when driving multiple inputs and outputs (such as would be found in daisy chaining or bus driving) and the means to compensate for it. **Section VII** deals with unused inputs and outputs, while **Section VIII** discusses the ac coupling of input signals. **Section IX** explains the necessity for and the means to assure stable power supplies extending to the pins of the device. **Section X** provides information on power pin decoupling as a means to assure that sufficient charge is available at the pins of the IC. The last two sections provide some information for both automatic and manual assembly of SMT packaged devices and for unpackaged die.

II PACKAGES

GigaBit offers a combination of packages to fulfill various applications. A 36 pin flat pack, which should be mounted upside down to provide optimum heatsinking, and leadless chip carrier (LCC) are defined as package types F-36 and L-36 respectively. Two 40 pin packages are also available to provide additional pin count and greater heat dissipation capability.[3] The 40 pin LCC is defined as L-40 and a 'C' leaded version is designated C-40.

Since the Flatpack has a conductive metal lid both top and bottom at VSS potential, and the 36 pin LCC has thermal vias at VSS potential, care must be taken to avoid shorting pc traces to these lids or vias. Thermally-conducting/electrically-insulating material such as Silpad (available from Bergquist), or mica placed between the package and the board may be used under the flatpack to permit traces to pass under the flatpack. It should be noted that the 40 pin LCC and C lead package have a recessed electrically floating metal lid which eliminates the requirement for this insulation. Care should be taken if controlled impedance lines are routed under any of the packages, since the package itself will add a second ground plane converting the microstrip to a stripline, with a corresponding reduction in characteristic impedance. While in most cases this local reduction in impedance will cause only minor disturbances if it occurs once or twice per signal line, a compensating local reduction in line width will preserve the characteristic impedance.

All power pins are decoupled inside the package with a capacitor of approximately 200 pf to the internal VSS supply except for VDDO which is internally decoupled to the VTTC pin.

III. PC BOARD MATERIALS

In the past, substrates have been fabricated from glass epoxy, polyimide, polystyrene, polyethelene, PTFE (polytetraflouroethylene), ceramic, and composites of the above materials. Each material has unique properties which have been capitalized upon by manufacturers to produce boards with the requisite mechanical and electrical properties. Recent advances have also been made in new materials for boards possessing outstanding characteristics at moderate cost. These materials, RO-2800 and

Rexolite are described in literature by Rogers[4] and Oak[5]. E. I. du Pont de Neumours and Co. has recently announced a new plastic material trademarked Arylon which appears to have properties well suited to GHz boards. Pertinent characteristics of a few materials and some of the commercially available laminates are given in Table 1.

TABLE 1

MATERIAL	DIELECTRIC CONSTANT	DISIPAT FACTOR	CTE (10^{-6}/°C)	TENSILE MOD
Glass Epxy	4.8[3]	0.022[3]	13-16	2.5
PTFE	2.1[4]	0.0004[4]	224	0.05
PTFE (μfiber)	2.2[4]	0.0008[4]	24	0.14
Polyimide Glass	4.5[3]	0.10[3]	12-14	2.8
RO2800[1]	2.8[4]	0.002[4]	8-11	0.14
Rexolite[2]	2.6[4]	0.002[4]		

Notes: All measurements except CTE at 25°C.
[1] Rogers Corp. See Ref 4.
[2] Oak. Rexolite 2200 . See Ref 5.
[3] @ 1MHz.
[4] @10 GHz

Glass Epoxy Considerations

Nearly all commercial and most military designs have heretofor employed glass epoxy as the board material for digital designs. Its low cost, ready availability and processing familiarity justify this selection for most low speed digital applications. It may be used with digital GaAs designs as well, although four factors must be considered before a decision is made to use it.

A. Propagation Delay

The dielectric constant of 4.8 restricts the propagation delay of microstrip to ~150 ps/inch and that of stripline to ~190 ps/inch. A board material with a lower dielectric constant will propagate the signal with less delay.

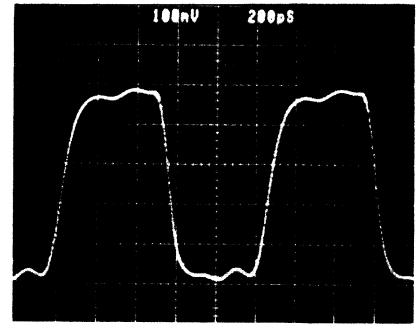
B. Increased Coupled Noise

The high dielectric constant of glass epoxy dictates that for a given trace width, the distance of the signal trace from the ground plane will be greater than for other materials to achieve a certain line impedance. Therefore adjacent traces on the same signal plane will have a larger portion of the switching energy coupled into them for the same inter-trace spacing. To maintain noise margin, the spacing between traces would necessarily be increased if the dielectric thickness and trace width may not be decreased.

C. Dielectric Losses

A microstrip line is not an ideal conductor due to three different types of losses. Two of these are associated with the conductor; the resistance which is present even at dc, and the skin effect which is a function of the frequency. The first is well understood and the second is generally negligable for the frequency and distances encountered, however the third component, that of dielectric loss, may not be. Glass epoxy becomes lossy at high frequencies, although not as lossy as some organic materials such as polyimide in the presence of moisture. The effect of this will be noted when a PicoLogic signal is propagated some distance on a board. Because the output slew rates are typically 5 -10 V/ns, the signal contains significant levels of odd harmonics beyond 5 GHz. Figure 1 is a photograph of the output of a 10G004 Quad 2:1 Multiplexer illustrating the rise and fall times for an output swing of 1.5 V p-p with the input driven from a 600 mV p-p sine wave at about 1 GHz.

FIGURE 1. Output Waveform of 10G004
(corrected vert. = 316mV/div.)



These higher order harmonics are attenuated proportional to the trace length. This effectively slows the rise and fall times at the receiving end of the line, thereby creating additional delay prior to the input reaching the threshold (-1.3v) of the receiving device.

Despite these speed-related shortcomings many designs employing PicoLogic IC's use glass epoxy as the laminate. High clock rates can be maintained when delays can be matched. Of course, poor rise and fall times degraded by losses in board material will be restored up to the limit of the output slew rate {(ΔVout/Δt)max} by the high frequency gain {(Av(f)} of each PicoLogic device thru which the signal propagates approximating the following rms summation:

$$(1) \quad (\Delta Vout/\Delta t)^2 \approx \{(\Delta Vin/\Delta t) \cdot Av(f)\}^2 + \{(\Delta Vout/\Delta t)max\}^2$$

This simplifies when well below the slew rate limit to

$$(2) \quad \Delta Vout/\Delta t) \approx (\Delta Vin/\Delta t).Av(f)$$

D. Effects of Thermal Mismatch

The fourth negative factor relates to glass epoxy's coefficient of thermal expansion (CTE). It is more than twice that of the ceramic packages (CTE of approximately

$6.5x10^{-6}$/°C). Since the best device electrical performance may be obtained with LCC packages, which lack compliant leads, thermal cycling can cause stress in the solder joint between the board and the package. However this is not a major problem for packages as small as GigaBit presently employes. If the board and the package are not manufactured from the same material, or materials with nearly equal CTE's, one of the following schemes should be employed to resolve this dilemma:

a. Design either the package or the board from a material with a low tensile modulus such as PTFE or RO-2800 which will stretch or compress when stressed.

b. Add leads to the package, such as the C40 or L36, so as to provide the required compliance.

c. Minimize package size so as to decrease stresses due to thermal cycling, thereby increasing the number of thermal cycles before failure.

d. Reduce the PCB's CTE through the use of an imbedded copper-clad Invar sandwich or a similar approach.

e. Provide a long tubular solder interconnection between the board and the component.

It can be demonstrated that the 40 pin LCC package can withstand between 2,000 and 5,000 thermal cycles between failures for 1 watt dissipation, assuming a 5 mil high eutectic solder joint and the 90GHS40A heat sink with a 600 LFM air flow. This is equivalent to from 8 to 20 years for equipment cycled daily (five times weekly) which is an extreme case. Most equipment employing GaAs will not be subject to such frequent cycling and many will employ cooling methods capable of limiting temperatures to a 10 or 20 degree range. Note that the high degree of elasticity of PTFE and similar substrates will result in a considerable improvement in the number of thermal cycles despite its extremely high CTE.

The presence of copper (possessing a CTE of 18.3) on the boards, especially multilayer boards where the power planes are nearly uninterrupted copper, will increase the CTE of the substrate material, and will reduce the temperature rise of the part due to the improved thermal conductivity of the completed board.

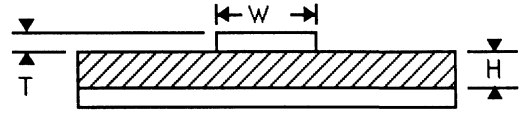
One factor which mitigates the differences in the thermal coefficient of expansion is the fact that the IC is the source of heat, hence it becomes hotter and reaches thermal equilibrium earlier after power is applied, somewhat offsetting its lower CTE. However if the power is turned off, but the blowers continue to operate, the ICs will cool significantly faster than the PC board, thus accentuating the stresses caused by differing CTE's. For this reason blowers should be cycled with DC power. A comprehensive discussion of thermal management is given in GigaBit application note 3[6].

IV. SIGNAL INTERCONNECTIONS

PC board design must utilize controlled impedance interconnect (customarily 50 Ohm) with all lines terminated in their characteristic impedance, otherwise signal overshoot and reflections may cause noise problems. Signal lines may be implemented with microstrip, stripline, dual stripline or wire over ground plane. Coaxial cable such as CoAxe[7] manufacturered by the Multiwire division of Kollmorgen Corp offers propagation delays down to 100 ps per inch with the expanded PTFE dielectric. Rectangular coax's are also available from Augat Microtec, which are formed by an additive process in a polyimide substrate.

For example a low trace density 50 Ω microstrip line on FR-4 glass epoxy with a dielectric constant of 4.8 might be determined to have the following dimensions: H =.010" (readily available), T =0.0007 (1/2 ounce copper),

Figure 2. Microstrip



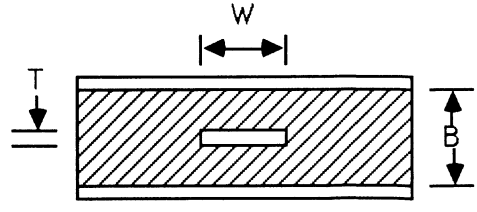
Characteristic Impedance:

$$Zo = (87/\sqrt{Er+1.41})\ \ln(5.98H/(.8W+T))$$

Propagation Delay:

$$Do = 1.016\sqrt{.475\,Er+.67}\ \text{ns/ft}$$

FIGURE 3. Stripline



$$Zo = (60/\sqrt{Er})\ \ln(4B/.67\pi(.8W+T))$$

$$Do = 1.016\sqrt{Er}\ \text{ns/ft}$$

FIGURES 2 & 3 provide the information necessary to calculate the trace dimensions for any given dielectric constant and thickness to achieve a specified impedance for microstrip and stripline respectively. The propagation delay may also be calculated. The general equation for characteristic impedance and intrinsic delay of any transmission line are given below:

(3) $Zo = \sqrt{(Lo/Co)}$

(4) $Do = \sqrt{(LoCo)}$

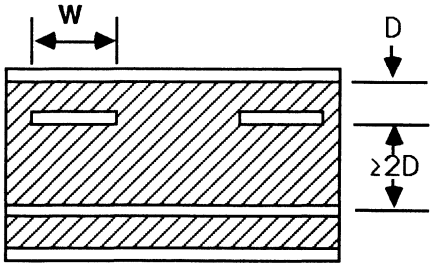
then the signal traces width (W) would be required to be 17 mils wide to maintain a 50Ω impedence. An alternate glass epoxy layout with increased trace density requirements might dictate a trace width (W) of 8 mils with a corresponding dielectric thickness of 5 mils.

In general the weight of copper used for signal traces should be 1/2 oz (0.0007) to permit the precision etching that is necessary to maintain impedances within ±10%. Conversly, power planes should use 1oz(0.0014") or 2oz(0.0028") copper to insure minimum inductance and resistance, and also provide improved thermal characteristics. The dimension T in microstrip (but not in stripline) boards will increase 0.5 to 2 mils as a result of copper plating for vias and will also increase due to solder plating if applicable. This thickness (T) can become an appreciable factor in the equation of a microstrip board of narrow trace widths (W).

Some of the prototyping and test boards made by GigaBit Logic have been gold plated, but this is employed to provide an interface for solderless sockets, and is unnecessary for performance. The skin effect is not significant for frequencies below 5GHz expecially for flat conductors such as strip line or microstrip which have a high ratio of effective conductive surface to cross sectional area.

It is possible to have two signal planes, a dual stripline, not separated by a power (A-C ground) plane if the two signal planes avoid parallel traces to minimize noise coupling between them. This can most readily be accommodated by using one plane for one axis of interconnection and a second plane as the orthogonal axis as illustrated in Figure 4. The distance between the signal planes and the trace densities on these dual striplines will influence the impedance discontunities as the two traces cross. Such discontinuities many be minimized by using narrow traces (typically <.010") seperated from the adjacent signal plane by twice the distance from the ground plane. Of course, the impedance in this case will fall between that for a stripline and microstrip.

FIGURE 4. DUAL STRIPLINE

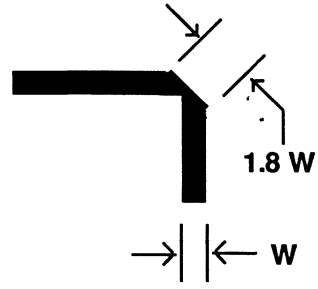


Avoiding Stubs

Output rise and fall times of GigaBit PicoLogic parts are typically 150 ps. Reflections from an unterminated stub will generally not be troublesome if the round trip propagation time from the signal source or point of termination to and from the stub is less than this rise or fall time. If this is the case, the primary reflection seen at the transmitting end occurs before the signal transition has completed. For a glass epoxy microstrip design, with a propagation delay of approximately 150 ps/in, this round trip must be less than 150ps, equivalent to a round trip propagation delay of 0.5 inch of trace. The round trip internal delay of the 36 and 40 pin packages is approximately 80ps, therefore stubs at the inputs greater than 0.25 inches (6 mm) must be avoided to prevent reflections from inputs. The 40 pin packages have sites for terminating which are much closer, and would permit slightly longer stubs on the board.

Generally, precise attention to detail must be observed when designing with picosecond transitions,

FIGURE 5. Cutting Corners



however there is an exception where cutting corners may be beneficial. An area similar to capacitive loading occurs during normal routing of signals. When a printed circuit trace makes a bend on the board its capacitance per unit length will be increased and its inductance per unit length will be decreased. This is especially true for sharp angles of 90° or more. It has been found that this effect may be compensated by cutting the corners as shown in Figure 5[8]. The 1.8 W factor shown is not critical; figures between 1.6 and 2.0 all have been employed. This modification should not be necessary in any but the most critical applications with 100-200 ps risetimes due to the very small reflections resulting from this capacitance.

V. MULTIPLE FANOUTS

Since all PicoLogic outputs can easily source 60 ma and the input currents are approximately 200μa, fanout will be

limited by a-c rather than d-c considerations. Four methods to increase fanout are parallel driving, use of multiple output buffer circuits such as the 10G010 or 10G011A, series termination, or daisy chaining, and are described below.

Parallel Drive

Each PicoLogic output is capable of driving two 50Ω terminations to -2v and achieving VOH>-0.8v and VOL <-1.8v thereby driving other PicoLogic devices at full rated speed. The output impedance ranges between 8 and 12 ohms to VDDO when the outputs are turned on (High).

Multiple Output Buffers

Two circuits are defined as dual fanout buffers: the 10G011A and the 10G010 with each half of each providing four outputs in parallel. They differ only in input structure with the 10G010 offering multiplexed inputs or differential inputs (with the obvious option of logical inversion), and the 10G011A offering a fixed logic function.

Series Termination

The third option is that of using series (source) termination instead of shunt termination. This is illustrated in the accompanying **Figure 6**. Note that the termination resistor is located at the source and the receiving end of the line is unterminated. The value of the termination resistance at the source (Rs), when added to the output impedance of the PicoLogic device (Ro = 8Ω) should equal the characteristic impedance of the line (Zo). Operation in this fashion causes the voltage swing at the junction of the transmission line and Rs to be half amplitude due to the resistor divider action. When the signal reaches the terminus of the line which is unterminated the reflection coefficient of 1 causes the amplitude to be doubled and reflected back along the line. The zero reflection coefficient at the source will absorb all reflected energy at this point and limit further reflections. Note that at any intermediate point on the line the signal will only reach half amplitude until the reflected wave reaches this point on the line. For this reason daisy chaining on this line is not possible, although two inputs could be driven from a line if they are located within 0.4" of one another.

The user must insure that the pulldown resistor Rpd to VEE is sufficiently small to supply the current necessary to cause the half amplitude swing (700mv) across Zo as described above. The derivation of Rpd for a single line follows:

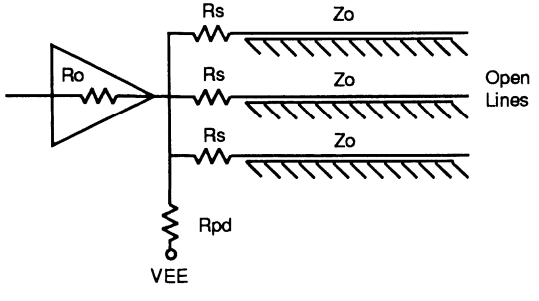
$$Ipd = 0.7v/Zo = (Voh-VEE)/(Rpd+Rs+Zo)$$

letting Voh = -0.5v and VEE = -5.2v solve for Rpd

$$Rpd \leq 5.7Zo - Rs$$

In the 50 Ω case this results in a maximum value for Rpd of 245Ω when driving a single line. When driving N lines this value should be divided by N. A fanout limit of 3 will be imposed by the IOH maximum of the picologic devices.

Figure 6: Source Termination

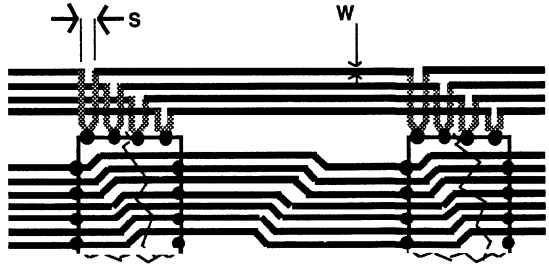


Series or source termination is desirable when driving a backplane or other situations where impedance discontinuities cause multiple reflections. All reflections are absorbed at the source.

Daisy Chaining

Daisy chaining is a technique for interconnecting logic signals, which is only suitable for shunt terminated lines. **Figure 7** illustrates the schemes for interconnecting multiple ICs on a single line as described below.

FIGURE 7. P.C. Board Daisy Chaining



A signal may be tapped into a multiplicity of inputs as it propagates along a trace, and be terminated once only at the end of the trace. This can readily be achieved for board designs that horizontally connect the vertical pads of parts, by traces on any layer which contact the component through the use of vias. However, when horizontal interconnection of horizontal pins must be accomplished, the task is more difficult and will generally result in a longer electrical path, skewing the data with respect to that of the vertical pins. It should be noted that the the trace makes a U to connect to the pin. This avoids the stubs, providing adequate space S is used to assure mutual coupling does not introduce discontinuities. If S can be maintained at twice the distance H above the ground plane, coupling will be minimal. In the general case, delays must be accounted for and additional delays can be provided on the board either by controlling which trace is buried, (remem-

ber, strip line delays are longer than microstrip delays) or by adding trace length with meandering or zig-zag lines. Random logic will generally require the use of more than only the top and bottom layers for signal interconnection in order to compress the design into the smallest possible area. A more detailed discussion of the capacitive effects due to daisy chaining follows.

VI. STRAY CAPACITANCE EFFECTS

When dealing with daisy chained inputs it must be recognized that the waveforms will be degraded due to input capacitance. Most PicoLogic parts have > 1.5 pf input capacitance including the package capacitance, however some parts may have capacitance up to 5 pf on clock and master reset lines. Since the pad on the board itself will generally be wider than the 50 Ω trace width, it will appear capacitive. For the following computations we shall consider each input equivalent to 1pf. Since in a daisy chain these inputs are distributed along the transmission line a distributed capacitance model serves better than a lumped model. This input capacitance will have the effect of reducing the impedance of the line and increasing its propagation delay. The effect on both propagation delay and characteristic impedance may be determined by adding the package capacitance C_s to the intrinsic C_o of the transmission line and recalculating .

The propagation velocity in any uniform dielectric media may be found from the following equation. $Vo = c/\sqrt{e}$; where c is the speed of light in a vacuum ($3*10^8$m/sec) and e is the relative dielectric constant. Recalling the general equations (3), (4) for the intrinsic impedance and delay applicable to any transmission line: $Z_o = \sqrt{(L_o/C_o}$ and $D_o = \sqrt{(L_oC_o)}$. For glass epoxy microstrip, assuming a relative dielectric constant of 4.8, Do, the intrinsic delay equals 150 ps/in. for all characteristic impedance values. Note that this delay differs from that which would be calculated from the above equation since microstrip has air as a dielectric on one side thereby effectively lowering the relative dielectric constant. The values of C_o and L_o, the line intrinsic capacitance and inducance per unit length, are given in Table 2 for impedances of 50, 75 and 100 Ω.

TABLE 2- Glass Epoxy Microstrip

Z_o Ohms	C_o pf/in	L_o µH/in
50	3	0.0075
75	2	0.01125
100	1.5	0.015

Note that C_o can be determined for any material by solving equation (3) for C_o resulting in the equation $C_o = D_o/Z_o$.

We shall now determine the influence of this stray package capacitance C_s, on the delay and impedance of the line. If we assume a daisy chain with one device per inch, and we assume a 50Ω line then the C_o will be increased by the1.5 pf C_s, from 3 to 4.5 pf/in. We may now derive new equations from equation (3) and (4) for the loaded impedance (Z_L)and the loaded delay (D_L)by adding this stray capacitance C_s as follows:

$$(5) \quad Z_L = \sqrt{\{L_o/(C_o+C_s/d)\}}$$
$$(6) \quad D_L = Z_o^2(C_s/d)/(L_o-Z_o^2C_o)$$

Then $Z_L = \sqrt{(L_o/(C_o+C_s))} = 40.8\Omega$. The propagation delay will likewise be increased per the equation $DL = \sqrt{\{(L_o(C_o+C_s)\}} = 184$ps/in. This is somewhat idealized since the capacity will also appear as a lumped constant to a degree, therefore degrading the rise and fall times.

It should be noted that PicoLogic output capacitance is similar, hence the analysis for bus driving/wire-oring, where several outputs are on a common line, would be comparable. Calculation of the influence of capacitive loading on lines with higher Z_o shows that the influence on both delay and Z_o is more pronounced for a given capacity. Although lower impedance lines dissipate more power this factor results in improved performance, especially at GHz speeds.

A method to minimize the effect of the additional capacitance caused by the device is to reduce the line width in the vicinity of the pins such that the narrower line over this length has a higher impedance than Z_o. When the effect of the device capacitance is added to this higher impedance line, the resulting reduction in impedance would equal the desired Z_o. The length over which the higher impedance line must extend may be derived from equation 5 by setting $Z_L = Z_o$ where d = distance of higher impedance line, and C_s = package capacitance. Solving for d yields:

$$(7) \quad d = Z_o^2C_s/(L_o-Z_o^2C_o)$$

It may be seen from Table 2 that for a $Z_o = 75\Omega$, C_o is only 2pf/inch compared to 3pf/inch for 50Ω, and L_o is 0.0125 µH instead of 0.0075 µH/in for 50 Ω. Solving equation 7) for 75Ω microstrip yields d = 0.40", and for 100Ω microstrip d = 0.22". It is desirable to minimize the length of this higher impedance line localizing it to the immediate vicinity of the C_s. The 100Ω microstrip line would appear a better choice, however the limiting factor will be the linewidth which can be fabricated. Tapering the line at this transition is guilding the lilly, somewhat similar to cutting the corners mentioned earlier.

VII. UNUSED INPUTS AND OUTPUTS

In many cases inputs will not be driven from a logical source, but instead must be established at a fixed logical low or logical high. These pins must not be left open, but should be tied to either the VDDL or VDDO supply for a high, or should be tied to VSS or VTT for a logical low (with

the former preferred in each case). Note that this contrasts with ECL which always provides an input pull down resistor to VEE which will cause unconnected inputs to default to the low state. ECL inputs should not be tied directly to the positive rail; the excessive high level may cause saturation of the input stage, and anomolous behaviour.

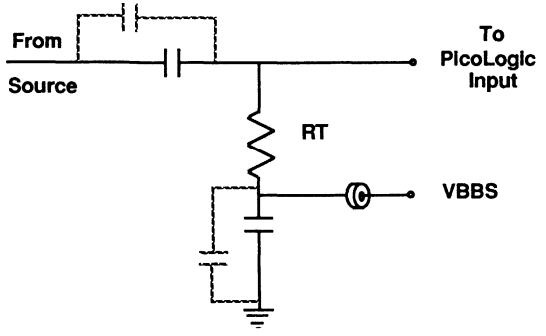
The VBB inputs should not be left open, but should rather be connected to the internally supplied VBBS when driven from Picologic devices, or connected to the VBB supply of the driving ECL family. This causes Picologic 's threshold to track that of the driving family if necessary. The internal VBBS supply is nominally -1.3 volts, however it is designed to have a temperature coefficient of +0.6 mv/°C, midway between 100K, which is flat, and 10K.

Unused outputs should be left open (unterminated) to conserve power. The maximum power reduction may be achieved by setting the inputs to that state which will force the unterminated output high. Only the 10G012 family provides seperate power pins for each half of the chip to permit powering down of the circuit. Note that the 10G012A's VBBS supply is derived from the "A" side of the circuit, hence that side must be powered if VBBS is required.

VIII. A-C COUPLING

Occasionally signals such as those derived from VCO's or other oscillators, or even Manchester or other encoded data streams will not be biased around -1.3 volt thresholds, but will lack any dc component in the data itself. In order to use these signals they must either be ac coupled or dc shifted by means of resistor networks. Level shifting through the use of resistor networks has been previously discussed[9]. Capacative coupling is possible, as illustrated in **Figure 8**, only if the signal has no dc component unless dc resoration is employed. RZ or unencoded NRZ are examples of data which contain a dc component and could not be ac coupled without d-c restoration.

FIGURE 8. A-C Input Coupling



When ac coupling, the input signal must be coupled via a capacitor which has an impedance << 50Ω for both the lowest and highest frequency components of the data stream. Since large capacitors may become inductive at high frequencies, parallelling a large and small capacitor may be essential. Obviously parallel resonance should be avoided. The termination resistor is then terminated to VBBS, with adequate decoupling capacitance (impedance << 50Ω) at the bottom of the termination resistor to prevent introducing noise into VBBS and also to assure that the resistor appears with negligable reactive component. A resistor or ferrite bead may also be used as shown on the diagram to further block any remaining ac from entering the VBBS supply of the chip.

TABLE 3

PicoLogic / NanoRAM FAMILY POWER SUPPLY SPECIFICATIONS

	MINIMUM	NOMINAL	MAXIMUM
Vss	- 3.5 Volts	- 3.4	- 3.3
Vee	- 5.5	- 5.2	- 5.1
Vtt	- 3.5	- 2.0	- 2.0

Vddo and Vddl are equal to zero Volts (GND).

IX. POWER SUPPLY INTERCONNECTIONS

Table 3 is a table of the power supplies which must be provided to the PicoLogic family to assure that the devices will be ECL input level compatible. Most PicoLogic devices can tolerate ±5% deviation on VSS and VEE over the full temperature range specified, however, some devices require the tighter tolerance given in Table 3 to assure proper input thresholds and sufficient margins for ECL compatibility.

VSS Supply

Were it not for the threshold stabilizing effects of VTRIM or VBB described elsewhere[10,11], the input thresholds of PicoLogic would be directly affected by VSS (i.e.ΔVth/ΔVSS ≈ 1). Thus a 100 mv change in VSS would result in a 100 mv change in Vth. However, this equation applies only for the first generation of PicoLogic parts having VTRIM not connected for ECL tracking. If VTRIM is connected as recommended or second generation PicoLogic devices employing VBB are considered, the effect of changing VSS on Vth is greatly reduced (ΔVth/ΔVSS

≈0.085) as long as the range over which the VBB (or VTRIM) circuit operates is not exceeded. This region is quite limited when process variables and temperature extremes are considered, imposing the ± 100 mv tolerance on VSS for the family. Recent improvements in VBB feedback indicate that this operating range exceeds ±5% on VSS and a one volt range on VBB.

To insure that VSS is maintained for all devices in the system, it is essential that stable power sources and a low resistance, remote sensing, VSS supply should be set to -3.4 volts under normal conditions referencing the most positive voltage point in the system.

VEE Supply

It should be noted that the major constraint on VEE is the necessity to maintain a minimum differential between VSS and VEE (VSS - VEE≥ 1.6 V). Therefore, it is desirable to maximize (in the absolute sense) VEE. For this reason, power supply distribution should feed the VEE supply to the PicoLogic devices before supplying ECL devices in the same system. If remote sensing of power supplies is employed, the sense point need not be located within the PicoLogic area since a more negative VEE will have no adverse effects, and since IEE<< ISS, the power increase will be minimal even if VEE approaches - 5.5 V.

VCC Supply

A positive power supply of +5 V is required for some GaAs circuits introduced by GigaBit. The 12G014 Pipelined RAM and the 16G040 Clock and Data Recovery Circuit are the most prominent examples of these. The +5 V required should be maintained within ±250 mv. This will assure proper performance at minimum power dissipation.

Power Supply Sequencing

Although Power supply sequencing is not essential, some caution must be exercised if the VSS supply is not derived from the VEE supply. Since the transistors are depletion mode devices all transistors will be conducting if VSS is on without benefit of the reverse bias provided by VEE, and power dissipation will increase. An even more onerous problem arises if the VEE supply is held at ground potential, such as might occur if a significant number of ECL devices provides a heavy load from VEE to VDD or if a several thousand microfarad capacitor appears on the output of the VEE regulator to ground. In this case the internal capacitance between VSS and VEE, comprised of junction diodes as described in the next section, will become forward biased and may conduct sufficient current so as to damage the parts. For this reason, if there is a possiblity of VEE being held at ground while VSS is set at -3.4volts, it is essential to provide a Silicon power diode between VSS and VEE. A 100μf electrolytic capacitor should be placed in parallel with this diode to prevent occurence of a spike during the forward recovery time of this diode.

Use of Power Planes

Due to high switching currents evident in all high speed logic, the primary power supplies must be distributed on a power plane to reduce the dynamic impedance of these supplies. Any part which causes its power source to droop during switching will have a reduced speed as a result of this "soft" supply. Likewise any power switching transient caused by one device may adversly affect the input threshold or speed of all other devices supplied by this common source. This is particularly true of transients on VSS, the AC reference of PicoLogic parts.

For this reason every effort should be made to stabilize all power supplies from transients. This may be accomplished by including internal and external decoupling (to be discussed in section X) and by use of power planes instead of power buses. Power planes have much lower dynamic impedance than power buses, hence providing the "solid" supply required for best operation. Calculation of resistance and DC currents may lead designers into a false sense of security. Power buses typically have dynamic impedance in the range of five Ohms, depending on dielectric constant and thickness of the board, trace width, thickness and proximity to and density of other DC planes. It is therefore recommended that all PicoLogic PC boards have the following power planes:

VSS (- 3.4 V)
VDD (for both VDDL and VDDO)
VTT (- 2 V)

VEE (- 5.2 V) may be supplied as a bus on a signal plane in some cases, since both the dc and transient currents are relatively low, and the parts are tolerant of noise on VEE. Obviously, if the board is co-populated with ECL, VEE must also be supplied via a dedicated power plane.

X. HIGH FREQUENCY DECOUPLING REQUIREMENTS

The following discussion should assist the reader in understanding those factors which are unique to PicoLogic IC's.

Internal Logic Decoupling

The majority of the internal current flow for the logic is between VDDL and VSS supplies. The purpose of decoupling is twofold. The first is to maintain the supplies even under transient conditions so the logic can consume the charge required during switching. Any collapse of supplies will result in an increase in internal delays and transition times. Therefore it is necessary to maximize the decoupling between VSS and VDDL. This may be best accomplished by decoupling all VDDL pins to the VSS plane, and decoupling all VSS pins to the VDD plane as close as possible to the pins.

The output source follower current flows between the VDDO pin to the output pin which is normally terminated

at the end of a transmission line in 50Ω to VTT = -2 volts. Since the return path is via the VTT plane, the VDDO pin should be decoupled to the VTT plane and the VTT pin should be decoupled to the VDDO plane.

The VBB pin provides tracking of ECL thresholds and as such is a signal input. Although it is implemented in two different fashions[10], having somewhat different characteristics, the decoupling philosophy can be identical. The differential VBB approach provides an input which will respond to high frequency signals, whereas the VBB feedback approach has an internal low pass filter. Since the signal and the return path (coax shield or VTT plane in most cases) may possess common mode noise, minimization of this common mode noise can be attained if the VBB pin is decoupled to the VTT plane.

Good high frequency (low inductance) chip capacitors should be soldered as close as possible (less than 0.2" (5mm)) to the package between relevant signal or power traces and the appropriate power planes. The value of the capacitor may be determined by the required charge which must be supplied during the switching current transient as follows:

(8) $C \geq I\ (\Delta t/\Delta v)$

where I for this example is assumed to be the IDDO transient current e.g. 8 outputs driving 50 Ω to -2v having a VOH=-0.5 and VOL=-2.0

$I=8(2.0v-0.5v)/50 = 240ma.$

Δt is the transition time during which the capacitor must store the charge .

$\Delta t = 200ps$

Δv is the permissible noise voltage induced as a result of the transient.

$\Delta v \leq 50$ mv

$C \geq 0.24\ (0.2 \times 10^{-9})/0.05 = 0.96 \times 10^{-9}$ or 960 pf.

Therefore 1000pf chip caps should be used to decouple VDDO to VTT and VSS to VDDL. Since IEE currents are typically an order of magnitude lower than ISS currents, a 100pf capacitor should suffice between VDDL and VEE. VBB inputs should also have an external supplemental 100 pf capacitor to the VTT plane as close as possible to the point to which the input lines are terminated.

All GigaBit packages contain integral decoupling capacitors on all power pins in the 200pf to 400pf range to provide bypassing as close to the die as possible. These are implemented either with interdigitated reverse biased p-n junction diodes in the case where a silicon substrate is employed or as ceramic chip caps in the case of the 36 I/O LCC. Due to the use of the junction capacitors, the polarity of the power pins must be observed. This is not normally an issue except for the the VTTC pin which is internally decoupled to the VDDO pin. If output inversion or TTL output levels are configured by the user, or the signal is derived from the VDDO pin, the VTTC pin should be tied to the VDDO pin instead of connecting it to VTT = -2V.

Additionally the 40 pin packages provide a VTT ring at the top of the package to facilitate decoupling all supplies to this potential. Although it might not seem appropriate to decouple VSS and VDDL pins to the VTT ring based on the previous discussions, it is permissable if the VTT power plane is adequately bypassed to the VDD and VSS planes with resultant noise levels below 50mv p-p. It is obviously the ideal decoupling point for the VDDO supply.

In addition to local decoupling at each site, it is also essential as with any electronics board to provide some low frequency decoupling at the power entry point of the board. These values must be determined as a function of the total board current.

XI. SOLDERING & REMOVAL OF LCC PACKAGES

NOTE: The small geometries and low capacities inherent in high speed devices act to increase sensitivity to electrostatic discharge. At present, all GigaBit ICs utilize 1.0 micron channel length MESFETs. Therefore, handling and soldering precautions similar to those observed with ECL or CMOS devices should be followed.

Leadless Chip Carriers are superior packages for the high speed GHz digital signals encountered with GaAs technology. However they are not in widespread use today, hence a brief description of board assembly in the prototype lab is appropriate. Due to the extensive information available on production assembly techniques for LCC's these discussions will be limited.

LCC packages are generally soldered using solder paste and vapor phase reflow, hot air, or infrared techniques for production. Since the lid sealing profile subjects the package to 300°C for 3-4 minutes, conventional reflow techniques at ≈220°C will cause no difficulties. Since the leads are gold they should be pretinned for most reliable connection. In accordance with standard practice, parts should be preheated to 100°C for at least 30 seconds to minimize thermal shock. Manual attachment using a soldering iron with controlled temperature between 550 and 625°F is also possible for limited production quantities using standard 63/37 solder. This solder may also be used for soldering the chip resistors and capacitors to the top of the package. Johanson R09 capacitors and Minisystems WA47 resistors have been found acceptable.

Desoldering the GigaBit LCC packages require that all contact pads be simultaneously heated for proper removal. This section provides the user with proven successful techniques for manual LCC attachment and removal. Flat pack attachment and removal is not discussed here since this is a better understood process.

Manual LCC and C-Lead Attachment

1. Place the board on a grounded work station and ground the operator with an appropriate wrist or ankle strap.
2. Apply a thin layer of resin flux on the PC board footprint to be soldered.
3. Place the LCC on the flux coated footprint and visually align all four sides.
4. Holding the part in position with one finger, apply a temperature controlled (550 deg.F to 625 deg.F) fine tip soldering iron and a small amount of 63/37 resin core solder to one corner until the solder flows between the LCC and the board (approx. 1 second).
5. Tack down the opposite corner using the same procedure.
6. Feed solder and the iron tip along all four sides of the package and its interface with the board as fast as the solder will flow (one to two seconds per side). Visually verify and touch up as needed.
7. Remove any excess solder and clean the board using an appropriate solvent.
8. Inspect the assembly for a clean fillet and the absence of any solder bridging.

NOTE: this operation is particularly successful if tinned pads on the board extend at least 1mm beyond the edge of the component. This permits excess solder to gather on the opposite side of the iron from the IC. If the solder mask extends too close to the edge of the component, the remaining pad length will not be sufficient to contain excess solder, and the probability of trace bridging will be increased.

Manual LCC and C-Lead Removal

1. Place the board on a grounded work station and ground the operator with a wrist or ankle strap.
2. Apply a thin layer of resin flux around the perimeter of the part to be removed.
3. Preheat the removal tool for approx. 10 minutes. A suitable removal tool (one that is capable of contacting and heating all four sides of the LCC simultaneously) is available from: NU Concept Computer Systems Inc., Route 309 and Advance Lane, Colmar PA 18915 (215 822-8400).
4. Grasp the LCC with the preheated removal tool for approximately 2 seconds applying a gentle twisting motion to ascertain when the solder has liquefied.
5. When loose, immediately lift the part and place it on a work surface to cool.
6. Examine the board for any lifted pads and repair them as necessary.
7. Remove excess solder and clean the board to remove flux and debris with an appropriate solvent.

NOTE: the entire operation should require less than 5 seconds when properly performed. Either premature removal force, or delay in removing the device, may result in lifted pads.

Package Attachment Information

Package leads are Alloy 42 plated with 1.5µ, 99.9% gold over a nickel undercoat. Thermal vias in the 36 I/O LCC are plated with tungsten. None of the package materials or bond wire will melt under normal SMD soldering temperatures. However, because of circuit considerations, the entire package should not be subject to a temperature above 250°C for more than 1 hour.

For vapor phase reflow soldering using FC-70, the user must specify and procure solder sealed ICs from GigaBit. Epoxy sealed packages cannot withstand vapor phase assembly temperatures.

Solder sealed packages may be cleaned in an ultrasonic bath for not more than about 90 seconds or the package marking may by removed. Bond wires will not be damaged by ultrasonic cleaning.

If devices are to be stored for 12 months or more, the user should specify and procure packages with solder dipped leads. Leadless packages will withstand long periods of storage if kept in a dehumidified cabinet with dry nitrogen flow.

XII. DIE APPLICATIONS IN HYBRID DESIGNS

To realize the full performance of GaAs SSI and MSI components die may be interconnected on a ceramic substrate to create a hybrid. A hybrid design has the advantage of providing minimum lead lengths which translates into lower inter-connect delays and thus, higher performance. Beryllia will provide better thermal conductivity than alumina, but both provide an excellent match to the CTE of GaAs.

All of GigaBit Logic's components are available in die form and their assembly into a hybrid differs little from that of silicon die. Reference should be made to literature in building hybrids[12,13]. The physical differences are enumerated below:

a) GaAs is much more brittle than Si; (requiring more delicate handling)
b) To reduce breakage the die are thicker than Si (PicoLogic die are nominally 25 mils);
c) The CTE is greater for GaAs than for Si more nearly matching ceramics as illustrated in the following table:

Properties	Substrates Al_2O_3	BeO	Si	GaAs
Thermal Conductivity (W/m-K)	20	260	149	45
Thermal Exp. Coefficient (x 10^{-6}/°C)	6.7	7.5	3.8	6.8

d) All die metalization is gold
e) GaAs should not be exposed to temperatures greater than 270°C.

Due to the physical differences between GaAs and Si the following precautions should be taken when assembling hybrids:

a) Reduce pressure on wire bonding. Thermocompression or thermosonic may be used but at lower pressure than that used for Si.
b) Set the height of the bonding equip for the thickness of the GaAs die.
c) Use gold bond wires.
d) Limit high temperature die attach or package sealing approaches.

XIII SUMMARY

Designing with GaAs is similar to designing with ECL. The component location and orientation on the board should be carefully assigned to facilitate high frequency wiring, maintaining equivalent signal lengths where necessary. The wiring delay should be considered when calculating timing diagrams. Each of the power supplies should be provided on a plane, with the possible exception of VEE and VBB (the reference supply). These supplies have very small transient currents and may be provided on a grid basis or wired from the power bus to each of the chips rather than being daisy chained. This contrasts with the signal lines which should be daisy chained from point to point and terminated at the end point with a terminating resistor. As with ECL, Picologic I.C.'s are designed to drive transmission lines.

Chip resistors and capacitors act as a catalyst in achieving the gigabit speed potential of the parts. These components should be soldered as close as possible (<0.2 ") from the pin as follows:

A capacitor should be soldered between every used VDDL trace and the VSS plane

A capacitor should be soldered between every VEE trace and the VSS or VDD plane.

A capacitor should be soldered between every used VDDO trace and VTT plane.

A capacitor should be soldered between every VSS trace and the VDD plane.

Chip resistors must be soldered as closely as possible to the final terminus of the transmission line. If more than one driver is on a bus, the bus must be terminated at each end.

Despite close adherence to these cookbook rules, decoupling may prove inadequate. If performance is degraded beyond that which is expected, monitoring the power supply pins with a sampling scope will help to isolate decoupling problems. Empirical solutions may be required due to the high frequencies involved.

XIV APPENDIX

Operation at these frequencies will transport many digital designers into the rf domain for the first time. In an effort to ease this transition, a brief table is provided which permits the conversion from dBm (referenced to 1mw) in a 50 ohm terminated system to volts peak to peak. This peak to peak conversion assumes a sine wave, which is a good approximation at the highest frequencies passed by PicoLogic devices. At lower frequencies the waveforms will approach square waves hence the peak to peak amplitude will be less. This table provides peak to peak amplitudes for each case.

dBm	V(rms)	V(p-p) (sine wave)	V(p-p) (square wave)
+20	2.25	6.37	4.50
+13	1.00	2.8	2.0
+10	0.71	2.01	1.42
+9	0.64	1.81	1.28
+8	0.58	1.64	1.16
+7	0.50	1.41	1.00
+4	0.36	1.00	0.71
+3	0.32	0.90	0.64
+1	0.25	0.71	0.50
0	0.23	0.64	0.45
-1	0.20	0.57	0.40
-3	0.16	0.45	0.32
-6	0.12	0.33	0.23
-12	0.058	0.16	0.116
-16	0.036	0.10	0.07

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Thermal Management of PicoLogic™ and NanoRam™ GaAs Digital IC Families

Application Note #3

I. INTRODUCTION

Thermal management of integrated circuits is neccessary in order to ensure long-term device and system reliability and performance. The goals of thermal management are two-fold: to keep individual transistor junction temperatures as low as possible (to maximize device reliability) and to keep device operating temperatures as uniform as possible across the entire system which they comprise (to minimize parametric variations).

Low junction temperatures insure optimum device reliability. MTBFs (Mean Time Between Failures) of greater than 100,000 hours for GaAs ICs can be realized if junction temperatures are maintained at or below 125°C. Junction temperatures lower than this will result in increased reliability while higher temperatures will degrade reliability. This is described by the well known Arrhenius equation and is shown graphically in **Figure 1-a** for an activation energy of 1.4 eV, typical for GaAs ICs. **Figure 1-b** shows FIT (failure unit) rates as a function of temperature. From Figure 1 it is seen that a device operated at 100 °C junction temperature would have an MTBF ten times as great as the 125 °C MTBF. Actual device operating temperatures must be fixed by the system designer after considering such factors as system complexity (i.e., number of devices) and required reliability levels. Reliability of PicoLogic™ ICs is discussed extensively in reference [1].

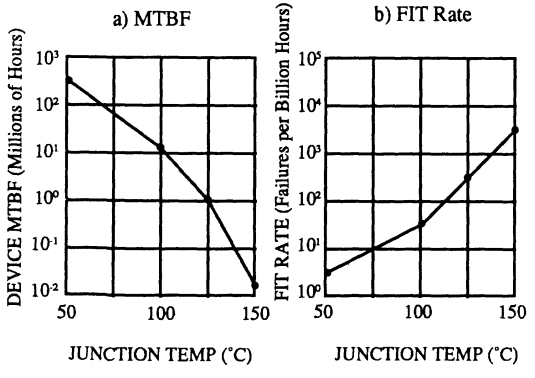


FIGURE 1: Approximate Device MTBF and FIT Rate vs Junction Temperature for a 1.4 ev Activation Energy

Thermal characteristics of GaAs ICs are similar to those of silicon bipolar ECL ICs. The thermal conductivity of GaAs is low (approximately 1/3 to 1/5 that of silicon, depending on temperature—see **Table 1.**) Board level packing density (and hence power density) will typically be higher for digital GaAs systems to preserve the short propagation delays of the ICs. Despite these minor differences, the thermal management techniques required for GaAs ICs are no different than those required for surface-mount silicon bipolar devices.

This application note provides the information neccessary for the proper thermal management of GigaBit Logic's families of GaAs ICs. **Section II** contains the thermal characteristics of GigaBit Logic devices and packages. **Section III** provides some background on heat transfer, which is needed to describe the thermal path from package to environment. Sample thermal calculations are performed in **Section IV**, based on the data presented in Sections II and III. For those interested in a quick estimate of their thermal management requirements, a simple 4-step method is listed in **Section V**, along with a summary. **Appendix A** provides some technical details on thermal resistance calculations and measurements which may be useful for hybrid thermal design and management and of transient thermal characteristics.

Table 1 lists some material and thermodynamic properties of air and packaging materials which will be used in this report.

TABLE 1: MATERIAL PROPERTIES

Thermodynamics Properties of Air at 100°C

Specific heat (Cp)	0.941	W/sec g °C
Kinematic viscosity (μ)	0.000219	g/sec cm
Thermal conductivity (k)	0.000277	W/cm °C
Density (ρ)	0.0011	g/cm 3

Thermodynamic Properties of Common Packaging Materials at 100°C

	Thermal Conductivity (W/cm °C)	Coefficient of Thermal Expansion (10^{-6}/°C)	Specific Heat (W/sec g °C)
Aluminum	2.35	25	0.90
Ceramic (alumina)	0.20	6.5	0.84
Ceramic (beryllia)	2.20	8.0	1.09
Copper	3.90	18.3	0.39
Epoxy (silver filled)	0.02 to 0.06	40-50	0.24
GaAs	0.35	6.9	0.35
Glass	0.003	12-16	0.80 (est)
Kovar	0.20	5.8	0.44
Silicon	1.10	2.6	0.70

II. THERMAL RESISTANCES

Junction temperatures of GaAs ICs can be related to device

power dissipation by the following approximate relationship:

$$T_J = T_A + 10°C + (\theta_{SC} + \theta_{CA}) P_D \quad (1)$$

$$= T_A + 10°C + \theta_{SA} \times P_D$$

where :

T_J = maximum junction temperature (°C)
T_A = maximum ambient temperature (°C)
P_D = maximum device power dissipation (W)
θ_{SC} = ave. die surface to case thermal resistance (°C/W)
θ_{CA} = ave. case to ambient thermal resistance (°C/W)
θ_{SA} = ave. die surface to ambient thermal resistance (°C/W)

Die surface temperature is essentially equivalent to $T_{j(region)}$. The 10°C factor represents the temperature differential between T_j and $T_{j(region)}$, which is typically not a function of overall circuit power dissipation. The surface to case thermal resistance is determined largely by package design whereas the case to ambient thermal resistance is dominated by system-level considerations.

Thermal resistances can be treated as analogous to electrical resistances, with local temperatures and power dissipation as the counterparts to nodal voltages and currents, respectively. This is shown in **Figure 2**. Parallel and series networks of thermal resistances are calculated just as electrical resistive networks would be.

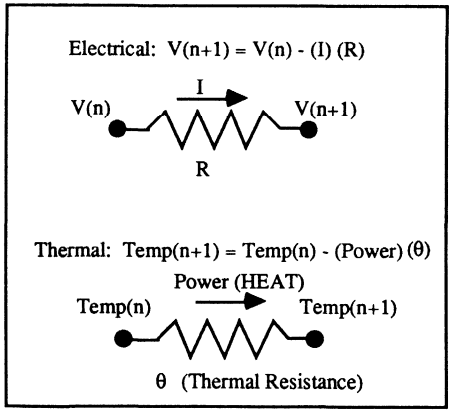


FIGURE 2: Electrical and Thermal Resistances

Package Types and Construction

GigaBit Logic assembles GaAs ICs in four primary package types: 36 and 40 I/O ceramic leadless chip carriers (referred to as L-36 and L-40 in this report), 36 lead glass/metal flatpacks (referred to here as F-36), and 40 lead ceramic "C"-leaded chip carriers (referred to as C-40). Cross-sectional views for these packages are shown in **Figure 3**. Mechanical drawings are shown in **Figure 4**.

The L-36 package is a multi-layer, co-fired, **cavity-up** ceramic package with integral chip capacitors for power supply decoupling and 50 Ω micro-strip transmission lines. The GaAs die is attached to the ceramic chip carrier, which has tungsten-filled thermal vias from the die-attach cavity to the package bottom. Note that these thermal vias (see Figure 4) should be connected to the VSS plane in the printed circuit board. This package is discussed in detail in reference [2]. Although there are actually 40 pads on the bottom of this package, the corner pads are not utilized, and hence it is referred to as a 36 I/O package. The F-36 package is a standard glass sidewall flatpack. To customize the package for gigahertz-rate operation, the GaAs die is mounted on a silicon IC which in turn is mounted in the flatpack . The silicon IC contains decoupling capacitors and 50 coplanar transmission lines [3]. Because of its low thermal resistivity relative to both ceramic and GaAs, the silicon acts as a heat spreader. The flatpack is mountable in either cavity-up or cavity down configurations. The L-40 package is a multi-layer, co-fired **cavity down** ceramic chip carrier which also utilizes the silicon substrate. The C-40 is a leaded version of the L-40 package. Because of their similar thermal characteristics, this application note will not, in general differentiate between the L-40 and C-40 packages. [Note: cavity-up and cavity-down refers to configurations where the die is attached to the package bottom and top surfaces, respectively.]

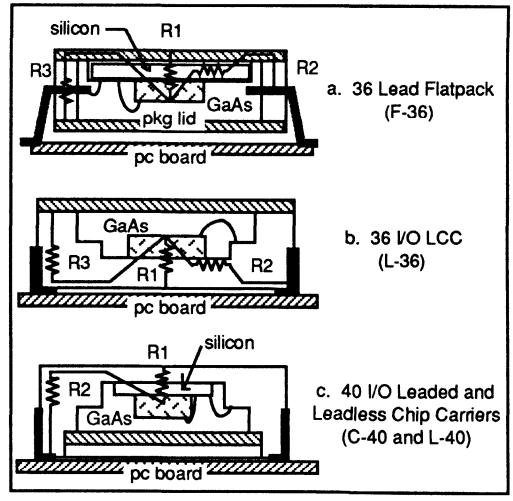
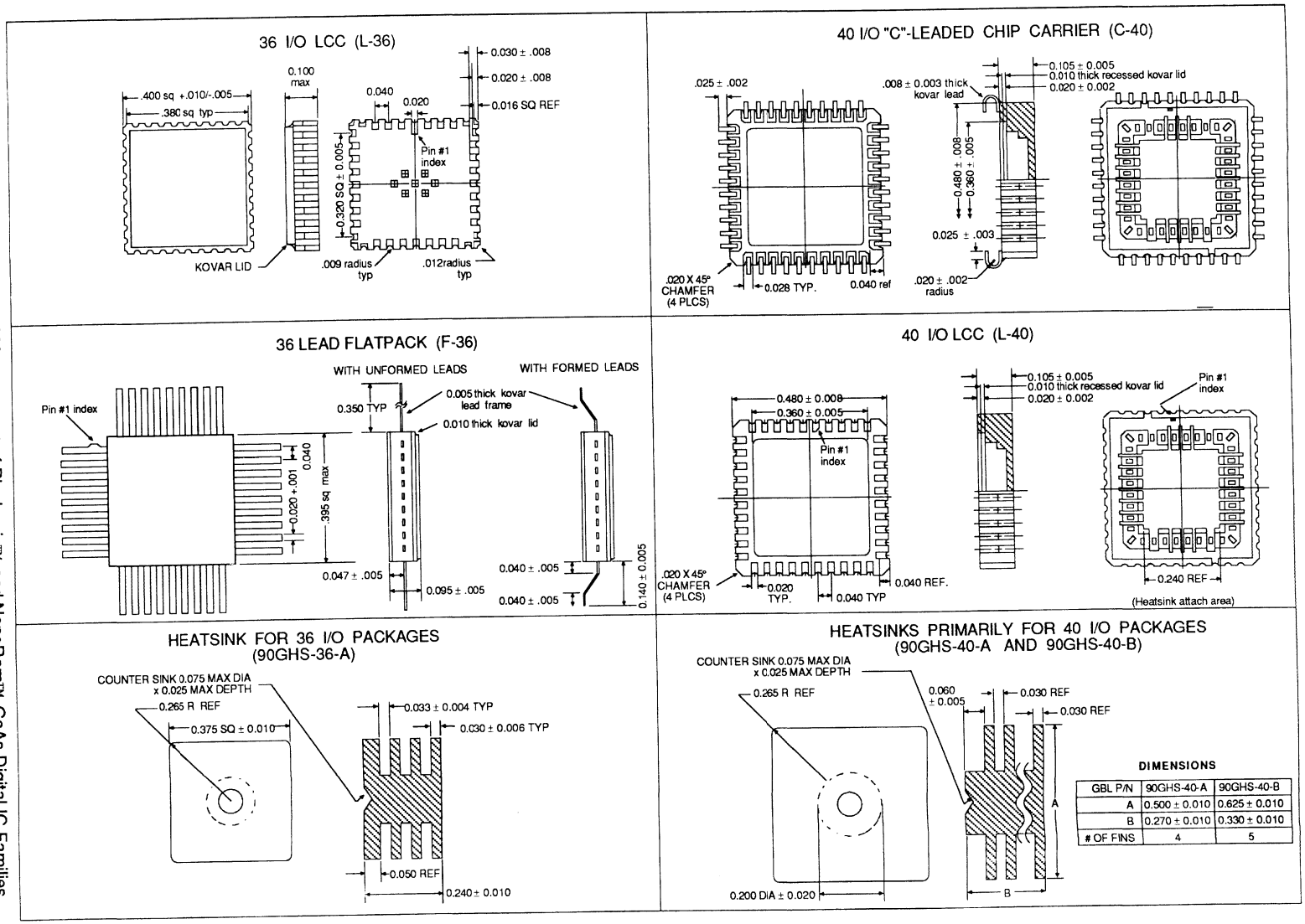


FIGURE 3: Package Cross-Sectional Views with Thermal Resistance Components

Package Thermal Resistance Components

It is useful to decompose the die surface to case thermal

FIGURE 4: PACKAGE AND HEATSINK MECHANICAL DRAWINGS



resistance of packaged GaAs devices into 3 components: die surface to package base, die surface to leads, and die surface to lid (referred to here as R1 and R2 and R3, respectively.) This is illustrated in **Figure 3.** Figure 3-a shows the F-36 package mounted in cavity-down configuration. Figure 3-b shows the L-36 package. Because the L-40/C-40 package is inverted, the package "base" is really the top surface, as shown in Figure 3-c. R3 is not shown for this case because the die to package lid thermal resistance path is not significant (the lid is recessed from the pcb surface.) The silicon substrate in the F-36, L-40 and C-40 packages plays a significant role in reducing the R2 thermal resistance. This is discussed, along with other advantages of the silicon substrate in Reference [3]

For the purpose of calculating thermal resistances (and other thermal parameters), PicoLogic™ and NanoRam™ devices can be divided into four groups, based on die size. These are shown in **Table 2.** These device groupings will be referred to throughout this application note.

TABLE 2. DEVICE GROUPS

	GROUP 1	GROUP 2	GROUP 3	GROUP 4
Die Size (mil^2)	2000 to 4000	4000 to 6000	6000 to 10000	10000 to 15000
Power Diss.	0.3 to 0.5	0.5 to 1.0	1.0 to 1.8	1.8 to 3.0
Includes	10G000A	10G002	10G022	12G014
	10G001	10G003	10G023	
	10G011B	10G004	10G024	
	10G012B	10G010	10G030	
	10G013	10G021A	10G040A	
	10G060	10G065	10G041A	
	16G010	10G070	10G044	
	16G011	10G181	10G045	
	16G020		10G046	
	16G021		10G061	
			10G100	
			10G101	
			16G040	
			16G044	

The component thermal resistances for the four die size groups and three package types are listed in **Table 3.**

Note that R1 does not vary much between package types. This is because die parameters (size, thickness, material) dominate R1. R2 and R3 depend primarily on package parameters. R2 and R3 are very high for the flatpack because of the thermally insulating package glass sidewalls. **For this reason, it is strongly recommended that the flatpack be mounted cavity-down, i.e., upside down, as shown in Figure 3-a.** Alternatively, the flatpack can be mounted cavity up if the base is in good thermal contact with the pc board. Thermal contact can be guaranteed with solder or thermally conductive epoxy. [CAUTION: the flatpack base is at VSS (nominal -3.4 V) potential while the lid is floating. The lid of the LCC is also at VSS potential. Thus, a conductive heatsink will be electrically "hot" if attached to the flatpack base or LCC lid. Use an anodized aluminum heatsink with electrically non-conductive epoxy to have the heatsink float electrically.]

TABLE 3: PACKAGE THERMAL RESISTANCE COMPONENTS (°C/W)

	GROUP 1	GROUP 2	GROUP 3	GROUP 4
F-36 PACKAGE				
R1	25	13	7	n.a.
R2 [a]	115	110	110	n.a.
R3	220	210	205	n.a.
L-36 PACKAGE				
R1 [b]	29	15	7	6
R2 [a]	58	38	22	20
R3	58	38	24	21
L-40/C-40 PACKAGE				
R1	29	15	7	6
R2 [a,c]	70	46	26	24

NOTES:
a) R2, the surface to leads thermal resistance refers to the parallel sum of all 36 or 40 leads
b) Group 3 devices in the L-36 package do not have the thermal vias.
c) Add about 1.5 to 2.0 °C/W to R2 for the C-40 case.

Case Temperatures

GigaBit Logic GaAs ICs are specified by case temperature. This implies a boundary condition where the device is in contact with an infinite heatsink through the R1 thermal resistance. Thus, for example, if a 0.5 watt Group 1 device in a flatpack has a fixed case temperature of 85°C, then the maximum junction temperature is 85°C + 10°C + 0.5W x 25°C/W = 108°C.

Appendix A discusses the measurements and calculations performed to determine the thermal resistances discussed in this section.

III. HEAT TRANSFER

Heat transfer from die to case, discussed above, is predominantly conductive (and thus is characterized by material thermal conductivities.) Case to ambient thermal resistance is essentially convective (and to a lesser extent, radiative). The convective analog of a thermal conductivity is the heat transfer coefficient, **h** (units are W/cm^2 °C). Although there are many types of convective cooling of electronic components (i.e., air or liquid,

forced or natural, etc.), we will concentrate here on forced air cooling. In general, natural (or "still") air cooling of GaAs ICs is only feasible for devices dissipating less than 1 watt unless special care is taken in designing the sub-assembly or module.

The heat transfer coefficient for forced air convection cooling can be expressed as:

$$h(v) = 0.0011 + 0.036(Cp\ \mu/k)^{.33}\ (v\ L\ p/\mu)^{.8}\ k/L \qquad (2)$$

(assuming turbulent flow) where v is the air velocity in cm/sec, Cp, μ, p, and k are as defined in Table 1, and L is a characteristic dimension of the system [4]. It is reasonable to assign to L the length of the printed circuit board, in cm. **Figure 5** shows the heat transfer coefficient as a function of air velocity for a range of "L" from 5 cm (high curve) to 20 cm (low curve). As a point of reference, 600 to 1000 lfpm air velocities are readily achievable in present-day ECL based systems. State of the art air-cooled systems achieve up to 1800 lfpm.

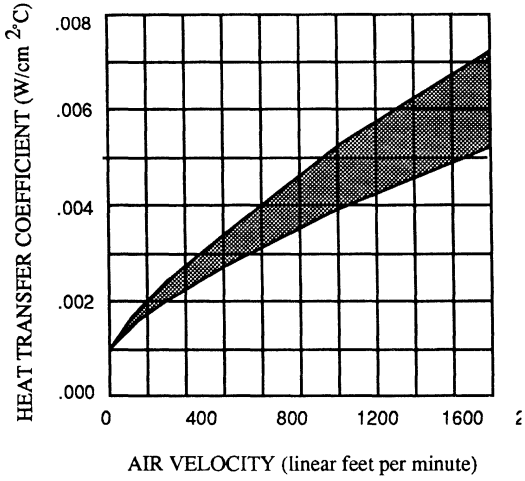


FIGURE 5: Heat Transfer Coefficients vs. Air Velocity

Heatsinks

The thermal resistance to ambient of some object with surface area "A" and heat transfer coefficient "h(v)" is given by:

$$\theta = A/h(v) \qquad (3)$$

The heat transfer coefficient describes both convection from the printed circuit board (through the package leads) and from the device heatsink (through the package body).

Figure 4 shows outlines of three heatsinks designed for use with PicoLogic™ and NanoRam™ packages. The 90GHS-36-A heatsink is intended for use with the 36 I/O packages. The 90GHS-40-A and 90GHS-40-B heatsinks are slightly larger and are intended primarily for use with the 40 I/O packages, although they can be used with the 36 I/O packages (these heatsinks will be referred to as 36A, 40A, and 40B, respectively, throughout this application note.) The effective surface areas of the 36A, 40A and 40B heatsinks are 7 sq cm, 12 sq cm, and 24 sq cm, respectively. Using Figure 5 and equation (3), it is seen that the heatsink to ambient thermal resistances at 600 lfpm are approximately 46, 27, and 13 °C/W, respectively.

Use of a heatsink is strongly recommended for all PicoLogic™ and NanoRam™ ICs, particularly those dissipating more than 1 watt.

The heatsink should be mounted to the package with a thermally conductive, electrically insulating epoxy such as Ablestik 789-4 or 561K, or Thermalloy Thermalbond™. Because heatsinks 40A and 40B are intended primarily for the L-40 and C-40 packages they have a stud to provide clearance for the top surface passive components (terminating resistors and decoupling capacitors) which the package is capable of supporting, as shown in **Figure 6**. The stud does not impact the thermal resistance because it is located directly above the heat-dissipating die. Thermally conductive epoxies such as those listed above will contribute 1 °C/W or less to overall die surface to ambient thermal resistance. Use of thermal grease or heatsink compound instead of conductive epoxy will add 5°C/W or more to overall thermal resistance.

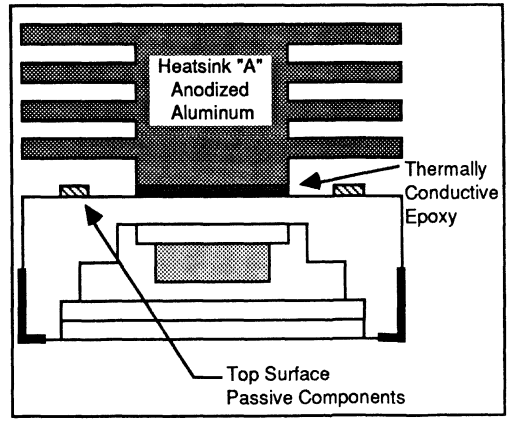


FIGURE 6: 40 I/O LCC with Heatsink

IV. THERMAL MANAGEMENT CALCULATIONS

Most PicoLogic™ and NanoRam™ devices can be maintained at reasonable operating temperatures (i.e., 125°C or lower junction temperatures) with a minimum of effort. The informa-

tion provided in Sections II and III will allow designers to determine device operating temperatures for the specific system conditions of interest (i.e., device spacing, airflow, board spacing, inlet air temperatures, etc.) **Table 4** shows rule of thumb cooling requirements for the four device groups of Table 2. **Please note that these are only approximations and that actual requirements should be carefully calculated using actual system and device parameters.** Two oz. copper (2.8 mils thick) is recommended for all board power supply planes. This will minimize pc board lateral thermal resistance.

Sample Calculation Parameters

To demonstrate the methodology for more accurately estimating device operating temperatures, a representative sample calculation will be performed. Consider an array of 32 Group 3 devices packaged in 40 I/O LCCs located on .750" centers. Unless otherwise specified, heatsink 90GHS-40-A (of Figure 3) will be assumed. The devices have a nominal power dissipation of 1.0 watt and a maximum power dissipation of 1.4 watts. The maximum ambient temperature is assumed to be 70 °C. The devices are soldered to a multi-layer, single sided (i.e., devices on one side only) printed circuit board with 2 oz. copper planes for each power supply.

TABLE 4: ESTIMATED COOLING REQUIREMENTS FOR PICOLOGIC™ AND NANORAM™ ICs

	W/O HEATSINK	W/ HEATSINK
GROUP 1		
• flatpack	not recommended	still air
• LCC	still air	still air
GROUP 2		
• flatpack	not recommended	200 lfpm
• LCC	400 lfpm	200 lfpm
GROUP 3		
• all pkgs	not recommended	200-600 lfpm
GROUP 4		
• all pkgs	not recommended	600 lfpm or greater

NOTES:
(1) These are only rules of thumb. Actual cooling requirements will be a funct ion of system parameters.
(2) Trade-offs are always possibl between heatsink size, device spacing, air velocity, board spacing, etc.

TABLE 5: SAMPLE CALCULATION ASSUMPTIONS

Nominal Device Power Dissipation.....	1.0 watts
Maximum Device Power Dissipation.....	1.4 watts
Nominal Operating Junction Temperature.....	110 °C
Maximum Operating Junction Temperature....	125 °C
Maximum Ambient Temperature.....	70 °C

System MTBF Calculation

Suppose that it is desired that the sub-system (i.e., the array of 32 devices) has an MTBF of 2 years. It can be shown (though it is not within the scope of this application note) that for a collection of "N" similar components, system MTBF can be estimated by:

$$MTBF_{system} = 0.69 * MTBF_{Component}/N \qquad [4]$$

Thus, for a system MTBF of 2 years we require a device MTBF of approximately 800,000 hours. From Figure 1 it is seen that this requires average maximum junction temperatures of approximately 110 °C.

The thermal management goal for the sample calculation is assumed to be as follows: maximum junction temperatures not to exceed 110 °C under nominal conditions, maximum junction temperatures not to exceed 125 °C under worse case conditions. For this first order calculation we will ignore the board dielectric material and assume that thermal conduction is good between the closely spaced power planes. We will also ignore the temperature and altitude dependence of the parameters of Table 1. The primary assumptions for this sample calculation are summarized in **Table 5.**

If equation [1] is applied to the nominal and worse case conditions, the following conditions result:

Nominal case: $110°C \le 70°C + 10°C + \theta_{s-a} \times 1.0$ watts
Worse case: $125°C \le 70°C + 10°C + \theta_{s-a} \times 1.4$ watts.
where θ_{s-a} is the surface to ambient thermal resistance.

The nominal case requirement is slightly more restrictive than the worse case requirement, calling for a θ_{s-a} of 30 °C/W or less.

Calculating Surface to Ambient Thermal Resistance

For Group 3 devices in the L-40 package there are two significant parallel thermal dissipation paths determining θ_{s-a}: through the package to the pc board and through the package body to the top surface and heatsink—that is, through R2 and R1, respectively. [Note: this will vary from package type to package type.]

Because some of the package pads are connected to short signal traces with relatively small heat dissipating areas, we must derate the die surface to leads thermal resistance. A reasonable estimate would be R2' = 1.5 R2, or R2'=39 °C/W. The surface to ambient thermal resistance is then given by:

$$\theta_{sa} = \frac{1}{\frac{1}{R1 + 1/h(v) \cdot A_{heatsink}} + \frac{1}{R2' + 1/h(v) \cdot A_{board,\ per\ device}}} \quad [5]$$

where h(v) is the heat transfer coefficient as a function of air velocity, $A_{heatsink}$ is the heatsink effective surface area and A_{board} is the pc board effective area per device. Each package has about 6.25 cm² of board area (including top and bottom sides, based on our .750" centers assumption) to dissipate heat in addition to the 12 cm² of heatsink area. If we assume that the board is 50 square cm in area (i.e., L in equation [2] is 7 cm), and airflow is, for example, 400 lfpm (h=.0027 W/cm² °C), then equation [5] reduces to:

$$\theta_{SA} = \frac{1}{\frac{1}{38}\text{ (hs contribution)} + \frac{1}{98}\text{ (pcb contribution)}} \quad [6]$$

$$= 27\ ^\circ C/W$$

It is seen that better than half of the heat generated by the device is dissipated through the heatsink. In the absence of a heatsink, the 12 cm² of heat dissipating area in equation [5] would be replaced by 1.5 cm (representing the package top surface area.) The resulting surface to ambient thermal resistance would be 71 °C/W. For a 1 watt device, this represents a 44 °C temperature differential at the device level. **Thus, we see that our system level reliability requirements are met if the heatsink is used, but are significantly missed if a heatsink is not used.** The benefit of using a heatsink is clear.

As a point of reference, a typical 16 pin plastic DIP with an alloy-42 leadframe and an aluminum heat-spreader has a θja of roughly 70 °C/W in forced air. Use of a copper-alloy leadframe and thermally loaded molding compound can lower the thermal resistance to about 25 °C/W [5].

Figure 7 shows the results of the calculation of equation [4] as a function of air velocity for our example for the no heatsink case and for heatsinks 90GHS-40-A and -B. The shaded region represents the conditions required for a surface to ambient thermal resistance of 30 °C/W or less (i.e., for nominal device operating temperatures of 110 °C and maximum device operating temperatures of 125 °C.) It is seen that without a heatsink, no amount of forced air brings thermal resistance low enough to ensure the desired operating temperatures, while for the 40B heatsink, a very nominal amount of air flow (about 100 lfpm) is required. As determined above, about 400 lfpm is required for the 40A heatsink. Of course, these results can vary significantly with different package to package spacings on the printed circuit board.

Table 6 a&b presents the results of the equivalent of equation [5] for most PicoLogic™ device groups, package types and heatsink sizes. Note that Table 6-a assumes a fairly dense board

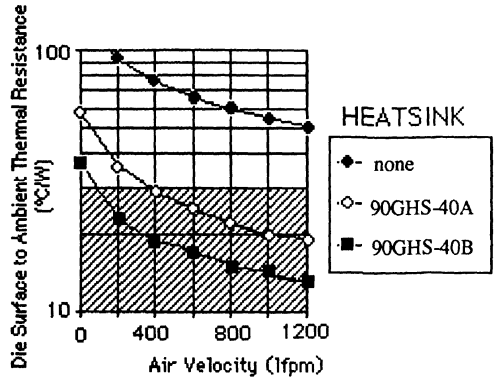


FIGURE 7: Surface to Ambient Thermal Resistance for Group 3 Device in L-40 Package Under Conditions Specified in Text

level density (.750" package centers). Prototyping densities will typically be less, with correspondingly lower thermal resistances due to the increased board area per device. This is shown in Table 6-b, which assumes packages on 1.5" centers. The difference in thermal resistance between the high density and prototype density case ranges from extremely important (for no heatsink and still air) to insignificant (for large heatsinks and high air velocities).

The thermal resistances of Table 6 include first-order temperature dependent effects. These first order effects are most important for the cases with high thermal resistance (clearly, since higher thermal resistances correspond to higher temperatures.) The most important of the first-order temperature dependent effects is that the radiation component of the heat transfer coefficient varies as the fourth power of the case absolute (°K) temperature. To include temperature dependent effects, one must assume a device power dissipation and an ambient temperature. The assumed power dissipation levels are 0.5, 1.0, 1.5 and 2.5 watts, respectively, for Group 1, 2, 3, and 4 devices. The assumed ambient temperature is 55 °C. Wide variations in these values (up

TABLE 7: AMBIENT TEMPERATURE GRADIENT (assumes 0.5 inch board to board spacing)

Air Velocity (lfpm)	ΔT (°C)/W/pkg
200	2.20
400	1.10
600	0.72
800	0.55
1000	0.44
1200	0.40

TABLE 6: PicoLogic™ and NanoRam™ Die Surface to Ambient Thermal Resistances vs. Heatsink Size and Air Velocity

Assumptions:
- 10 cm by 10 cm single sided, multi-layer, 1 oz. copper pcb
- Heatsink eff. surface areas (actual dimensions in Fig. 4) are: 36A: 7 sq. cm. 40A: 12 sq. cm. 40B: 24 sq. cm.
- Flatpack is mounted cavity down (inverted) with base in good thermal contact with pcb.
- Thermal vias are utilized on 36 I/O LCCs
- Nominal power dissipation (W) by device group is given by G1= 0.5 W G2=1.0W G3=1.5W G4= 2.5 W
- Ambient temperature is 55°C

A. HIGH-DENSITY SYSTEM ENVIRONMENTS (packages on 0.75" centers)

	36 LEAD FLATPACK (see Note 2)												36 I/O LCC								40 I/O CHIP CARRIER (LEADED OR LEADLESS)							
	Device Group 1				Device Group 2				Device Group 3				Device Group 1				Device Group 2				Device Group 3			Device Group 4		
HEATSINK...	none	36A	40A	40B	none	36A	40A	40B	none	36A	40A	40B	none	36A	40A	40B	none	36A	40A	40B	none	40A	40B	none	40A	40B
Air Flow (lfpm)	Rth, s-a (°C/W)				Rth, s-a (°C/W)				Rth, s-a (°C/W)				Rth, s-a (°C/W)				Rth, s-a (°C/W)				Rth, s-a (°C/W)			Rth, s-a (°C/W)		
0	180	96	74	53	149	81	62	43	130	72	55	38	136	90	77	64	107	74	63	51	100	52	36	80	45	32
200	140	67	52	39	125	59	44	30	114	54	39	26	93	62	54	47	78	52	44	37	81	35	24	69	33	22
400	123	56	44	34	112	49	36	25	105	45	33	22	77	52	46	42	64	43	37	32	70	29	19	62	27	18
600	111	50	40	32	103	43	32	23	98	40	29	19	67	46	42	38	55	37	33	29	63	25	17	57	24	16
800	104	46	37	30	97	39	29	21	92	36	26	17	61	42	39	36	49	34	30	27	57	22	15	53	21	15
1000	97	43	35	29	91	36	27	20	88	33	24	16	56	40	37	34	45	31	28	26	53	21	14	50	20	13
1200	92	41	34	28	87	34	26	19	84	31	22	15	52	38	35	33	42	29	27	24	50	19	13	47	18	13

B. LOW-DENSITY PROTOTYPE/TEST ENVIRONMENTS (packages on 1.50" centers)

	36 LEAD FLATPACK (see Note 2)												36 I/O LCC								40 I/O CHIP CARRIER (LEADED OR LEADLESS)							
	Device Group 1				Device Group 2				Device Group 3				Device Group 1				Device Group 2				Device Group 3			Device Group 4		
HEATSINK...	none	36A	40A	40B	none	36A	40A	40B	none	36A	40A	40B	none	36A	40A	40B	none	36A	40A	40B	none	40A	40B	none	40A	40B
Air Flow (lfm)	Rth, s-a (°C/W)				Rth, s-a (°C/W)				Rth, s-a (°C/W)				Rth, s-a (°C/W)				Rth, s-a (°C/W)				Rth, s-a (°C/W)			Rth, s-a (°C/W)		
0	125	77	62	46	112	68	54	38	105	62	49	34	60	48	44	39	45	38	34	30	59	37	28	51	33	25
200	106	58	46	35	99	51	39	28	95	48	36	24	45	36	33	30	32	26	24	22	48	27	19	44	25	18
400	98	50	40	32	92	44	34	24	89	41	31	21	40	32	30	28	28	23	21	19	44	23	16	40	22	16
600	93	46	37	30	87	40	30	22	84	37	27	18	37	29	28	26	25	20	19	18	41	20	15	38	19	14
800	88	43	35	28	83	37	28	21	81	34	25	17	35	28	26	25	23	19	18	17	39	19	14	36	18	13
1000	85	41	33	28	80	34	26	20	78	31	23	16	34	27	26	24	22	18	17	16	37	17	13	35	17	12
1200	82	39	32	27	77	32	25	19	75	29	21	15	33	26	25	24	21	17	16	15	36	16	12	33	16	11

NOTES:

(1) Required thermal resistance is given by: Rth, s-a ≤ (Tj,max - Tamb - 10°C)/(Power dissipation)

to 50 %) can be tolerated with less than a 10% effect on the thermal resistance value listed in Table 6.

Ambient requirements can have a dramatic impact on air velocity requirements. For example, if the maximum ambient requirement in our example is relaxed by 10°C to 60°C, then the required θ_{sa} becomes 40 °C/W instead of 30 °C/W. The required air velocities for heatsinks 40-A and 40-B become 200 lfpm and still air, respectively, (down from 400 lfpm and 100 lfpm).

Inlet Temperatures vs. Ambient Temperatures

Ambient temperature is defined as the air temperature in the immediate vicinity of the device. In applications where the board-level power density is high, the effect of nearby devices raising the ambient temperature above inlet temperature must be considered. In the example above, the 50 sq cm board contains 32 devices, for a total power dissipation of 32 watts. The rise in air temperature across the board can be expressed as:

$$\Delta T\ (°C) = 1.76 * P_{board}/CFM \qquad [6]$$

where CFM is the air volumetric flow rate in cubic feet per minute [6]. **Table 7** shows the temperature rise per package per watt of power dissipation as determined by equation [4] for 0.5 inch board-to-board spacing. For example, if the 32 devices on the example board are arranged 4 wide by 8 deep (deep referring to the direction of air flow), then the air in the vicinity of the last device will be 8 x 1.1 = 9 °C warmer than at the first device, assuming 400 lfpm air velocity. Thus, to insure ambients of 70 °C, the inlet temperature would have to be 61 °C or less. [Note: this ignores any temperature rise from system inlet to the beginning of the pcb of interest. In many applications this factor can represent a significant adder, up to 15 °C or more.]

Maximum ambient temperature is esstentially equivalent to system outlet temperature.

V. SUMMARY

This application note has provided the information required for proper thermal management of the PicoLogic™ and NanoRam GaAs digital IC families. The thermal characteristics of all GigaBit devices and packages have been presented, along with some background on heat transfer. A detailed sample calculation was performed to demonstrate a thermal management methodology. This methodology along with the general results shown in Table 6 can be used to estimate cooling requirements for any PicoLogic or NanoRam device as shown below:

1. Determine the desired maximum operating junction temperature and the maximum ambient (i.e., outlet) temperature.
2. Determine the device group of interest from Table 2, the package type, and the maximum power dissipation from the device data sheet.
3. Determine $\theta_{s\text{-}a,\ required}$ from the following equation:
   $\theta_{s\text{-}a,\ required} \leq (Tj,max - Tamb - 10\ °C)/P_{diss}$
4. Determine an acceptable heatsink/air velocity combination from Table 6 which satisfies
   $\theta_{s\text{-}a,\ required}$.

Some of the important points to remember about the thermal management of PicoLogic™ and NanoRam™ digital ICs are:

- Most PicoLogic™ and NanoRam™ devices will require a heatsink and forced air in high-density systems environ-ments. In general, a small heatsink and 600 lfpm of air will be sufficient. In low density prototyping environments, a heatsink alone may be adequate.
- When using a heatsink with the flatpack package,always mount the package upside down. This is the most efficient means of removing heat from this package.
- Understand the tradeoffs between board-level density, heatsink size, air velocity, and temperature requirements. There are many ways to achieve thermal management needs.

APPENDIX A: THERMAL RESISTANCE MEASUREMENTS AND CALCULATIONS

This appendix will provide some backround material describing how the thermal resistances of Section II were derived. This information will be helpful to hybrid designers or those performing custom assembly of PicoLogic™ and NanoRam™ ICs. The transient thermal behavior of GaAs ICs will also be discussed, which has important implications for testing and characterization.

Thermal Resistance Measurements

There are a number of techniques for measuring thermal resistance from junction (or die surface) to a specified reference point (case, heatsink, ambient, etc.) A number of these techniques are discussed in MIL-STD-883C, METHOD 1012.1—THERMAL CHARACTERISTICS. The die surface temperature discussed in this application note is essentially equivalent to $T_{j(Region)}$ in the MIL-STD. Typically, the reference point temperature is measured by direct means with a thermocouple. The die surface temperature can be measured directly (with liquid crystal indicators or IR microradiametry) or indirectly by measuring some temperature sensitive parameter (TSP) on the integrated circuit.

Most of the thermal resistance measurements reported in this application note were made by using the forward biased I-V characteristic of an isolated diode on the surface of the GaAs IC as the TSP. The diode is calibrated over temperature in an oven to determine the forward-bias voltage drop required to maintain a constant 250 μA current. This calibration provides the TSP temperature coefficient, $\Delta V_f/\Delta T$ (mv/°C). This coefficient will be referred to as C_{TSP}.

To measure, say, the surface to ambient thermal resistance for a particular device under test (DUT), the ambient temperature V_f @250 μA is measured with no power applied. A known amount of power, P, is applied to the DUT. After allowing several minutes for the DUT to thermally stabilize, the new V_f required to maintain the 250 μA is measured. The surface to ambient thermal resistance of the DUT is then given by:

$$\theta sa = [V_{f,init}-V_{f,final}]/[(C_{TSP})(P)] \quad (A\text{-}1)$$

Thermal Resistance Calculations

The thermal resistance through a path of cross-sectional area A and thickness t, as shown in **Figure A-1** is given by:

$$\theta = t/(K\,A) \quad (A\text{-}2)$$

where K is the material thermal conductivity (see Table 1).

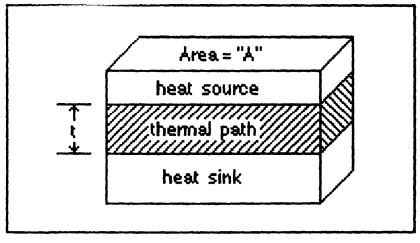


FIGURE A-1: Thermal Resistance Path

However, when the cross-sectional area of the heat source is less than that of the thermal conductor on which is it sits (as is the case for an IC mounted on a package or hybrid substrate), then thermal spreading takes place. This is shown in **Figure A-2.** For most cases it is adequate to assume a spreading angle of 45°. The cross-sectional area to use in equation [A-2] is then the average of the heat source cross-sectional area and the projected cross-sectional area of the thermal spreading path on the heat sink.

As mentioned in Section II, thermal resistance networks can be treated as electrical resistance networks. Thus, the large number of tools available for analyzing electrical networks can be utilized for thermal analysis of complex structures. For example,

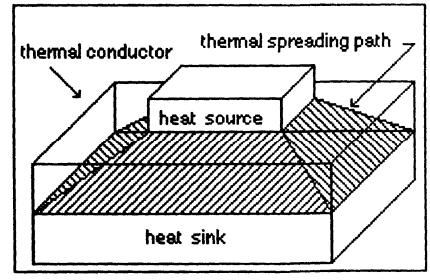


FIGURE A-2: Thermal Spreading

a resistive network like that shown in **Figure A-3** can by studied by an electrical analysis program such as SPICE. The value of the individual resistors is determined by the thermal conductivity of the material and by the "grid size" of the network. If the heat source is modeled by a current source whose value in amperes is equal to the power dissipated in watts, then the nodal voltages at a given point will correspond to the temperature differential from heat source to that point. More than one current source can be used to model either power distribution across an IC surface or muti-chip hybrids. Any number of material layers can be modeled. Programs such as SPICE can analyze networks with hundreds or thousands of nodes and resistors.

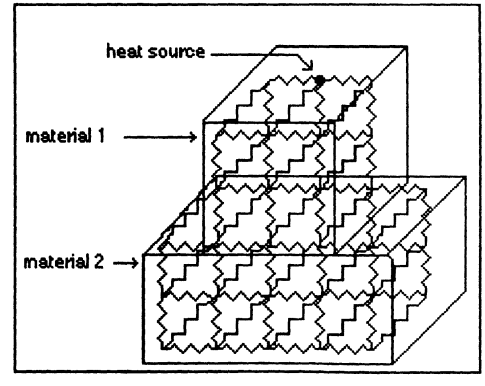


FIGURE A-3: Network for Thermal Analysis

Transient Behavior

When power is applied to an IC, it does not instantaneously realize its equilibrium temperature. This is because the heat is initially absorbed by the thermal capacities of the materials in the thermal path. The thermal capacity of a material is given by the product of its specific heat (see Table 1) and its mass. Thermal capacitances and resistances can be analyzed as if they were electrical capacitances and resistances. Thus, an equivalent

circuit to analyze the transient thermal behavior of a packaged IC is shown in **Figure A-4**.

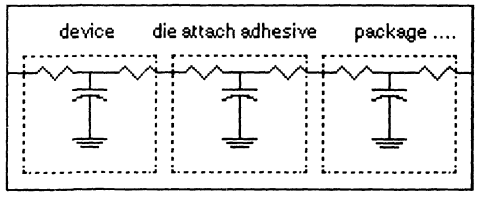


FIGURE A-4: Equivalent Circuit for Transient Analysis

With a model such as that in Figure A-4, the device transient or "turn-on" thermal behavior can be studied. Figure A-5 shows the turn-on thermal behavior of a 1.5 watt Group 3 device in 40 I/O LCC withot and without heatsink. It is seen that up to about 1 second, there is no difference in junction temperature between the heatsink and no heatsink case. However, the junction temperaure of the device without heatsink rises rapidly after about 1 second and stabilizes after about 2 minutes. The device with a heatsink takes longer to stabilize (about 10 minutes) due to the large thermal capacity of the heatsink.

This transient thermal behavior (not significantly different from that of silicon ICs) is important to keep in mind when testing, characterizing, and "cold-starting" PicoLogic™ and NanoRam™ ICs. For example, during a short test, case temperature or heatsink temperature may not be a good indicator of junction temperature.

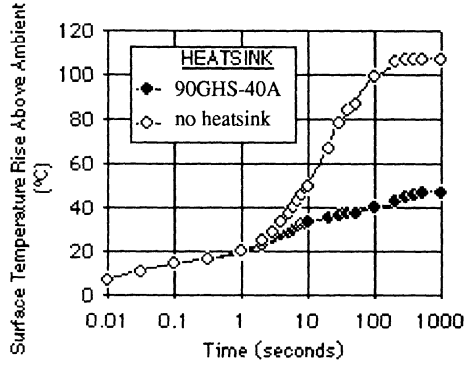


FIGURE A-5: Transient Turn-On Response of a 1.5 Watt Group 3 Device in 40 I/O LCC with and without Heatsink

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INTERFACING PICOLOGIC™ AND NANORAM™ GaAs IC's TO OTHER LOGIC FAMILIES

Application Note #4 By: Carl Eggert Deierling

I. INTRODUCTION

To enhance the acceptance of a new logic family it is desirable to be compatible with existing logic families. Since the gallium arsenide (GaAs) NanoRam and PicoLogic families set new standards for speed, unachievable by silicon, it is obvious that they should be compatible with the highest speed pre-existing logic family: ECL. PicoLogic devices are not intended to replace ECL devices, but rather to complement them; being used in those critical path areas where every picosecond saved will yield a benefit.

The implementation of ECL compatibility is somewhat complicated because three distinct and incompatible ECL families exist. In addition, there are applications in TTL or CMOS systems requiring either the minimal skew time, low propagation delays or short rise and fall times of PicoLogic devices. This note discusses the issues that arise when interfacing PicoLogic and NanoRam devices to and from other logic families. PicoLogic devices utilize the Capacitor Diode FET Logic (CDFL) circuit design approach which is described in the next section.

II. CDFL CIRCUITRY

Capacitor Diode FET Logic (CDFL) and its different applications have been extensively discussed in previous literature ([1], [2], [10]). The CDFL-based circuit provides high speed operation while minimizing power consumption. High production yields [9] obtained on large quantities of numerous different types of SSI and MSI circuits, and subsequent reliability testing [3] has validated the CDFL circuit design approach for logic design at very high clock rates. An analysis of the circuit will facilitate subsequent discussion of the circuit approaches used for achieving compatibility with other high speed logic families.

A. CDFL Internal Components

CDFL circuitry consists mainly of depletion-mode metal-semiconductor field-effect transistors (D-MESFET) and Schottky diodes (the F and D respectively in CDFL). The DC characteristics of these GaAs Schottky diodes are similar to those of silicon P-N diodes, with typical forward voltage drops of about 0.8V at typical current densities, except that their usable frequency range extends beyond 500 GHz (R_sC_j cutoff). The single gate MESFET (Metal Semiconductor Field Effect Transistor) is a Schottky junction depletion mode N-channel FET, with a nominal pinchoff voltage equal to -1.0V and DC characteristics similar to a silicon N-channel JFET. The f_t (current gain-bandwidth product) of these one micron gate length transistors are in the 12 - 15 GHz range.

In addition to these major components each circuit also employs N^+ implant resistors and gateless MESFETs referred to as saturation resistors (SATR's) for current limiting. Reverse biased large area diodes, acting as capacitors are used as ac-coupling (speed-up) capacitors (the C in CDFL) to handle the charging and discharging of circuit loading (fanout and parasitic) capacitances and for power supply decoupling. Dual gate MESFETs are utilized to form the NAND function and for other special-purpose functions.

B. CDFL Circuit Description

Figure 1 shows a portion of the schematic of an MSI logic function employing the basic CDFL NOR gate circuit building block. The circuit is implemented in 3 stages: input, NOR gating and output stage.

1. Input Section

The input section provides the functions of input overvoltage protection, level shifting ECL inputs by -2.4V, and ECL threshold level tracking.

The input current is limited to a maximum of 12 mA by means of the SATR (Q1) in series with the input. This, in conjunction with the input clamp diodes which are internally connected to VDDL and VSS, limits the voltages reaching the internal structure of the IC. This configuration will provide input protection against Electrostatic Discharge (ESD) and will also permit the impression of large amplitude sinusoids, thereby increasing the input $\Delta v/\Delta t$ during the transition region. This reduces the jitter or phase noise at the output of PicoLogic IC's. Input clamping safely permits input signal amplitudes in excess of 4.5V peak-to-peak.

The three diodes and two resistors connected from the input SATR to the gate of Q4 shifts the input signal 2.4V negative such that it is at the appropriate level to cause the -1V pinchoff gating transistor (Q4 or Q5) to be switched on and off in response to ECL level inputs. DCAP, the single large reverse-biased diode in parallel with these three series diodes acts as a high frequency coupling capacitor. This diode capacitor assures, in the case of negative transitions at the input, that circuit capacity below the diodes will be charged by the input itself, and not necessarily rely on the internal sinking current provided to VEE by transistor Q3, therby improving the response to negative input transitions.

Transistor Q3 provides the biasing current through the diode level shifter which results in the voltage drop across it. By

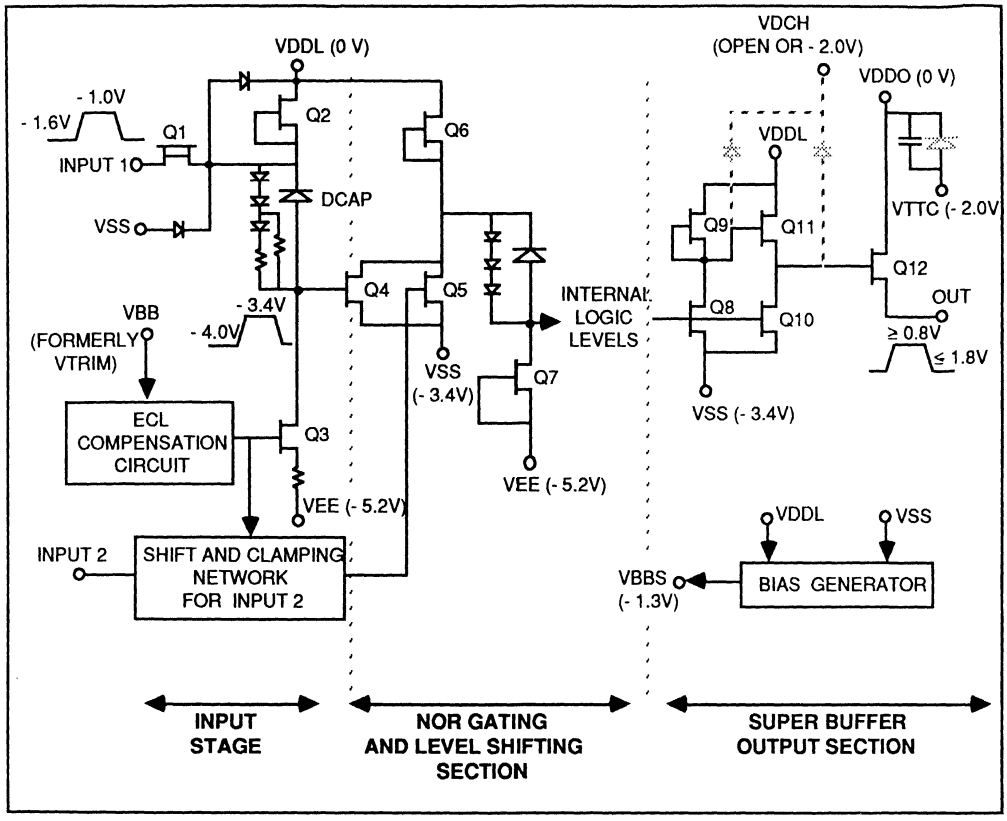


FIGURE 1. CDFL basic schematic for a 2-Input NOR gate

controlling the voltage applied to the gate of Q3, the current is made to vary the drop across the shifter. As the gate voltage is made more positive, the transistor current increases and the forward drop across the diodes (V_f) and series resistor increases. The result is an increase in the shift voltage and consequently in the input threshold voltage. Likewise, as the gate voltage of Q3 is made more negative and approaches the pinchoff voltage of the transistor, the current is reduced and the drop across the diodes decreases, hence reducing the input threshold voltage. This control of Q3 gate voltage is the basis for the ECL compensation schemes to be discussed in greater detail later in section **IV-B.**

The sole function of Q2 is to source a portion of the current being sunk by Q3 so as to minimize the input current (typically 200 μA). The current sunk by Q3 varies as a function of the ECL compensation voltage, and the current sourced by Q2 is fixed. Therefore, the current direction at the input pin could reverse and actually flow out of the input in the case of extreme threshold requirements which would reduce the current through Q3 to a value less than that supplied by Q2. For this reason unused inputs should not be left open, although, they would generally be pulled low at normal temperatures with usual values of VBB and VSS. To guarantee specific input levels, inputs should be tied to VDDL or VSS (or VTT) for a high or low state respectively.

2. NOR Gating Section

The internal logic portions of the circuit are represented by Q4, Q5, and Q6. As the gate to source voltage of either Q4 or Q5 goes more positive than the pinchoff voltage (-1V), the transistor begins to pass drain current in increasing amounts (in an approximate $[V_{gs} - V_p]^2$ dependency) as Vg is increased. Assuming, for example, if Q5 is below pinchoff (Vg < - 4.4V), if the gate of Q4 is taken more positive than about - 0.2V (with typical FET swings), the drain current of Q4 will exceed that which can be supplied by the pullup active load Q6 (usually about 2/3 the size of Q4 or Q5). Hence, its drain output voltage will quickly drop from near VDDL (the value at pinchoff) to a few hundred mV

above VSS.

Because these are N-channel MESFETs, the drain output voltages are more positive than VSS, but since they are depletion mode MESFETs, this output voltage must be level shifted to the negative (below VSS) potentials required at the gate of loading stages to turn the D-MESFETs off. This is identical to the level shifting portion of the input circuit with the exception that the ECL compensation circuitry is unnecessary.

In the case of a simple NOR gate such as a 10G001, it should be noted that the gating section is merged with the superbuffer output, thus eliminating transistors Q8 and Q9.

3. Super Buffer Output Section

The output driver section, one of the major improvements from earlier generation PicoLogic designs, now incorporates a superbuffer. Earlier generation IC's used only an unbuffered source follower at the output. The superbuffer shown in **Figure 1** is an additional gain stage formed by Q8, 9, 10, and 11 with Q11 and Q12 forming a Darlington-type output driver. This provides considerable drive capability to the gate of Q12, improving output rise time which makes it more nearly equal to the fall time of 100 to 150 ps. The size of the output source follower is equal to 600 to 750 microns which assures that minimum VOH of -0.8V can be maintained even when driving a 25Ω load terminated to -2.0V (48 ma).

Two shaded diodes are shown with dotted line connections to VDCH. These are used to limit the high state voltage that may be applied to the gates of Q11 and Q12 which in turn clamps the output high voltage. Connection of the VDCH pin to VTT = - 2V will limit maximum VOH to ~ - 0.5V. VDCH control of the PicoLogic VOH level is necessary, in some instances when a PicoLogic device drives an ECL device, to avoid saturating the ECL input. The voltage supplied to the VDCH pin may be adjusted if required to provide more precise control of the output high level. One feature of VDCH which should be noted is that its use will limit the waveform to the fastest portion, eliminating the "tail" on the rising edge. Alternate schemes for limiting VOH will be discussed in section **IV-A** of this application note. It should be noted that due to pin count limitations, the diodes and associated VDCH pin have been deleted in some recent designs, hence the shaded depiction in **Figure 1**.

Newer generation PicoLogic IC's contain a threshold reference generator which internally generates -1.3V and provides it on the VBBS output pin. This pin is normally strapped to the VBB pin when the PicoLogic device is being driven by another PicoLogic IC. As discussed in section **IV-B**, for very precise threshold tracking of ECL levels, an ECL VBB voltage level may be applied to the VBB input pin.

C. Circuit Design Improvements

Reference 1, which has been superceded by this application note, describes the first generation CDFL circuits used in PicoLogic devices. These differed from today's circuitry in the following three areas:

1) In first generation CDFL, the input section had a different ECL tracking circuit and an associated input called VTRIM. This distinction will be discussed in greater detail later in section **IV-B.**

2) The output stage was also different in that it lacked the superbuffer and consisted of only the output source follower (Q12 of **Fig. 1**).

3) Another difference is that the majority of the optional diode clamping inputs (Vich, Vicl, Vlcl, Vlch, Vdcl) which were formerly provided in the circuit to improve performance, have been deleted. Improved performance, as a result of advancements in production processes and circuit design techniques, have minimized the advantage to be gained by the use of these clamps. Furthermore, the additional voltage supply requirements necessary to use these clamp diodes, and the need for extra I/O pins as device complexity advanced from the SSI to the MSI level of integration, indicated that removing these diodes and their associated pins from the circuit was prudent.

The only PicoLogic circuits which do not as yet contain the circuit revisions mentioned herein, are the 10G060, 10G065, and 10G070 divider circuits, which are normally driven from a high level source such as a VCO, and the 10G040 and 10G041 time division multiplexer and demultiplexer. These latter two circuits will incorporate VBB in the "A" revisions. Neither the 10G012A nor the 10G021A incorporate the ECL compensation circuit, because these circuits have differential inputs (data inputs only on the 10G021A). However, VBBS is provided on the 10G021A and 10G012B. Other than this, the 10G021A, 10G012A and all new devices possess all the circuit improvements mentioned herein. For specifics see the data sheets.

D. CDFL DC Power Supplies

With reference to **Figure 1**, the power supply requirements for the PicoLogic and NanoRam families are indicated in **Table 1**.

VDDL is the drain power supply for the logic and input sections and is normally connected to ground in an ECL environment. This corresponds to VCC2 of the 10K ECL families and VCC for the 100K ECL family. The second ground connection is the drain supply for the output transistors which is identified as VDDO. This is analogous to 10K's VCC1 and 100K's VCCA. The rationale for the separation of the ground connections is identical to that of ECL: to isolate any ground noise introduced by output switching transients from the internal logic functions. VDDO will normally be connected to the same ground plane as

VDDL; however, the provision of separate pins eliminates any common package lead or wire bond inductance. As will be described in subsequent portions of this application note, additional interfacing flexibility is also provided by separating the VDDL and VDDO pins. Note that multiple package pins for VDDL, VDDO and VSS are provided to reduce inductances and to share supply currents. All of these pins should be connected to the appropriate supply planes on the circuit board for proper low-

TABLE 1.: PicoLogic™/NanoRam™ family power supply voltage specifications*.

VOLTAGE	MINIMUM	NOMINAL	MAXIMUM
VSS	-3.5 V	-3.4 V	-3.3 V
VEE	-5.5	-5.2	-5.1
VTT	-3.5	-2.0	-2.0
VCC**	+4.75	+5.0	+5.25

* VDDO and VDDL are equal to zero Volts (Gnd)
** NanoRam™ and analog parts only.

noise operation and reliability.

The VEE supply is connected to -5.2V and corresponds to ECL's VEE supply. In CDFL, VEE provides the most negative potential used for a current source, and unlike the VEE of ECL, it has relatively low DC and transient currents.

VSS (- 3.4V) acts as the source supply for all logic switching circuitry. This supply is the major supply for CDFL circuitry and would establish the input threshold were it not for compensation schemes added to provide ECL compatibility (section IV-B). For this reason it should be maintained as noise free and well regulated as possible. Both heavy transient and DC currents will flow from VDDL to the VSS supply.

With reference to **Figure 1**, the VBB input (formerly VTRIM) controls the ECL threshold tracking circuit in current generation PicoLogic devices. This circuit constitutes a major portion of the design methodology used to obtain precise input threshold matching and tracking when PicoLogic IC's are driven from low level inputs such as ECL. The use and operation of the threshold tracking circuit will be discussed extensively in section IV-B.

A VTTC (called VTT in data sheets prior to 1986) pin is indicated on the data sheets and on the schematic of **Figure 1**. This pin should be connected to the VTT (external termination voltage) power plane for normal ECL/GaAs interfacing. This pin does not connect to the GaAs die but provides for decoupling between the VDDO pin and VTTC pins. Since output currents flow from the VDDO supply to the VTT supply, a capacitor inside the IC package can provide the charge needed during the turn-on transition to assure a short rise time at the output. Note that this capacitor is implemented with a reverse biased silicon diode in the case where the package employs a silicon substrate. For this reason, VTTC should never be connected to a potential more positive than VDDO. **Figure 1** shows the VTTC decoupling capacitor although it is on the silicon substrate rather than on the GaAs chip to emphasize that the diode is present in packaged parts. If VSS is used as the termination supply then the VTTC pin should be connected to VSS. Note that this pin requires no DC current.

The last DC power pin shown on the schematic, used for clamping the outputs in the high state, is called VDCH (Voltage for Driver Clamp High) which was discussed in section II-B3. In general, VDCH will be connected to VDDL if no clamping is desired, otherwise it will be connected to VTT or a potential near VTT for special interface applications. Since current flows out of the VDCH pin, any supply used to furnish VDCH must be capable of sinking current; in fact passive regulating components to VSS (such as series diodes) may be used.

All power supply pins on packaged devices are decoupled inside the package. This may be either by means of a large area silicon P-N diode capacitor in the case of the silicon substrate for all flatpacks, as described above, or by means of ceramic chip capacitors in some of the LCC packages.

III. POWER SUPPLY COMPATIBILITY

The first element considered when addressing the issue of compatibility between logic families is power supplies. **Table 2** illustrates the degree of supply compatibility between different logic families including GaAs, ECL, and TTL/CMOS, and is described below.

A. GaAs DC Power Supplies

Different GaAs manufacturers do not have identical supplies due to differences in circuit design and pinch-off voltages employed. Some attempts to standardize are underway; JEDEC Committee 50.2 has been formed to further this goal. Unfortunately the prior introduction of a number of parts by various manufacturers hinders the compatibility of first generation parts.

All PicoLogic components operate over their data sheet operating temperature range with the tolerances given **in Table** 1 and provide complete ECL compatibility except as detailed otherwise in the data sheets. **Table** 3 indicates the power supplies which may be used to satisfy different system requirements. The voltage difference between each of the supplies are approximately the same but the ground reference has been altered to provide the

desired system ground. VDDL, normally considered the ground reference in ECL systems, may be varied from nominal without major effects on circuit operation. Internal logic swings, and the drive in the high state to the gate of the ouptut source follower will vary as a function of this supply.

Table 3 (section f) refers to an option which is available in PicoLogic IC's which have a VDCH pin. The outputs of these PicoLogic IC's can be logically inverted from their defined logical state very easily by just a change in the supply voltage that is connected to VDDO pin and the termination supply voltage.

B. ECL Supplies

Early generation ECL families are powered from VEE of -5.2V and require an external load termination supply of -2.0V. These two voltages were adopted by the PicoLogic family. The more recently introduced ECL family, F100K, was designed to operate with VEE nominally at - 4.5V. Fortunately the voltage compensated 100K family operates well with VEE equal to -5.0 to -5.4V and 100K's increased power dissipation at this higher voltage is proportional to the voltage increase (not the square of the voltage increase) because the internal voltage compensation feature stabilizes the DC current. In the case of depletion mode GaAs devices, however, an intermediate additional supply is also required. In the case of PicoLogic IC's, a VSS equal to -3.4V has been selected for the optimum operating point.

C. TTL & CMOS SUPPLIES

TTL and CMOS power supplies generally operate with VCC set to +5.0V. This supply, or any other positive supply up to +6V can be used as the supply for the load resistor when driving from PicoLogic IC's into CMOS or TTL families. See the I/O compatibility section for further discussion of this issue.

IV. I/O COMPATIBILITY

The second area in which compatibility is an issue concerns the interfacing of signal levels. Two distinct cases exist: PicoLogic devices driving another family and visa versa. **Table 4** presents an overview of the degree of signal level compatibility between all relevant logic families.

A. PicoLogic IC's Driving ECL

The ability of PicoLogic IC's to drive ECL is not an issue since PicoLogic IC output signal swings considerably exceed the input levels required by ECL. Thus, despite the variation of input level requirements of 10K and 10KH with temperature, and even with supply voltage in the case of the Motorola 10K family, PicoLogic IC's can easily supply VOH and VOL of sufficient magnitude to provide even better noise margins than ECL intra-family specifications. **Table 5** [4-8] provides the required input levels for the various ECL families and compares these to PicoLogic family output levels.

1. Requirements to Limit "High" Level

Certain parts in ECL families (10K, 10KH and 100K) may require that the input voltage (VIH) be limited to be no more

TABLE 2. Power supply compatibility matrix

	GaAs D-MODE	ECL	TTL / CMOS
PicoLogic	Different circuit design approaches and pinchoff voltages may dictate different supplies	PicoLogic requires one additional supply: - 3.4 V	+ 5V supply can be used for pull-up resistor
ECL	--	100K uses - 4.5 V (standard; functional at - 5.2V); 10K and 10KH use - 5.2 V	No compatibility
TTL/CMOS	--	--	Compatible, except newer CMOS families may operate from + 3.3 V supplies

TABLE 3. Power supply options for multi-logic family environment

	Configuration	VEE	VSS	VDDO	VDDL	VTTC	VTT
a	Std ECL Interface [1] Vo = -0.6 to -1.8 V	- 5.2V	- 3.4	0	0	- 2.0	- 2.0
b	Std GaAs Interface [2] Vo= 1.2 to 3.2	- 2.0	0	+ 3.5	+ 3.5	+ 1.0	+ 1.0
c	TTL/CMOS Outputs [3] Vo= 0.4 to 5 V	- 5.2	- 3.4	0 or - 0.5	0	Note 4	+ 5.0
d	Test Interface [5] Vo =+0.2 to +1.4V	- 3.2	- 1.4	+ 2.0	+ 2.0	0	0
e	Positive Supplies [6] Vo =+3.2 to +4.6V	0	+ 1.8	+ 5.0	+ 5.0	+ 3.0 or + 1.8	+ 3.0 or + 1.8
f	Output Inversion [7] Vo = -0.1 to - 1.6V	- 5.2	- 3.4	- 2.0	0	Note 4	0
g	AC Signal Mode [8] Vo = -0.8 to +0.8V	- 3.8	- 2.0	+ 1.4	+ 1.4	- 2.0	- 2.0

1. Outputs may be shorted to GND. Optional connection for 10GPDK/90GUPK Prototyping Kits. Use VDCH or other resistor scheme to limit VOH.

2. Outputs may not be shorted to GND. VDCH should not be used.

3. Outputs may be shorted to GND. VDCH must not be used. Use VDDO at - 0.5 volts if a low value load resistor (e.g. 100 Ohms) is used for faster output edge rates. Outputs are logically inverted.

4. Do not connect to a potential more positive than that connected to the VDDO pin.

5. Scopes and test equipment provide termination. Shorting outputs to ground may damage the device.

6. A transistor translator must be provided to drive TTL (see Fig. 5b). Shorting outputs to ground will damage the device.

7. VDCH must be tied to - 2.5 volts (one diode drop above VSS). Shorting outputs to ground may destroy device. Tying outputs creates wired AND.

8. Inputs may be AC- coupled with a termination resistor to ground.

positive than -0.6V. Specifically, those ECL inputs which have a collector pullup resistor on the input transistor side of the differential pair are susceptible to saturation; those with collectors directly tied to VCC (0V) would require positive input voltages to cause saturation. VOH limiting prevents the speed degradation which would result if the ECL input transistor (being neither Baker clamped nor gold doped) were driven into saturation. Although VIH(max) may range from -0.52 to -0.88V for the various families over the full military temperature range, discussions with ECL manufacturers indicate that VIH(max) = - 0.6V will not saturate most ECL parts at temperatures above 25°C. Note that the actual specification of VIH (max) **per Table** 5 is actually more negative than this value, and a worst case design would mandate an even more restrictive permissible signal variation in the high state. Since PicoLogic IC's VOH, if unlimited by external means, will reach -0.6 to -0.3V when terminated with 50 ohms to -2.0V, various alternatives to limit the VIH reaching an ECL device are discussed here. Reference should be made to **Figure 2.**

Figure 2a portrays the source follower output terminated in 50 Ohms to -2.0V. In this case, VOH is not limited, and is the preferred interface except when VOH limits are necessary for ECL VOH compatibility.

Figure 2b is similar except that the termination voltage is -3.4 volts which is equal to VSS. VOH is shifted negatively, but may still be too

positive for certain ECL inputs. This would be used when a separate - 2 volt supply is not available. Note that the output transistor is turned on in both the high and low states making the part suitable for source termination.

Figure 2c offers an excellent solution for limiting the VIH to 100K ECL parts, since the variations in pinchoff voltage (Vp), and other internal parametric variations are attenuated by the effect of the series resistor Rs. Values for VOH and VOL are given for various values of Rs. This solution also has the benefit of reducing power dissipation slightly and providing slightly better output impedance match to transmission lines on output "high", minimizing signal reflections. Output edge rates are not degraded. In this scheme, the Rs must be located very close to the PicoLogic output pin to reduce the line reflection.

Figure 2d illustrates an alternate scheme for reducing

TABLE 4. Input/output compatibility matrix for different families of logic devices

		DRIVEN LOGIC		
	LOGIC FAMILY	**GaAs D-MODE**	**ECL**	**TTL/CMOS**
SOURCE LOGIC TYPE	**PicoLogic**	Large output signal amplitudes (in comparison with ECL levels) simplify GaAs to GaAs Interfaces and provide high noise immunity	Large output signal amplitude of GaAs simplifies interfacing to ECL over all temperatures and voltages. May need to limit VOH.	Symmetry of output source follower MESFET permits direct interface with proper voltage shift
	ECL	Small output signal amplitudes of ECL with varying temperature and voltage coefficients require caution when interfacing	Small output signal amplitudes of ECL with varying temperature and voltage coefficients require caution when interfacing	Requires level translator
	TTL / CMOS	Requires Translator or resistor network	Requires Translator	Compatible, except where + 3.3V power supply voltage is required

TABLE 5. PicoLogic and ECL interface specifications

	PicoLogic & NanoRam		10K ECL				MECL 10KH™		100K ECL
			Fairchild		Motorola				
TEMPERATURE [DEGREES C]	0 to +85		0	+75	0	+85	0	+75	0 to +85
VOH max	- 0.3 V	VIH max	- .84	- .72	- .85	- .70	- .84	- .735	- .88
VOH min	- 0.8 V	VIH min	-1.14	- 1.04	- 1.15	- 1.03	- 1.17	- 1.07	- 1.16
VOL max	- 1.8 V	VIL max	-1.49	- 1.45	- 1.49	- 1.44	- 1.48	- 1.45	- 1.47
VOL min	- 2.0 V	VIL min	-1.87	- 1.83	- 1.87	- 1.82	- 1.95	- 1.95	- 1.81

	10K ECL				MECL 10KH™		100K ECL	PicoLogic and NanoRam	
	Fairchild		Motorola						
TEMPERATURE [DEGREES C]	0	+75	0	+85	0	+75	0 to +85		0 to +85
VOH max	- .84	- .72	- .85	- .70	- .84	- .73	- .88	VIH max	.0
VOH min	- 1.00	- .90	- 1.00	- .89	- .92	- 1.02	- 1.02	VIH min	- 1.0
VOL max	- 1.66	- 1.62	- 1.66	- 1.61	- 1.63	- 1.60	- 1.62	VIL max	- 1.6
VOL min	- 1.87	- 1.83	- 1.87	- 1.82	- 1.95	- 1.95	- 1.81	VIL min	- 2.5

* MECL 10KH is a trademark of Motorola Inc. .

VOH. Since the VDDO drain supply is isolated from the internal logic drain supply VDDL, the output high level can be restricted by reducing the voltage applied to the VDDO pin. One possible simple scheme for deriving this voltage is with a diode in series with the VDDO pin and system ground as shown. A silicon P-N diode such as a 1N3600 or 1N5120 has tightly specified forward voltage drop and temperature characteristic over an appropriate operating current range. Reference to **Figure 3** shows the VIH (min and max) values for the Motorola 10K family over the military temperature range. Other 10K families are somewhat more tolerant to VIH(max) variations. Superimposed on these curves are the VOH (min and max) curves for PicoLogic devices with their VDDO connected as shown in **Figure 2d**. Note that the output is terminated to -1.7 volts with a 50 Ω resistor to limit the VOL to that specified for 10K ECL VIL(min): -1.58 to -1.82V (over the entire temperature range). The VOH curves account for worst case temperature coefficients of the diodes, which results in the non-parallelism of these curves as the temperature is varied. The diode should be located proximate to the ECL chip receiving the signal to insure best temperature tracking. Decoupling at the GaAs part is essential not only due to the distance from the diode, but also to negate the undesirable effects of the forward and reverse recovery times of the diode which is approximately 10ns (an eternity at GaAs speeds).

Other power sources or diode drop networks may be utilized provided that the combination of capacitor and switching speed of the network will support the speed of PicoLogic devices. A silicon hot carrier (Schottky) diode could be used to achieve improved switching characteristics, however, it would result in a higher VOH. The circuit configuration of **Figure 2d** has very good temperature tracking capability and is very attractive when interfacing to non-temperature compensated ECL families such as 10K and 10KH. If the minor degradation in rise and fall times due to higher impedance VDDO becomes objectionable, a separate DC supply which is temperature compensated with a diode

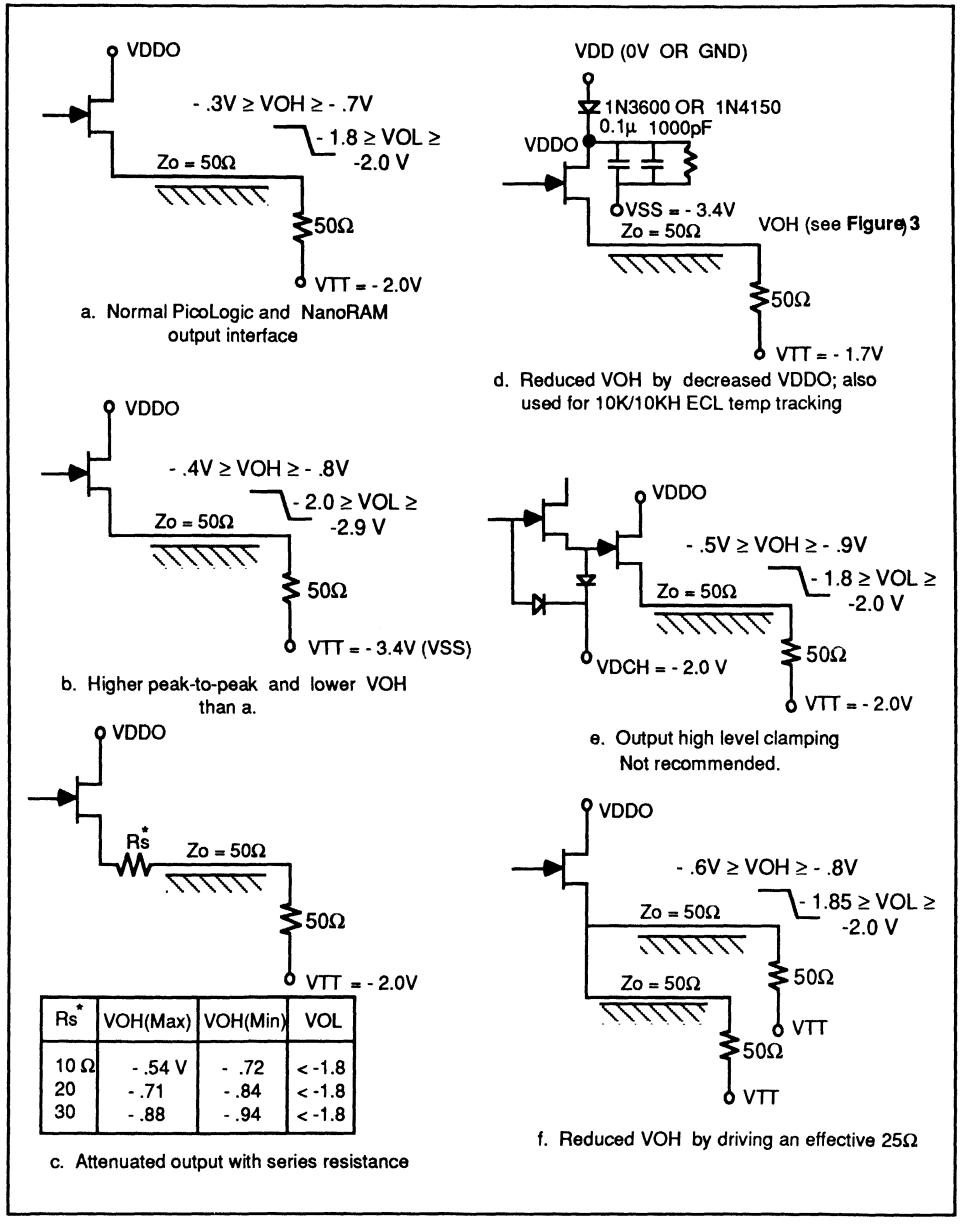


FIGURE 2. Options for limiting PicoLogic VOH when interfacing to ECL devices

thermally coupled to the ECL family could be used to power VDDO.

Figure 2e illustrates the use of the VDCH (Voltage for Driver Clamp High) pin, which has been provided on most PicoLogic devices designed for ECL output compatibility. This pin can be biased to -2.0V when driving ECL to limit VOH. While the VDCH approach offers the best AC performance (lowest delay times and fast, clean rise times), for very precise VOH control it may be necessary to adjust the VDCH potential because of some dependence of VOH (at a given VDCH value) on temperature and internal parameters (mainly pinchoff voltage) of the IC.

Figure 2f demonstrates the effect on VOH of terminating the output to a 25Ω load. This is the equivalent of driving a 50Ω bus terminated at each end. VOH is reduced compared with **Figure 2a.**

B. ECL Driving PicoLogic Devices

The most difficult issue concerning ECL compatibility is encountered when driving PicoLogic IC's from ECL. Since the input threshold of ECL may be affected by temperature and VEE variation, ECL circuitry has been designed so that its output tracks input threshold variations. The temperature coefficient of the ECL threshold, given in **Table 6**, can be predicted for a given ECL logic family and varies from ~ 0 for temperature compensated 100K to approximately +1.3 mV/°C for 10K. Likewise, the input threshold variation with VEE, summarized **in Table** 6, ranges from ~0 for voltage compensated varieties of 10K, 100K and 10KH to 140 mV/V for Motorola 10K and MECL III. Since the input thresholds vary as a function of both temperature and VEE in some of these ECL families, the outputs must track the inputs to a first order in order to provide maximum noise immunity.

Due to this variation in ECL output thresholds, it is impossible to incorporate a fixed compensation scheme for an interfacing family. Indeed ECL designers must carefully consider interfaces between 10K and 100K, and even consider the loss of noise margin between different 10K devices where either thermal or VEE gradients occur between interfacing devices in the same system.

1. ECL Threshold Tracking Using VBB

Instead of providing a fixed compensation scheme, current generation PicoLogic parts incorporate a VBB input pin which permits the interfacing device to control the input threshold of the GaAs device. This voltage can be supplied by a driving ECL component or from a spare ECL gate (**Fig.** 4a). The VBB input not only simplifies the user's design but also removes the element of error due to variations in PicoLogic device input threshold, since each device will be uniquely internally compen-

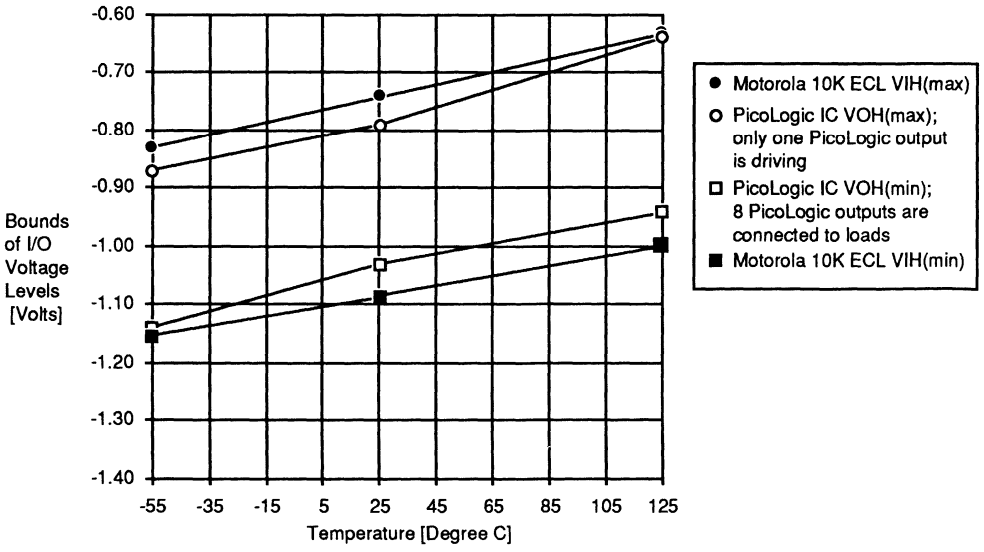


Figure 3. Temperature variation of voltages at the PicoLogic to ECL interface using the scheme of Fig. 2d. VIH (max) and VIH (min) curves of 10KH and Fairchild 10K (not shown) are located outside the top and bottom curves respectively.

sated to cause its threshold to match the VBB used as a standard reference. Obviously, it is impossible to compensate for the variations caused by processing, temperature or voltage gradients within a given ECL family.

VBB can be derived as shown in **Figure 4a**, or it may be obtained from one of the ECL differential input parts which have a VBB supply on an output pin, such as the 100114, 10125, 10114, 10115, 10116, and their military temperature range counterparts. Connecting this supply to the PicoLogic IC's VBB input will precisely match the input threshold of each PicoLogic part to the ECL family from which the VBB was derived.

The addition of the VBB input circuit to current generation PicoLogic devices has resulted in full ECL input compatibility. All PicoLogic process variables, and the effects of temperature and power supply (e.g. VSS) variation for both the PicoLogic and interfacing ECL family, are compensated by this scheme. Only those variations within the ECL family which cause the threshold to vary from part to part, and second order effects within the PicoLogic and ECL families, will detract from ECL to PicoLogic noise margins.

In order to easily upgrade from older generation PicoLogic devices (with VTRIM) to current devices (with VBB), provision should be made on printed circuit board layouts to permit jumpering from the ECL generated VBB to the pin of the PicoLogic IC now labeled VBB. VBB must be connected to the on-chip generated VBBS (nom. -1.3V) reference output when a PicoLogic device is driven by another PicoLogic IC.

2. ECL Threshold Tracking with First Generation PicoLogic

In the earliest CDFL designs, a different scheme was used to allow ECL threshold tracking. There, a supplementary ECL and PicoLogic device would establish their respective thresholds by negative feedback as illustrated in **Figure 4b**. An error amplifier samples these two thresholds and applies a bias to VTRIM of sufficient magnitude to cause the PicoLogic IC threshold to approach that of the ECL. The same VTRIM voltage would be applied to all PicoLogic devices being driven by that ECL family operating under the same environmental and power supply conditions.

The nominal threshold of the PicoLogic family may be

Table 6. Typical parameter variations* in ECL and PicoLogic devices

VOLTAGE	MECL 10KH	MECL 10K™	F10K™	MECL III™	F100K™	PICOLOGIC
ΔVOH / ΔVEE	- .008 V / V	.016 V / V	+ .016 V /V	-	NE **	NE
ΔVOL / ΔVEE	+ .020	.250	.016	.270	+ .030	NE
ΔVth / ΔVEE	+ .010	+ .148	+ .025	.140	+ .025	NE
ΔVth / ΔVSS	N / A ***	N / A	N / A	N / A	N / A	- .04
ΔVBSS****/ΔVSS	N / A	N / A	N / A	N / A	N / A	+ .18
ΔVOH / Δt	+ 1.3 mV /°C	1.3 mV /°C	1.6 mV /°C	-	.060 mV /°C	- .47 mV /°C
ΔVOL / Δt	+ 0.4	+ .5	+ .54	-	.100	+ .83
ΔVth / Δt	+ 1.0	+ 1.0	+ 1.1	-	.080	- .29
ΔVBBS / Δt	+ 1.67	+ .92	NE	+ .83	NE	+ .73

* The variation of the parameters in the denominators is within the nominal range of these parameters for each device. Also, ΔVOH/ΔVSS and ΔVOL/ΔVSS for the PicoLogic device family is negligibly small.
** NE: Negligable effect, i.e. less than .01 V/V or less than 0.1 mV/°C
*** N/A: Not applicable
**** VBBS in PicoLogic is functionally equivalent to the VBB output in ECL ICs that have a VBB reference output.

MECL 10K and MECL III are trademarks of Motorola, Inc.
F10K and F100K are trademarks of Fairchild Camera and Instrument Corp.

somewhat more positive than that of ECL, hence, the voltage applied to the VTRIM pin may have to be more negative than -5.2V to provide compensation. This imposes the requirement that the operational amplifier which provides the error signal (VTRIM), have a negative rail sufficiently negative to permit the Op Amp's output excursion to reach - 6.8V in extreme cases. The VTRIM current for each device should be less than 50 μA, permitting the use of any operational amplifier unless several PicoLogic devices must be compensated. It should be noted that only those PicoLogic devices being driven from ECL need to have this VTRIM input supplied, and the signal should be uniquely developed for each different ECL family under any given set of operating and environmental conditions.

Figure 4b illustrates the principle of VTRIM operation,

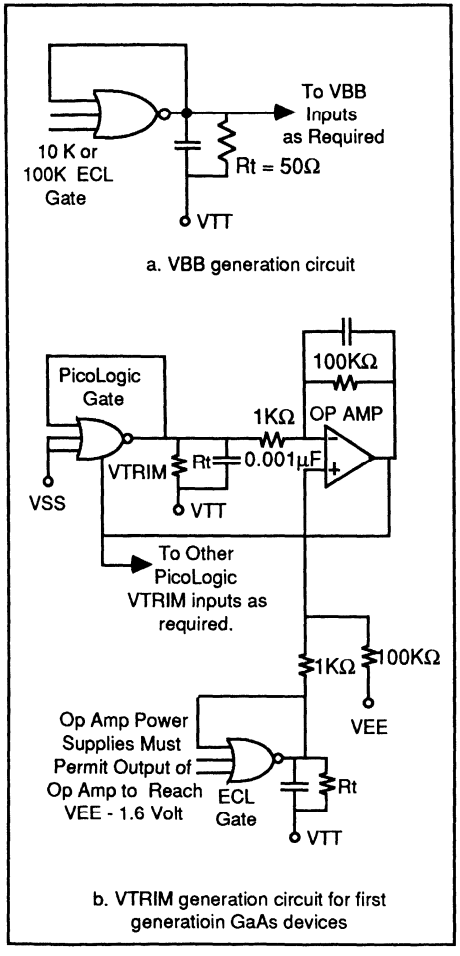


FIGURE 4. ECL threshold tracking circuit

employing both an ECL and PicoLogic NOR gate. Since both the ECL and GaAs components are biased at threshold, caution must be exercised to eliminate oscillations. At these frequencies, board layout and stray inductances and capacitances become very significant, and empirical techniques may be required to eliminate oscillations, although generally a 1,000 pf chip capacitor at the output of each device connected to VTT will suffice. An alternate scheme would employ a capacitor between input and output.

The VTRIM circuit provides a first order correction between the PicoLogic family and a given ECL family. Threshold variations between other PicoLogic family members and the parts used for generating VTRIM within either family, will provide a second order error which will not be corrected. To simplify system design for users of PicoLogic IC's, the VTRIM input has been replaced with a VBB input for new designs. The following parts were originally designed with VTRIM: 10G000, 10G011, 10G012, 10G060, 10G065, 10G070. To facilitate identification of those parts which have been redesigned to incorporate the VBB input, an "A" suffix has been added to the main part number prior to the dash number designating speed, e.g. 10G011A-4. The deployment of the VBB input instead of the VTRIM input obviates the requirement for the operational amplifier, the additional PicoLogic part and associated passive components and provides better overall performance.

C. PicoLogic IC Driving TTL/CMOS ICs

One of the interesting features of PicoLogic IC's is their relative ease of interfacing to TTL or CMOS circuits. Tolerance to large input swings permits a direct resistor divider type of interfacing from TTL outputs to PicoLogic IC inputs and the electrical symmetry of the output transistor permits direct driving of TTL or CMOS inputs from PicoLogic outputs. Two different types of interfacing to TTL/CMOS will be discussed:

- PicoLogic device operating at standard ECL levels with ECL supplies;

- PicoLogic device operating from TTL power supplies.

As previously mentioned, MESFETs employed in GigaBit's circuits are symmetrical in nature, meaning that drain (VDDO) and source (output) connections can be reversed or interchanged. Driving TTL from PicoLogic outputs capitalizes on this fact; the output MESFET can conduct current in either direction. If the polarity of VTT is reversed, the source follower becomes a common source with the output becoming the drain of the transistor. This provides voltage gain and inversion at the output stage.

1. PicoLogic Device Operating with ECL Supplies

Figures 5a and **6a** demonstrate the conventional con-

figuration used for driving TTL from PicoLogic outputs. As can be seen from **Figure 6a**, VDDO remains at ground potential, however the value of the load resistor is greatly increased (no longer serving as a ZO matching termination resistor due to its high value) and it is returned to the +5V TTL VCC supply. As the voltage on the output source follower gate transitions to the high state (Vgs≈ -0.2V) the output transistor will turn on, sinking nearly 5mA as required to pull the output to a VOL of a maximum of 0.5V. A close examination of this circuit reveals that any capacity C, on the output will result in a long exponential rise time governed by this R and C. This may be objectionable for some applications where a more rapid rise time, or nearly equal rise and fall times are required. See **Figure 6b** for the output waveform shape with a 1KΩ pullup resistor and the capacity of a TTL input connected to the output of a PicoLogic device. Note the exceptionally fast fall time as the output transistor turns on. This may also cause ringing on the negative transistion due to the improper termination of the line with the high negative $\Delta V/\Delta t$ edge rate. If either ringing on the falling edge or the slow rise time is troublesome, an alternative connection is possible which remedies these deficiencies. A smaller value load resistor may be used if VDDO is taken to a slightly negative voltage (≈ - 0.5V). This negative supply must be able to sink the output current, so it could be supplied from a negative voltage regulator. This may be implemented by the VDDO supply shown in **Figure 5a**. Two Si diodes can be connected which will bias the VDDO pin to approximately -0.5V. Biasing VDDO negative in this fashion permits the load resistor to be decreased in value to 100Ω and still assures that VOL does not exceed 0.4V.

Negative biasing of VDDO facilitates the use of a low value load resistor in two fashions: a) forward biasing the gate of the output transistor and b) permitting a greater drop(Vds) across it without exceeding the VIL requirements of TTL.

Since the gate voltage will normally approximate -0.2V in the high state there will be a forward Vgs bias of -0.2 - (-0.5) =+0.3V in this case thus increasing the available drain current. The characteristic curves of the output MESFET appear as shown in **Figure 7**. From these curves it may be seen that the VDS voltage would be approximately 0.4V under these conditions with a 100Ω load. Since VDDO is biased at -0.5V, VOL will be -0.5-(-0.4) or -0.1V, certainly a good logical low for TTL, while not being sufficiently low to possibly turn on some parasitic PNP's known to exist particularly in LS parts.

Obviously parameters may vary within the circuit, and this will cause the output level to vary correspondingly. The primary variation which will cause output level changes when the output is in the ON state is the variation in MESFET pinchoff voltage. If this variation is limited to ±200mV, then a first order approximation of the outputs may be taken to be represented by transitioning to either of the adjacent Vgs curves. This would correspond to Vgs equal to +0.4 or +0.0V resulting in a -0.3 or +0.1V VOL respectively.

2. PicoLogic IC's Operating from TTL Supplies

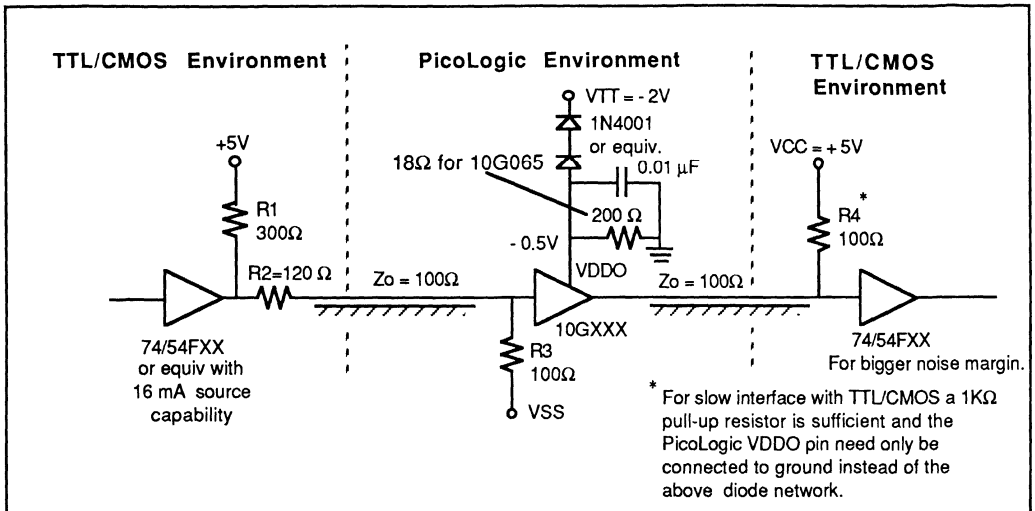
The power supply options shown in **Table 3** illustrate that positive supplies may be used to power PicoLogic devices. Although this simplifies the power requirements when interfacing to TTL or CMOS families, it somewhat complicates the logical interface. The TTL to PicoLogic interface remains a simple voltage divider as shown in **Figure 5b**. For R1 = 100 and R2 = 60 - 68 Ω, the VIH and VIL requirements of PicoLogic devices will be fulfilled. In the case of PicoLogic IC's driving TTL circuits however, an active circuit is required to translate the output levels. This circuit uses a single PNP transistor such as a 2N3906. The only concern using this approach is that the resistor R6 must sink the IIL of the TTL device and the voltage of the logical low state must not exceed the VIL(max). This may be readily accomplished when driving a single device if R6 is ≤ 400Ω for all TTL families. If LSTTL family is used, this value could be as high as 1KΩ; for FAST™[1] it could be as large as 800 Ω. The value of R3 is not critical, and should approximate 1KΩ unless a lower value is desirable to match the transmission line. The diode-resistor network can be used to bias the bases of several different transistors level translators on one printed circuit board.

D. TTL/CMOS Driving PicoLogic IC's

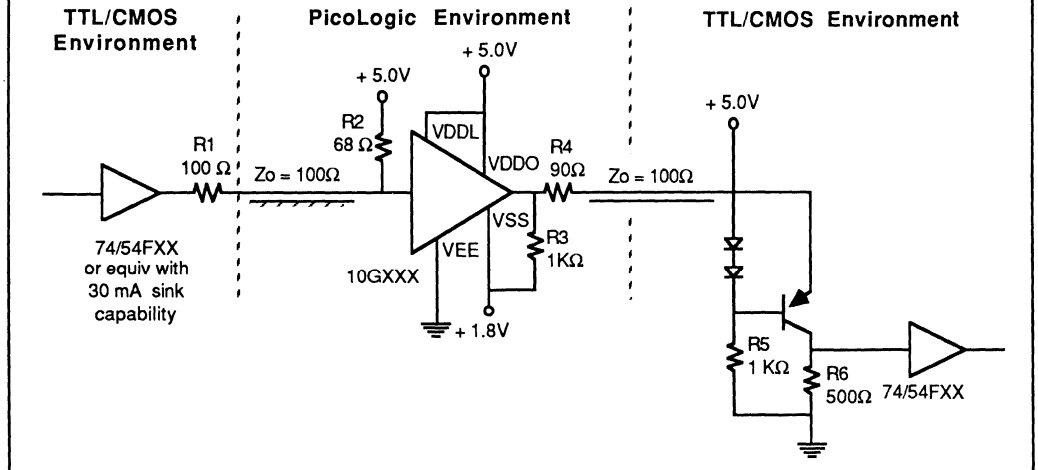
Due to the tolerance of PicoLogic IC inputs to large amplitude signals, it is possible to directly drive them from TTL or CMOS outputs through a resistor voltage divider. **Figures 5a** and 5b illustrate this feature. The resistor values must be selected such that the CMOS or TTL part has sufficient sinking or sourcing capability to drive this load. Minimizing impedances will assure the highest performance and also more nearly match the characteristic impedance of the connecting trace. The pull-up resistor to +5V (VCC) may not be eliminated even if the sourcing capability of the TTL or CMOS is adequate to drive the resistor divider to VSS. The reason for this is that when the TTL/CMOS output is low, the part has no capability to source current, hence, its output may actually be pulled below ground, possibly causing parasitic transistors to be turned on which could cause either a destructive latch up in certain CMOS devices, or prevent the output from going high in other cases. For this reason, even if the TTL or CMOS driving device can source sufficient current in the high state, the value of the pull up resistor R1 should be a maximum of 1.4 times the sum of R2 and R3. The minimum value would be determined by the TTL or CMOS IOL considering the current being sunk by R2 and R3. In general, the values given in the schematic are appropriate for FAST driving PicoLogic devices. Considering the output high characteristics of FAST, the swings present at the PicoLogic device inputs would be VIL ≥ - 0.7V and VOL ≤ -1.7V.

Note that this scheme employs source termination to

[1] FAST is a trademark of Fairchild Camera and Instruments Co.



a. Fast interface with TTL/CMOS when PicoLogic is at ECL levels



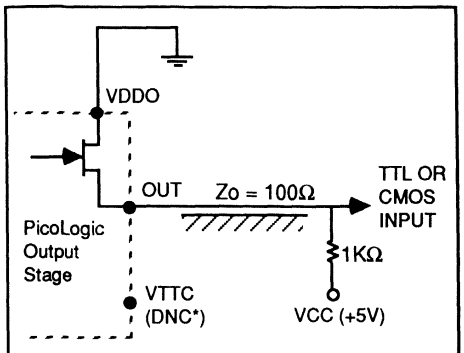
b. Interface with TTL/CMOS when PicoLogic supplies are at TTL levels

FIGURE 5. Interfacing between PicoLogic and TTL or CMOS devices

conserve power with the output impedance of the PicoLogic device (≈10Ω) plus R4 matching the Zo. Note that R3 is returned to VSS to insure that the output stage is always on to maintain this relatively constant output impedance. This common base configuration eliminates the Miller effect on the transistor's performance thereby greatly improving switching times. Speed will of course be limited by the ft of the transistor employed.

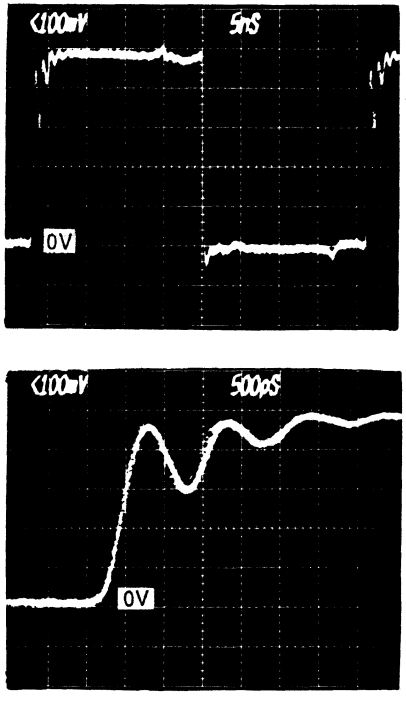
V. SUMMARY

In this note we have shown the flexible alternatives that the design engineer has when interfacing the PicoLogic family of GaAs IC's to other logic families. To provide a concise reference, the key points are summarized below:



* Do Not Connect

a. Low current output interface to TTL or CMOS



b. PicoLogic output waveforms

Figure 6. PicoLogic to TTL/CMOS interfacing circuit and a generated sample waveform (vertical scale: 1.0V/division)

A. Unused logic inputs may be tied directly to VDDL for logic high or VTT or VSS for logic low state. They should not be left open. This contrasts with ECL whose inputs may be left open or tied to any negative rail, but may not be tied to ground as a logic high, due to the ECL saturation problem discussed in section **IV-A.**

B. PicoLogic's VBB pin should be connected to one of the following:

1. The on-chip VBBS reference if the input signal is derived from another PicoLogic or NanoRam device, or from other large amplitude signal sources which provide a minimum VIH of -0.8 and a maximum VOH of -1.8 volts. Examples might consist of other GaAs devices, VCO's, and TTL or CMOS with resistor-divider drives.

2. An ECL derived threshold signal, VBB, for any devices driven from that ECL family. (See **Fig. 4a**).

C. Different inputs of the same PicoLogic IC should not be driven from two different ECL families lacking compatibility (e.g., 10K and 100K) except over the temperature range of 20 to 45°C.

D. The following pins (when available) should be left open if not needed: VTRIM, VDCH*, VDCL, VLCH*, VLCL, VICH* and VICL (VDCH must be tied to VDDO when not used). If external supplies are used then all supplies indicated with an asterisk must be current sinking (negative) supplies. All others must be current sourcing (positive). For large input signals it is desirable to connect VICH and VICL to -1.3 volts if these pins are provided.

E. The TTL output configuration results in a logical inversion.

F. If it is necessary to restrict VOH when driving ECL use the scheme illustrated in **Figure 2c** when driving 100K and **Figure 2d** when driving 10K or 10KH.

G. The output stage is an on-off switch to the VDDO pin. This dictates that a pull-up or pull-down resistor must be employed to achieve output signals.

VI. CONCLUSION

The PicoLogic family of ultra-fast GaAs logic IC's provides speeds 3-5 times faster than existing ECL. Straightforward interfacing to other logic families permits the use of PicoLogic IC's for the most speed critical paths of a design, thus eliminating bottlenecks which limit overall system performance. Attention to high speed interconnect techniques and the information presented in this note will permit ready application of these products whether interfacing with other PicoLogic or NanoRam products or with other logic families.

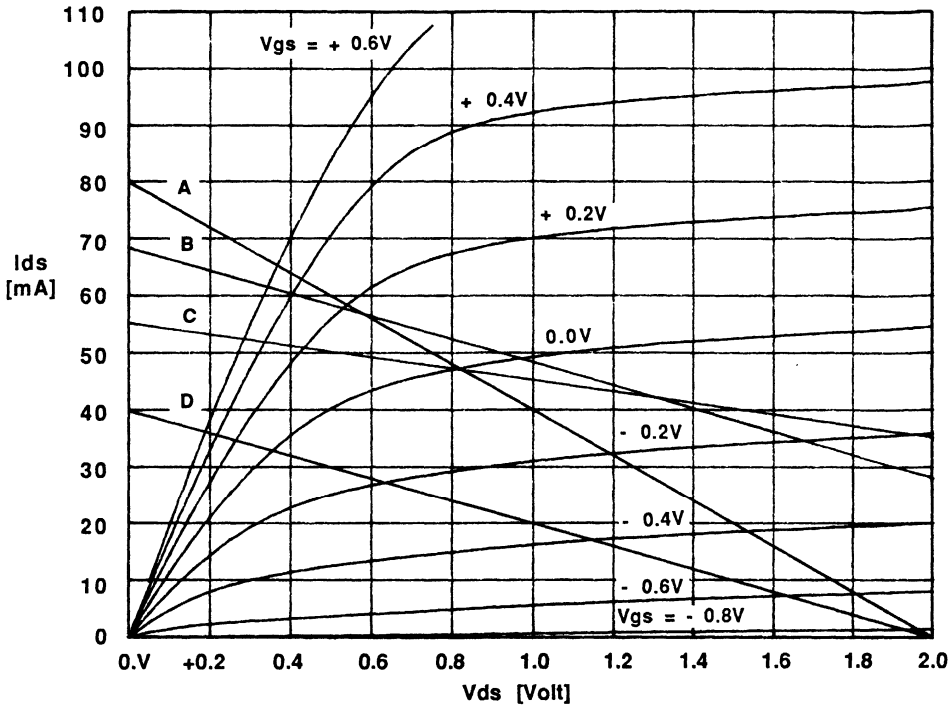


Figure 7. Output transistor current-voltage characteristics and different load lines; (A) 25Ω terminated to - 2.0V, (B) 50Ω terminated to - 3.4V, (C) 100Ω to + 5.0V with VDDO pin connected to - 0.5V, (D) 50Ω to - 2.0V. The load lines are derived with output clamp (VDCH) pin unconnected.

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Guidelines for the Use of the 12G014 400 MHz Registered RAM

Application Note #5 By: Carl Eggert Deierling

I. INTRODUCTION

Memory speed is a frequent bottleneck encountered in the design of high performance systems. The traditional von Neumann architecture requires the sharing of memory between data and instructions. RISC architectures compound the problem by their very nature; simple encoding of machine level instructions requires a greater number of instructions to perform a given function. RISC multiprocessors improve performance by sharing memory between N processors, but this necessitates N times the memory bandwidth of a single processor. Small, high speed cache memories can be used to supplement main memory in computer systems accelerating the slow speed of high density main memory. In addition to computer cache or cache tag memory, DSP, DRFM, video, communications, radar and numerous other applications require high bandwidth memories.

Thruput, whether it's measured in MIPS, MOPS, MFLOPS, Whetstones, Dhrystones, LINPACK rates, Livermore Loops, or in one customer's unique and humorous unit - LOCH (Library of Congress per Hour) - is always a term expressed as frequency, not delay. This is a key point to note. **Cycle Time in a RAM is generally the speed limiting parameter in high speed memory subsystems, not access time.** Despite this, most high speed SRAMs have been designed and specified with access time as the dominant speed specification. Access time is a more pertinent parameter when memory speed is several tens of nanoseconds, and system timing hinges on the access time of the RAMs. However, very fast (sub-10ns) RAMs are typically employed by design engineers with external registers at the inputs and outputs to minimize skew problems, even though these registers increase access time by a factor of at least two. The clocking frequencies and timing of these registers become key system considerations, requiring a cycle time specification. While external registers can be used to reduce memory subsystem speed bottlenecks, an even greater benefit to system performance can be derived if the input and output registers appear on the RAM itself. This will be shown to yield memory subsystem performance nearly equaling the performance of the individual registered RAM itself.

The 12G014 NanoRam™ is a GaAs 256 x 4-bit ECL compatible registered (pipelined) RAM with a 2.5 ns cycle time. This note describes how the 12G014 is used in an example 1K X 16-bit memory subsystem design to achieve performance determined by the RAM itself, and not by peripheral circuitry or board design.

II. ARCHITECTURE AND FEATURES

The logic diagram of the 12G014 is shown in Figure 1. Inputs which differentiate this RAM from a conventional static RAM are the differential Clock inputs and the Write Enable input (as opposed to a narrow write pulse input). DATA and Write Enable for the write mode, and Address and Chip Enable for both read and write modes, are all loaded into the input registers on the rising edge of the +Clock input. This edge of the clock also initiates the internal Write Pulse generation if Write Enable is active, circumventing the problem associated with propagating a narrow write pulse around a board, as required by conventional (non self-timed) SRAMs. The 12G014 is static in the sense that the CLK is not required to maintain stored data.

The CLK input also clocks the output registers, which operate in one of three different modes controlled by strapping the MODE pin to the appropriate supply voltage. In Latch Mode, the slave is always transparent, hence the entire flip flop becomes transparent on the falling edge of the clock as the master becomes transparent, and maintains data during the

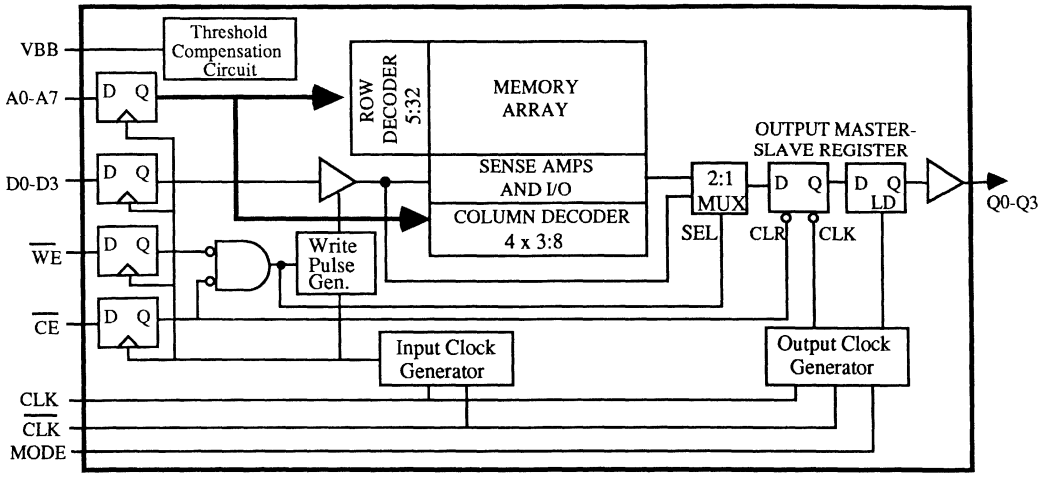


FIGURE 1. 12G014 Block Diagram

time when the clock is positive. In Transparent Mode (most similar to a conventional SRAM's architecture) both master and slave output registers are held transparent and read data is propagated to the output as rapidly as it is sensed. Latch and Transparent modes permit faster access times for those cases where system cycle time is longer than the 2.5 ns capability of the 12G014. Since the four output data bits must propagate through the output master/slave flip flops, even if held transparent, access time is increased from 1.5 to 3.8 ns. However, the additional delay incurred by adding registers to the input and output is returned several times over in a systems application by enabling a 2.5 ns system cycle time. In Register Mode, the output (slave) stage of the master/slave flipflop is loaded (latched) on the positive transition of the clock following the clock which loaded the input registers. In this mode, the data output is stable for the maximum duration; a critical parameter when reading RAM to achieve maximum performance. Register mode is preferred for most applications since it provides the fastest cycle time, and is the focus of the following discussion.

Two additional architectural features should be noted with respect to the output stage. With reference to the 12G014 block diagram (Fig 1), the data inputs D0-D3 are multiplexed to the output pins during a write operation, and will appear at the output with identical timing characteristics as though a read operation transpired. This does not provide inherent write-verify capability. The 12G014's write cycle time is identical to the read cycle time, considerably simplifying system design and is of obvious benefit if high speed writing is required. The second feature is the scheme by which the outputs are disabled as the chip enable goes low. Since the data appears at the output in response to the clock following the one which loaded the appropriate address and chip enable, the output must remain enabled even if the chip enable has gone high during the previous cycle. This is accomplished by virtue of the fact that the Chip Enable is actually a synchronous reset to the output register. After chip enable goes high to deselect the RAM, two rising clock edges must occur before the outputs are disabled in register mode. This permits conventional wire-ORing of the outputs with consistent data access across chip address boundaries.

One other DC input, VBB, plays a key role when the 12G014 is driven from ECL. This input establishes the input threshold voltage for all signal

inputs, thereby insuring that the RAM may be driven from any ECL logic family including 10K, 10KH, 100K, 10E, 100E or even older ECL families. Application Note 4 "Interfacing PicoLogic™ and NanoRam™ ICs to Other Logic Families" should be reviewed for an understanding of how VBB is used to allow the 12G014 to interface with other high speed logic families.

Figure 2 lists some of the salient features of the 12G014 with a corresponding list of benefits which may be ascribed to each. A review of this chart will yield rapid comprehension of the architecture and its advantages.

III. HIGH SPEED MEMORY SYSTEM DESIGN CONSIDERATIONS

Skew is the culprit militating against achieving system performance approaching that of the memory. Known skews may be eliminated by adding fixed delays (meander traces) in the faster paths to equalize the delay of slower paths; common practice for high speed logic designs. The subset of skew which limits performance in high speed logic designs is that delay which is either not defined, or variable between devices or with changing environmental conditions, thus preventing its cancellation as discussed above. For purposes of this discussion, this subset of skew wil be refered to as "indeterminate skew".

Minimization of performance limiting indeterminate skew can be accomplished in several fashions. Reducing propagation delay through a part will also reduce the variation in delay through the part. Therefore, faster components should be used to implement the speed critical paths in a design. These parts must be specified for a tight range between minimum and

FIGURE 2. 12G014 NANORAM™ MEMORY CAPABILITIES

FEATURES	BENEFITS
• Equal Read and Write Cycle Times	• Simplified System Design and High Speed Write
• Pipelined Architecture	• Maximizes System Performance
• 256 x 4 Configuration	• Ideal for Cache, Mail Box, Register File Scratch Pad, FIFO, or Buffer Memory
• Selectable Registered, Latched, or Transparent Output Modes	• Cycle or Access Times May be Optimized for Application
• Single Ended or Differential Clock	• Minimizes Clock Noise and Skew and Facilitates Interleaved Access
• Large Source Follower Outputs	• Capability to Wire-OR and drive a 50Ω Bus Terminated at Each End
• Internal Timing Generators Including Write Pulse	• Obviates Propagating Narrow Pulse Maximizes Subsystem Bandwidth
• Miniature Packages	• High Density Surface Mount Enhances System Performance
• First Member of NanoRam Family	• Pin Compatible Migration Path to Higher Densities

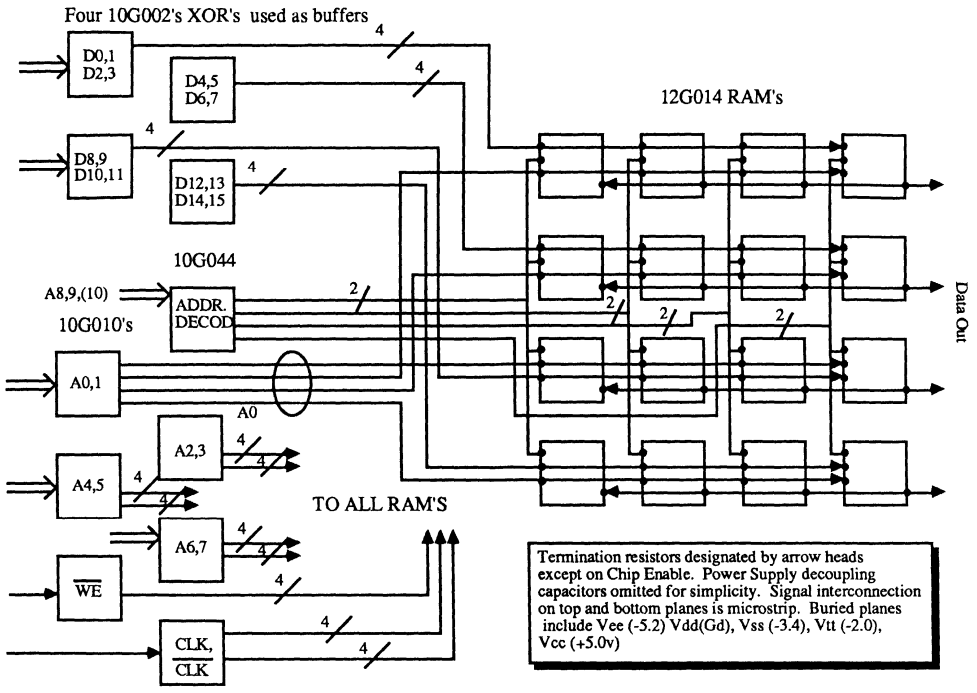


FIGURE 3. 1K X 16 Ram Board Block Diagram

maximum delays. AC characteristics over the temperature range of concern must also be specified. Furthermore, parts designed specifically for low skew such as fanout buffers (drivers with most logic common, but with multiple parallel outputs), may be placed in all parallel critical paths. Despite all precautions, the accumulated T_{dmax} - T_{dmin} (indeterminate skew) of components will eventually result in an unacceptably large number. For this reason, pipelining is used to reclock all signals into a register after propagating through a number of logic elements. This technique re-establishes a time base with the only remaining indeterminate skew being that of the register's clock-to-output delay difference and uncompensated PC board differences. Incorporating registers on the 12G014 at both inputs and outputs further minimizes these effects. The delay uncertainty of the on-chip registers is much less than the equivalent skew of external registers.

Any sequential part, which includes RAMs whether registered or not, possesses setup and hold times which impose an additional upper performance limit. A sequential device must have its inputs stable for a minimum period defined by the maximum of the sum of the setup and hold times. If the clock or other inputs cannot be precisely defined in time due to skew, this additional temporal uncertainty must be added to the sum of the setup and hold times to determine the system upper limit of cycle time performance. In the case of a RAM subsystem, if the sum of these times exceeds the cycle time of the RAM, they will dominate and the RAM can not be used to its full potential.

The block diagram for a 16K RAM board which was developed at GigaBit Logic appears as Figure 3. As shown, the board is configured as a 1K x 16 array. Optionally it can be configured as a 2K x 8 array. The interfacing IC's used in this design were

FIGURE 4. 16K RAM Board

four 10G002 Quad XOR Gates to buffer the 16 data bits, the 10G044 3:8 or Dual 2:4 Decoder for decoding higher order address bits and providing Chip Enables, and four 10G010 Dual 2:1 Multiplexing Fanout Buffers for driving the eight address lines. One-half 10G010 is also used for buffering Write Enable, and one is used to generate the complement of the clock and buffer the clock and its complement to all of the RAMs.

A photo of the completed board is shown in Figure 4. This board is a seven layer glass epoxy board with microstrip signals on the top and bottom layers. The five buried layers provide power planes to distribute V_{DD}, V_{SS}, V_{EE}, V_{CC}, and V_{TT}. The distribution of most signals is quite simple; a simple daisy chain from left to right, much as is shown in the Block Diagram, serves for the Addresses, Data Inputs, and Write Enables, since the signal pins are on the sides of the chip. These horizontal traces appear on the bottom plane of the board, and as can be seen from the photograph, several meander lines are present on the top plane of the board to equalize the delays between the various outputs and the different rows of RAMs. As the signals propagate from left to right through each of the four columns, they are delayed by 180ps for each column. For this reason, the Output from the first column of RAMs will appear 180 ps before the second and so on. However, since the board outputs are located on the right edge of the board, the first column must propagate past the remaining three columns, hence its output is delayed by this same 180 ps per column. Thus the data from all four columns of RAMs appear at the output connector simultaneously.

The Clocks and Outputs are somewhat more difficult to daisy chain, since the connections are on the top and bottom edge of the IC respectively. At GaAs edge rates of approximately 6 volts per ns, representing a rise and fall time of 150 to 200 ps between 20 and 80% points, stub lengths must be maintained at less than 0.4 inches as an absolute maximum. Since the

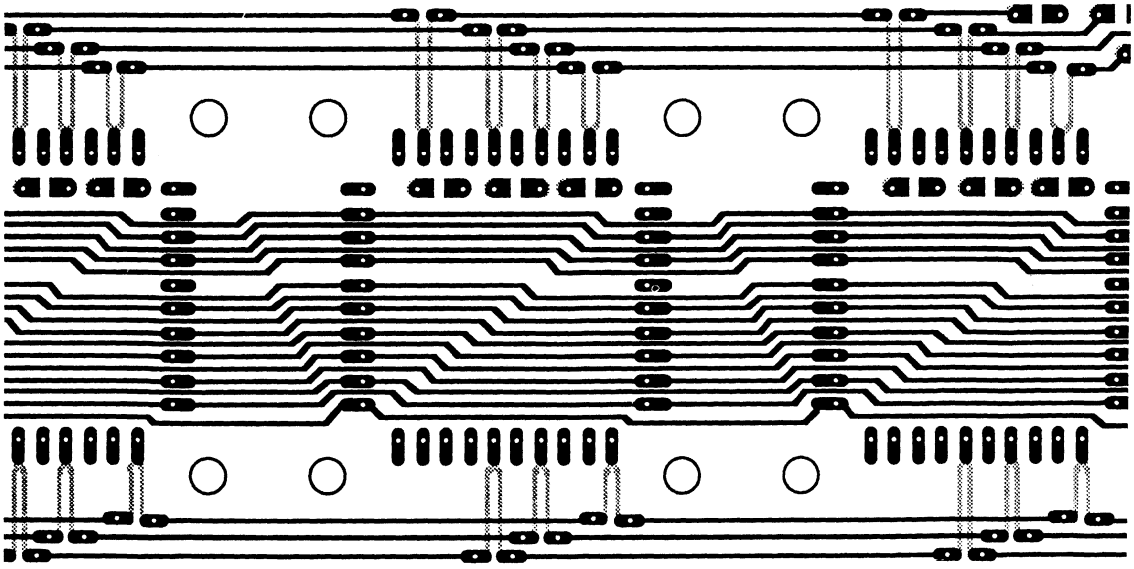


FIGURE 5. RAM Board Daisy-Chaining

outputs of four RAMs are bused, the board is layed out with "U"s making contact to the Outputs and CLK inputs as shown in Figure 5 to avoid stubs. The power planes are defined briefly in Figure 3, however a much more comprehensive discussion of board design, power planes, decoupling, termination, microstrip, strip lines and stubs may be found in GigaBit Logic Application Note 2 "Guidelines For The Use of Digital GaAs ICs". It should be noted that the Outputs must be terminated at both the right and left ends of the bus. This presents no problem since the entire PicoLogic™ and NanoRam families have sufficient drive capability to assure meeting VOH requirements even when driving 25 . Termination resistors are provided on the left end of the bus and the right end goes to a high quality mass termination connector and cable assembly which must be terminated at the destination. Ceramic chip capacitors and chip resistors are located on the bottom of the board, although in most cases they could have been located on the top as well. Each supply pin is decoupled at each device to the appropriate power plane to supplement the package internal power decoupling capacitors. Although this board was hand soldered, surface mount techniques permit application of adhesive to passive components to be subsequently either wave or reflow soldered to the bottom of a board.

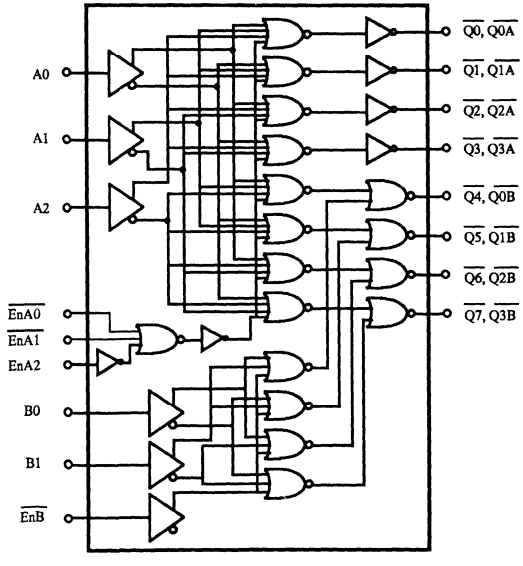


FIGURE 6. Logic Diagram of 10G044 Decoder

The Chip Enable signals derived from the 10G044 Decoder are handled uniquely. Each of these four signals must go to a column of RAMs. This was accomplished by locating the decoder midway between the top and bottom of the board, and using the duplicate halves driving through the middle of the array; one feeding the top two and the other feeding the bottom two RAMs in each column. In this manner, the maximum delay variation was equivalent to only a single chip center to center spacing (180 ps). If the decoder is configured as a 3:8 instead of a dual 2:4 decoder, the wiring on the output provides for a 2K X 8 configuration if the outputs of the upper and lower bytes are bused.

IV. TIMING ANALYSIS

For a detailed timing analysis refer to Figure 7, which shows all the high speed inputs to a single 12G014 RAM. Four different times have been identified. T1 is clock delay inherent in the 10G010 operating as a biphase generator/buffer. T2 is the data path delay due to any one of three different PicoLogic™ devices (10G010, 10G002 or 10G044). T3 is an intentional delay added in the clock line as required to position the clock in the middle of the 12G014 setup and hold time window with respect to the data. T4 is the clock period for the RAM: 2500 ps for the 12G014-2. The minimum and maximum delay for each of the parts is given for both 25°C and for 85°C case temperature. Although not shown, the delays of PicoLogic parts operating at 0°C are quite similar to 25°C operation, as shown in the relevant datasheets. At 85°C, maximum delays range between 50 and 100 ps longer than at 25°C. Since the 10G010 is used as a true and complement generator in the clock circuit, its delay is slightly longer than the same device used as the Address buffer (or for Write Enable), where the inputs go to Data input pins instead of the SEL inputs. It should be noted in this application that the slower -3 speed sort parts were used for all devices except the

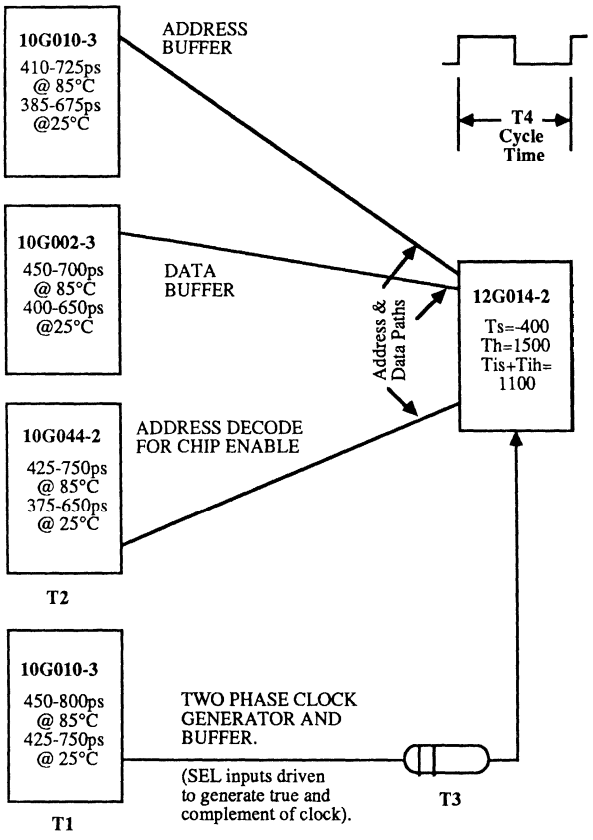


FIGURE 7. Memory Subsystem Timing Skews Over Temperature

10G044-2, which lacks a -3 slow sort part. It is also interesting to note that since even the RAM Chip Enable input is registered, it has the same timing as data, address or write enable inputs. This differs from conventional SRAMs which must have a much shorter Chip Enable time to allow the external decoder sufficient time to perform the decode function. In the case of the NanoRAM™, the 10G044 decoder delay time equals that of the driver delays for the other inputs, therefore RAM timing is equal for all inputs.

Figure 8 tabulates the calculations of setup and hold times which are provided by the peripheral PicoLogic™ parts for the RAM under worst case timing scenerios (based on the information contained in Figure 7) and compares these calculated values with those required by the 12G014 (Figure 9). Two system related times are defined: the System Setup Time (Tss), which is the setup time provided by the system, and System Hold Time (Tsh), which is the hold time provided by the system. It should be noted that board propagation times are omitted from these calculations, since they have been equalized in the board layout and will cancel. It is assumed that minimum RAM cycle time (2.5ns) is desired. The objective is to delay the clock by an amount (T3) which will cause the system margins for setup and hold times to be equal, thereby allowing for the maximum variations in delays due to loading and board propagation delay. Observe that the top two tables in Figure 8 give the setup and hold times for no additional clock delay (T3). It can be seen that for a given temperature, the least margin exists at 85°C: 100ps setup margin and 610ps hold margin for a total window of Tw (85°C) = 710ps. The ideal case would be to evenly divide this window between setup and hold times, by calculating the T3 delay from the equation derived below:

$$T3 = \frac{(Tss - Ts) + (Tsh - Th)}{2} - (Tss - Ts) = \frac{(Tsh - Th) - (Tss - Ts)}{2}$$

$$T3\ (85°C) = \frac{610 - 100}{2} = 255\ ps$$

Allowing for a board temperature gradient, the worst case analysis would be to assume that some components are at 25°C and others are at 85°C. Even with this unrealistic assumption it can be seen from Figure

CALCULATION OF SYSTEM SET-UP AND HOLD TIMES FOR 12G014 MEMORY SUBSYSTEM OPERATING AT 400MHZ (T4 = 2500PS)

SYSTEM SET-UP TIME CALCULATIONS WITH NO ADDITIONAL DELAY (T3 = 0)

Temp °C	Clock Delay (min) ps	Data/Addr Delay (max) ps	Delay Line Clk Delay ps	System Setup Time Provided ps	12G014 Setup Time Required ps	Setup Time Margin ps
	T1	T2	T3	Tss = T1+T3-T2	Ts	Tss - Ts
25	425	675	0	-250	-400	150
85	450	750	0	-300	-400	100
25-85	425	750	0	-325	-400	75

SYSTEM HOLD TIME CALCULATIONS WITH NO ADDITIONAL DELAY (T3 = 0)

Temp °C	Clock Delay (max) ps	Data/Addr Delay (min) ps	Delay Line Clk Delay ps	System Hold Time Provided ps	12G014 Hold Time Required ps	Hold Time Margin ps
	T1	T2	T3	Tsh = T2-T1-T3+T4	Th	Tsh-Th
25	750	375	0	2125	1500	625
85	800	410	0	2110	1500	610
25-85	800	375	0	2075	1500	575

SYSTEM SET-UP TIME CALCULATIONS WITH ADDITIONAL DELAY (T3 = 250PS)

Temp °C	Clock Delay (min) ps	Data/Addr Delay (max) ps	Delay Line Clk Delay ps	System Setup Time Provided ps	12G014 Setup Time Required ps	Setup Time Margin ps
	T1	T2	T3	Tss = T1+T3-T2	Ts	Tss - Ts
25	425	675	250	0	-400	400
85	450	750	250	-50	-400	350
25-85	425	750	250	-75	-400	325

SYSTEM HOLD TIME CALCULATIONS WITH ADDITIONAL DELAY (T3 = 250PS)

Temp °C	Clock Delay (max) ps	Data/Addr Delay (min) ps	Delay Line Clk Delay ps	System Hold Time Provided ps	12G014 Hold Time Required ps	Hold Time Margin ps
	T1	T2	T3	Tsh = T2-T1-T3+T4	Th	Tsh-Th
25	750	375	250	1850	1500	350
85	800	410	250	1860	1500	360
25-85	800	375	250	1825	1500	325

FIGURE 8.

8 that the total setup plus hold time window Tw(25-85°C) = 75 + 575 = 650ps. Application of the equation for T3 yields results similar to that for the 85°C condition.

$$T3\ (25\text{-}85°C) = \frac{575 - 75}{2} = 250\ ps$$

Using this value for T3, the bottom half of Figure 8 shows that setup and hold time margins are no worse than 325ps even with the assumption of a 60°C temperature gradient in the system. It should be noted that the actual T3 delay line was located at the input of the Clock Generator/Buffer, since only a single delay line was required to delay both phases of the clock. Where delays are not known apriori, provisions can be made on the board to accomodate a small length of coiled semirigid coax.

A factor which should not be overlooked is the timing effect of daisy chaining on inputs and bus driving at the outputs. As the input signals drive each RAM they encounter an input capacitance of ≈ 2 pf, mostly that of the package. Because of this capacitance, the signal is both delayed (Cin adds to the intrinsic Co of the line) and degraded in rise and fall times due to driving this C with a 50Ω line. Since the input threshold is approximately at the 50% point of the signal swing, both effects will increase delay. However, since all signals (except Chip Enable) undergo the same delays between columns, a good portion of this delay is deterministic, hence accountable for in the design. The decrease in edge rate is actually more of a problem than the increase in delay because it results in "indeterminate skew" due to threshold uncertainties. Likewise, the outputs are all bused and similar effects will cause reduced slew rates and incremental delays. A more detailed discussion of these factors and the background material necessary to estimate these additional delays is presented in Application Note 2. Overall, while these effects are real, they are nonlinear and result in reducing the setup and hold time margins by approximately 100 ps for the second device connected, and lesser amounts for each additional device connected. Degradation due to PC board losses should also not be ignored, where distances exceed one foot.

The duration of valid output data is a key

12G014-2 AC CHARACTERISTICS (NOTE 1)

Test Conds: Tc = 25°C to 85°C, Vcc = 4.75 to 5.25 V, Vss = -3.6 V to -3.2 V, Vee = -5.5 V to -4.9 V, Vddl = Vddo = Gnd.

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
REGISTER MODE READ AND WRITE CYCLES						
Tclkh	Clock High Pulse Width	1000			ps	
Tclkl	Clock Low Pulse Width	1000			ps	
Ts	Input Setup Time	-400			ps	2
Th	Input Hold Time	1500			ps	2
Tr,Tf	Output rise and fall times		175	250	ps	3
Trc	Read/Write Cycle Time	2500			ps	
Tar	Clock Rising Edge to Output Delay	800	1000	1200	ps	

NOTES:
1. AC test conditions, unless otherwise stated:
Vbb = -1.3 V, Rload = 50 Ω to Vtt = -2.0 V, Vih = -0.8 V, Vil = -1.8 V, edge rate all inputs = 400 ps measured between 20% and 80% points. All delays measured between 50% points of signal transmissions.
2. Measured from the rising edge of the clock input between 50% points.
3. Output rise and fall times are measured at the 20% and 80% points of the transition from Vol max. to Voh min.

FIGURE 9. 12G014-2 AC CHARACTERISTICS

consideration since some skew results from the busing as just described and in the output microstrip traces because they are U-shaped as depicted in Figure 5 and described earlier. Reference to the abbreviated 12G014-2 AC Characteristics in Figure 9 will provide all the information necessary to establish the output data valid time using just three parameters: Tar min, Tar max and Trc. If one considers an entire memory array, it becomes apparent that one RAM chip could exhibit the shortest clock to output delay while a second could exhibit the longest. Therefore, the leading edge of the access of the fastest could encroach on the trailing edge of the slowest, truncating the time during which the output is stable. This data stable time Tds = Trc -(Tar max - Tar min) = 2.1 ns. Herein lies the value of the register on the output. **The output data from all the RAMs in an array is stable and available for all but 400 ps of the 2.5ns cycle time** if other board related skews can be ignored. In actuality, 100 ps of input clock skew, 150 ps of board skew on the outputs and some degradation of output rise and fall times due to output busing, reduce the worst case Tds to greater than 1.7ns; still a long time for a 2.5 ns cycle time memory system.

Figure 10 is an example of a memory controller and array which could be implemented with PicoLogic™ and NanoRAM™ components by expanding the concepts discussed above and using several PicoLogic™ components in addition to those discussed.

V. CONCLUSION

Cycle time, not Access time must be viewed as the critical speed parameter in RAM subsystem design for most high speed applications. This requires that the cycle time be equal for both read and write modes, and that the RAM be operated in a pipeline fashion. Registered architectures now being designed into next generation RAMs such as the 12G014 permits achieving system performance nearly equal to the performance of the RAM itself. The problem of meeting setup and hold time requirements despite unavoidable skew between parts is minimized by incorporating the input pipeline registers directly on the RAM itself. Furthermore, on-chip output registers greatly simplify read timing since the outputs are stable for the majority of the cycle time. Conventional RAM architectures, based on non-registered approaches, place the bulk of the burden on the system designer to make the memory work in his system. On-chip input and output registers relieve the system designer from most of these considerations requiring only that interconnect path lengths are equalized at both inputs and outputs.

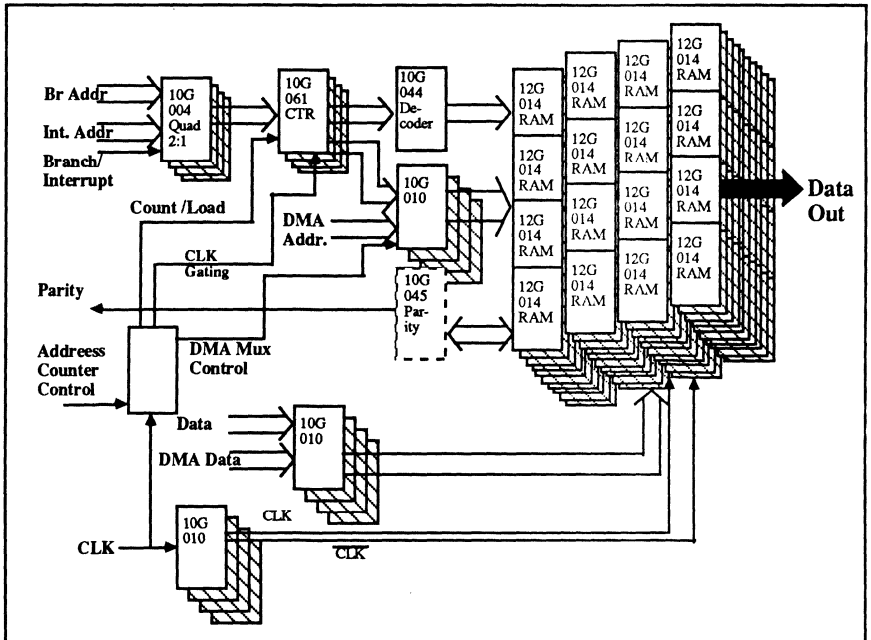


FIGURE 10. Memory Controller and Array

Guidelines for Using the 10G061 as a Universal Programmable Divider

Application Note #6 By: Mark Warlick

I. INTRODUCTION

This Application Note (AN-6) discusses and analyzes various schemes for configuring 10G061 Synchronous Counters as a universal programmable divider. The dividers recommended are continuous, i.e. have no illegal divide ratios, and the maximum number of divide ratios is given by $2^{4n} - 1$, where n is the number of stages used. The ability to divide by any continuous string of integers between x and y is especially important in frequency synthesis applications. The operation of the 10G061 and enhancing design techniques are delineated.

Proper use of the 10G061 requires a detailed understanding of its architecture and operation. When designing low noise frequency synthesizers using voltage controlled oscillators, high speed synchronous counters are needed to perform the ÷ N function. The availability of Gigahertz synchronous counters allows designers to use higher reference frequencies, thus keeping divide ratios low which in turn reduces phase noise. The 10G061 was designed to provide a solution to the design and development of high speed frequency synthesizers, and synchronous programmable dividers and counters. AN-6 will thoroughly discuss the operation and architecture of the device, and circuit implementations for using the device as a programmable divider.

II. 10G061 OPERATION

The block diagram of the 10G061 is shown in Fig. 1. The 10G061 is a fully synchronous, 4 stage

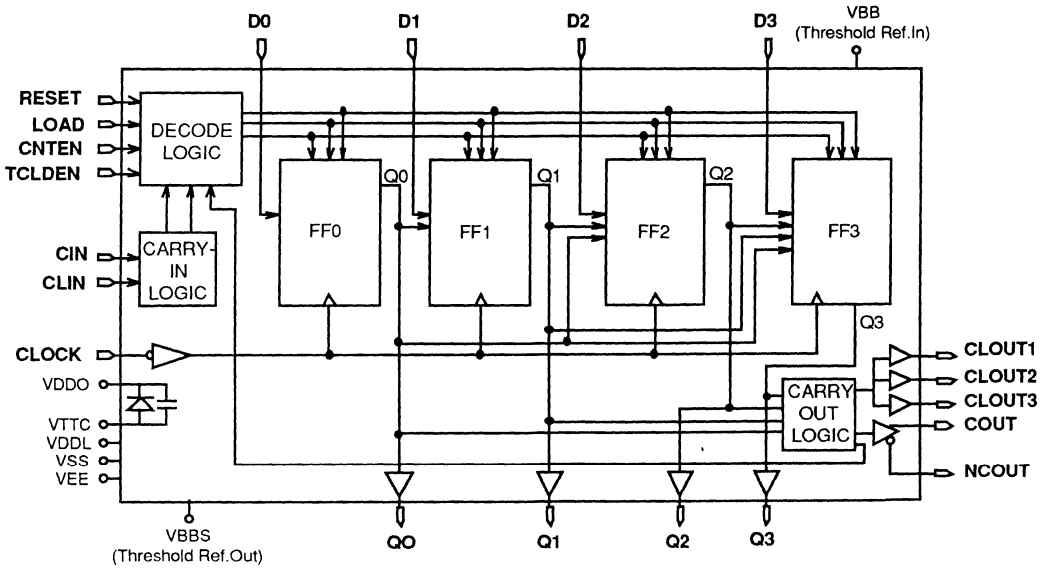


FIGURE 1. BLOCK DIAGRAM OF THE 10G061 SYNCHRONOUS COUNTER

TABLE A: 10G061 FUNCTION SELECT TABLE

FUNCTION	INPUTS							OUTPUTS		
	RESET	CNTEN	Cin	Clin	TCLDEN	Load	CLK	CLOUT	COUT	Q0 - Q3
RESET After the rising edge of the clock, all outputs are low.	1	X	X	X	X	X	∫	0	0	[Q0,Q1,Q2,Q3] = Lo
LOAD After rising clock edge, data on pins D0-D3 are loaded and appear at the outputs.	0	X	X	0	X	1	∫	$\overline{Q0}$•Q1•Q2•Q3	CIN•Q0•Q1•Q2•Q3	[Q0,Q1,Q2,Q3] $_{n+1}$ = [D0,D1,D2,D3]
FREE COUNTING/+16 Outputs advance their binary state on each rising clock edge.	0	1	X	X	0	0	∫	$\overline{Q0}$•Q1•Q2•Q3	CIN•Q0•Q1•Q2•Q3	[Q0,Q1,Q2,Q3] $_{n+1}$ = Next binary state
CASCADED COUNTING On 2nd rising clock edge, outputs start to advance their state.	0	0	1	⎍	0	0	∫	$\overline{Q0}$•Q1•Q2•Q3	CIN•Q0•Q1•Q2•Q3	[Q0,Q1,Q2,Q3] $_{n+2}$ = Next binary state
MODULO-2/15 DIVISION Counter repetitively cycles from ext. data binary state to 1111.	0	1	1	1	1	0	∫	$\overline{Q0}$•Q1•Q2•Q3	CIN•Q0•Q1•Q2•Q3	[Q0,Q1,Q2,Q3] $_{n+1}$ = Next binary state
MODULO-N PROG. DIV. The counter begins count at 2nd clock edge and cycles from ext. data binary state to TC (1111).	0	0	1	⎍	1	0	∫	$\overline{Q0}$•Q1•Q2•Q3	CIN•Q0•Q1•Q2•Q3	[Q0,Q1,Q2,Q3] $_{n+2}$ = Next binary state
COUNT DISABLE The counter is disabled. Outputs held at previous state.	0	0	0 X	X 0	X	0	∫	$\overline{Q0}$•Q1•Q2•Q3	CIN•Q0•Q1•Q2•Q3	[Q0,Q1,Q2,Q3] $_{n+1}$ = [Q0,Q1,Q2,Q3] $_{n}$

programmable up counter with all activity occuring on the positive edge of the clock. It supports speed enhancing functions such as carry-look-ahead and terminal count load enable (TCLDEN), which distinguishes it from other high speed counters. Table A summarizes the functions that the 10G061 is capable of executing.

The carry-look-ahead function greatly reduces the impact of interconnection delays by beginning the count enable process on the 14th count rather than the 15th count. This function also avoids the long delays involved with ripple propagating the carry-out to all stages as required when using counters without a carry look ahead function. Typically, CLOUT of the least significant stage drives the CLIN pins of the more significant stages. As the CLOUT of the least significant stage gets asserted on the 14th count, it sets the CARRY flip-flop of the more significant stages on the 15th count if the CIN signal is also asserted. In this manner, all more significant stages can be simultaneously prepared to count following the 15th count.

The Terminal Count Load Enable (TCLDEN) signal provides a speedy approach to parallel data loading. TCLDEN triggers a synchronous load, causing data on pins D(3:0) to be loaded into the counter on the next clock following terminal count. This signal, when asserted and decoded, enables the counter to load external data **if the CARRY flip-flop has been set** with CLIN and CIN on the appropriate clock cycles.

The synchronous RESET pin has the highest priority of all signals and forces the outputs to the zero state when high following the rising edge of the clock.

The LOAD command will parallel load data synchronously irrespective of the current count. Once the LOAD pin is asserted, the next rising clock edge will load external data D(3:0), which will then appear on the outputs. The LOAD signal has the second highest priority.

The CNTEN signal will enable the counter at anytime in the absence of LOAD or RESET signals.

Using the CNTEN, CIN and CLIN signals, several counting options are available (Table A).

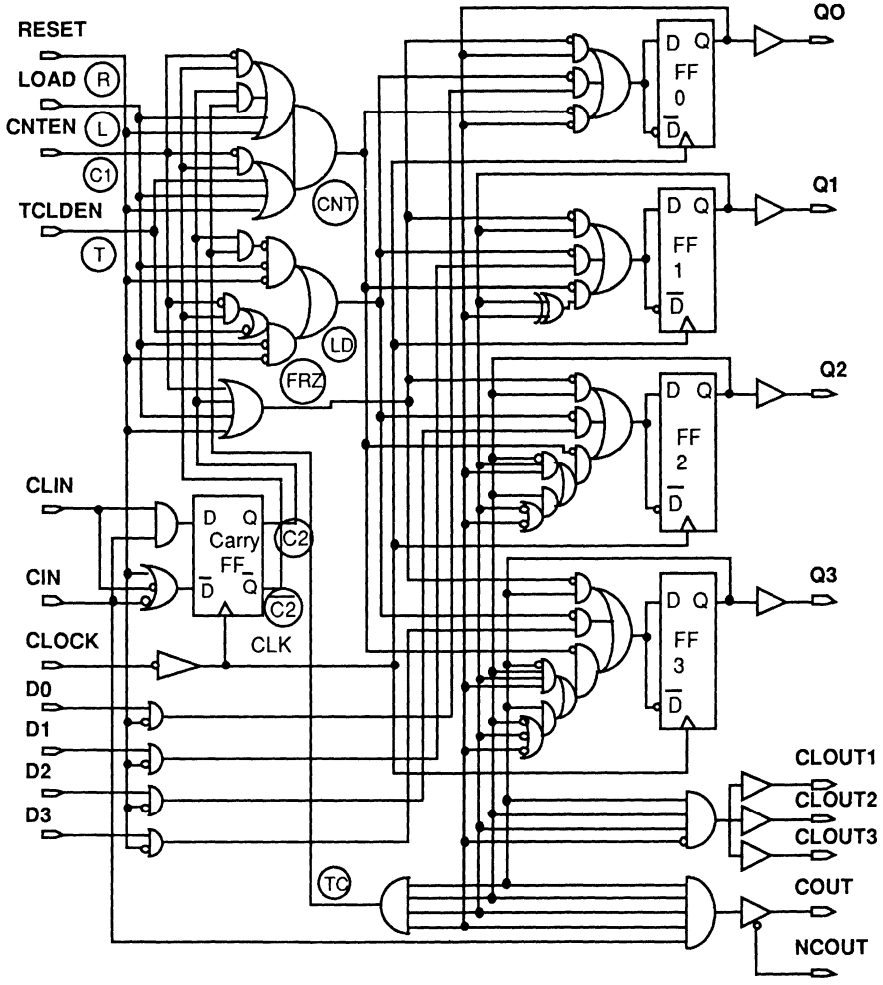
There are several subleties associated with this device not readily apparent. For example, the 10G061 can be programmed several ways to perform identical functions. It was stated earlier that the CLIN and CIN can jointly or the CNTEN can independently enable the counter. There are also several approches to loading external data into the counter. The LOAD and TCLDEN signals accomplish this task, though there are some differences in the operation of these signals. In general, the counter will load, count and freeze counting using the following equations:

$$CNT=[(R+\overline{C_1}\cdot\overline{C_2})+L+(TC\cdot C_2)]+\overline{[(R+(\overline{C_1}\cdot\overline{C_2})+T+L)]}$$

$$LD=[R+L+\overline{[(\overline{C_1}\cdot\overline{C_2})+\overline{T}]}]+\overline{[R+L+(TC\cdot C_2)]}$$

$$FRZ= R+L+C_1+C_2$$

FIGURE 2. 10G061 LOGIC DIAGRAM



where the signal names are shown in fig. 2.

Because of this flexibilty, some precautions must be taken to insure proper operation of the device. Note that the LOAD signal DOES NOT clear the carry flip-flop. In applications where the CLIN and CIN are used exclusively to enable the counter **and** the LOAD signal can be presented at any time, anomulous behavior can result. In particular, if a LOAD signal is presented simultaneously with CLIN, while CIN is also high, the counter will increment one count after the LOADed data appears on the outputs. This happens because the carry flip-flop is set by the coincident presence of CLIN and CIN, which causes an additional count enable signal on the following clock edge. In the more significant stages of an N-bit divider, this operation becomes particularly troublesome. Given the flexibility of the device, there are several approaches available to circumvent this behavior. A hardware solution would be to add an external inverter between the LOAD and CLIN pins. At the system level the designer can relax the requirement for an arbitrary LOAD and only load data at terminal count using TCLDEN.

SYSTEM DESIGN CONSIDERATIONS

In order to maximize the performance of the 10G061, clock skews must be miminized and actual pertinent device delays known. The performance data in Table B below supplements the information contained in the datasheet and is helpful for high performance system design.

TABLE B

Clock to Q (D3:0) - max. (Td)	1,150ps
Clock to NCOUT - max. (Td)	1,200ps
Clock to COUT - max. (Td)	1,050ps
Clock to CLOUT - max (Td)	1,150ps

In order to minimize skew, several precautions must be taken such as:

1. Minimize interconnect lengths between devices.
2. Calculate the propagation delays due to interconnect for each net.
3. Add delay lines, or meander lines, to the clock signal to equalize interconnect delay .

III. OPERATION AND ANALYSIS OF A THREE STAGE DIVIDER

Using three stages, the 10G061 can be configured as a high frequency modulo-n programmable divider, where the division ratio is any sequence of integers between 3 and 4096. One 10G000A quad three input NOR gate is externally required for this implementation. Frequencies in excess of 650MHz are possible using the scheme detailed in Fig. 4 using custom printed circuit boards.

The divide ratio is determined by the following equation:

Divisor = 4096 - Ext. Data

EXAMPLE:

In order to divide by 3, the parallel load data becomes FFDH (Hexidecimal) respectively into CNTRs C, B, and A.

PROOF:

1000H (HEX 4096)
-FFDH (LOAD DATA)
3H (DIVIDE RATIO)

CIRCUIT DESCRIPTION

CNTR A is always enabled to count with signals CNTEN and CIN hardwired high. CNTR B is enabled by the CLOUT signal of CNTR A. It is used to set CNTR B's internal carry flip flop on the next (15th) state. CNTR B is now enabled to count on the next rising edge of the clock. In those cases where FH (15) is loaded into the least significant stage, a COUT is immediately generated. It is used to drive the CNTEN input of CNTR B, thus enabling it to count on the subsequent rising edge of the clock. CNTR C is enabled with the COUT signal of the second stage, driving the CLIN input. The CIN input is driven by the CLOUT2 signal of CNTR A in a slighty different manner than was previously discussed. CNTR C is en-

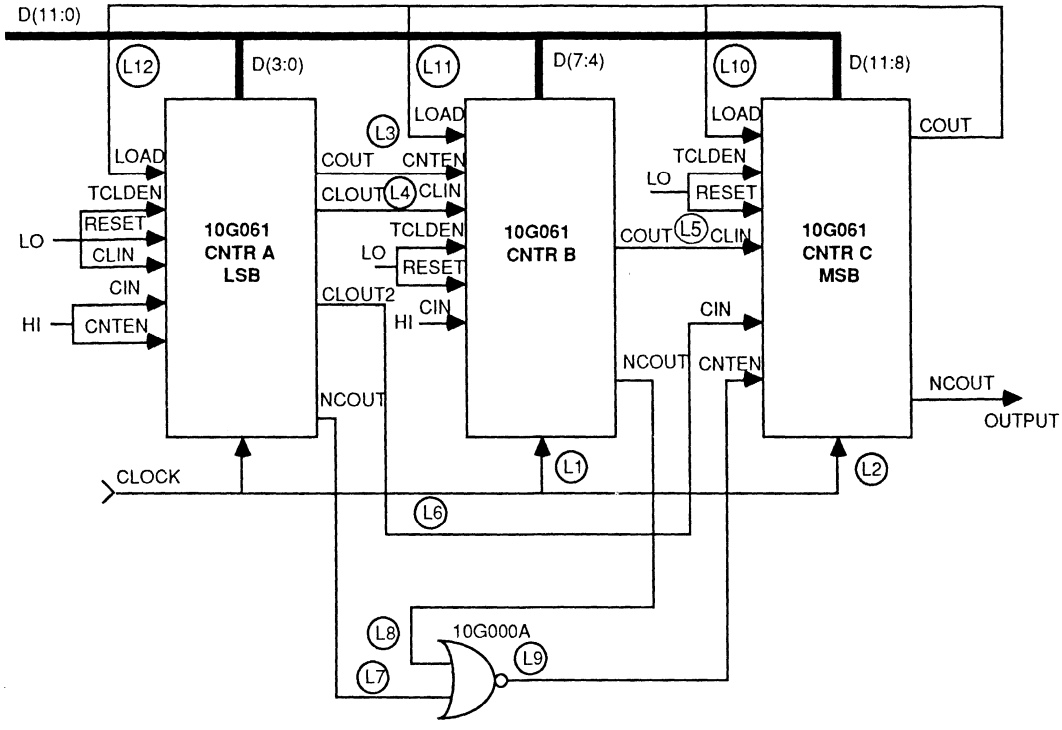


FIGURE 4.

abled to count one clock cycle early so it can generate the COUT signal used to LOAD all stages. It is necessary to generate the LOAD signal to CNTR A early to satisfy the LOAD set-up time and to take into account board delays (more on this later). Using this approach, the 12 bit counter output is taken from NCOUT of CNTR C. The third stage will only begin to count after CNTR B has reached its terminal count and CNTR A has reached its 14th state. If the first and second stages are loaded with FFH, the NCOUT signals are generated and NORed by the 10G000A and used to drive the CNTEN pin, thus enabling CNTR C to count on the next clock edge.

Loading external data, i.e. 4096 minus the divide ratio, occurs when the two most significant stages reach terminal count and the least significant stage generates a CLOUT. The COUT signal of CNTR C is used to drive all LOAD inputs. This approach allows at most 2 clock cycles before loading data into CNTR A. Therefore, the performance limiting nets are associated with the CNTEN signals.

Maximum performance of the circuit is determined by the following equation:

$$1/f = Tpd + Tset\text{-}up\ max + Tpd(interconnect)$$

Several paths must be analyzed to maximize the performance of this circuit using delay lines. As a baseline, all traces should be as short as possible and delay lines for the clock signal will be added to CNTR B and C to compensate for counter enable signal inter-

connect delays.
Looking first at CNTR A and B, for the L3 path,
T_{pdL3}= 300 + 1in(150ps/in) = 450 ps. max.
T_{pdL3}= 200 + 150 = 350 ps. typ.

For the L4 path,
T_{pdL4}= 350 + 150 = 500ps max.
T_{pdL4}= 250 + 150 = 400ps. typ.

Therefore, a delay line, **L1**, of 500 ps should be added to the CNTR B CLOCK input to compensate for the path delays analyzed above. Note that 1 in. of coax is being used for all connections for purposes of this example, but L3 and L4 should be equal in actual board designs.

Now looking at CNTR B and C, again several paths must be analyzed and compensated in the same fashion. Specifically, L5, L6 and the NOR circuit path delays must be determined and compensated.

T_{pdL5}=350 +150 = 500 ps. max.
T_{pdL6}=T_{pdL6} +T_{su} = 150 + 350 = 500 ps. max.

Therefore, a delay line of 500 ps. should be added to the clock input for CNTR C, **L2**. It must be noted that
$L7 + L9 + T_{pdNOR} \leq L2$
and
$L8 + L9 + T_{pdNOR} \leq L2$

to prevent CNTR C from counting when the two least significant stages get to terminal count. Additionally, L1 and L2 must be less than 1 clock period and L4 = L6. Similarly, the NOR gate should have its input signals delayed by the same amount. Specifically,
$T_{pdL7} = T_{pdL8}$
T_{pdL9} = As short as possible

Considering the LOAD signals, $L_{10\text{-}12}$ several precautions must be adhered to for sucessful counter design. Remember, here it is important not to present a LOAD simultaneous with a CLIN, therefore:

$2 \text{ clocks} \geq T_{pdCIN\text{-}COUT} + L10 + T_{suLOAD} \geq 1 \text{ clock}$
$2 \text{ clocks} \geq T_{pdCIN\text{-}COUT} + L11 + T_{suLOAD} + (L2 - L1) \geq 1 \text{ clock}$
$L12 + T_{suLOAD} + L2 \leq 1 \text{ clock}$

With these design equations, it is possible to achieve 650MHz typical performance using custom prionted circuit boards. This performance level is sufficient for most synthesizer applications. Using a GigaBit Logic prototyping board, 500MHz performance was realized (FIG. 5).

IMPLEMENTATION #2

This implementation (FIG. 6) employs a single external gate to create a three stage synchronous counter/divider. The operation of this circuit is very straightforward compared with the previous design. CNTR A is always enabled and will enable CNTR B on the 15th state. CNTR B will enable CNTR C when it reaches its 15th state. When all counters are individually at their 15th state, the NCOUT signals are NORed, and generates a LOAD signal. Note that with the addition of another gate, it is possible to asynchronously load data at anytime. This scheme will have a lower maximum operating speed for two reasons. First, it does not use the carry-look-ahead function. Second, it propagates the enabling signal at the 15th state. The maximum speed of operation is therefore limited by the sum of the CNTEN set-up time, CLOCK to COUT progation delay time and the propagation delay of the board interconnection (strip line, semi-

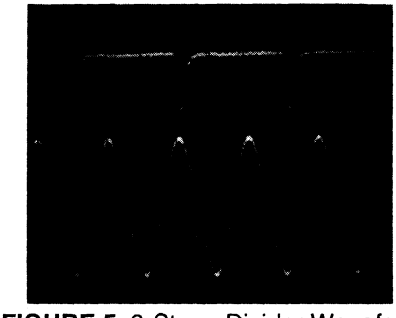


FIGURE 5: 3-Stage Divider Waveforms

rigid coax, etc.) **or** the sum of the CLOCK to NCOUT delay, LOAD set-up time and the interconnect delay. However, this scheme does offer synchronous LOAD and RESET, simplicity, and requires only a single external 10G000A quad NOR gate. Estimated speed of operation is 459MHz.

TWO STAGE DIVIDER EXAMPLE

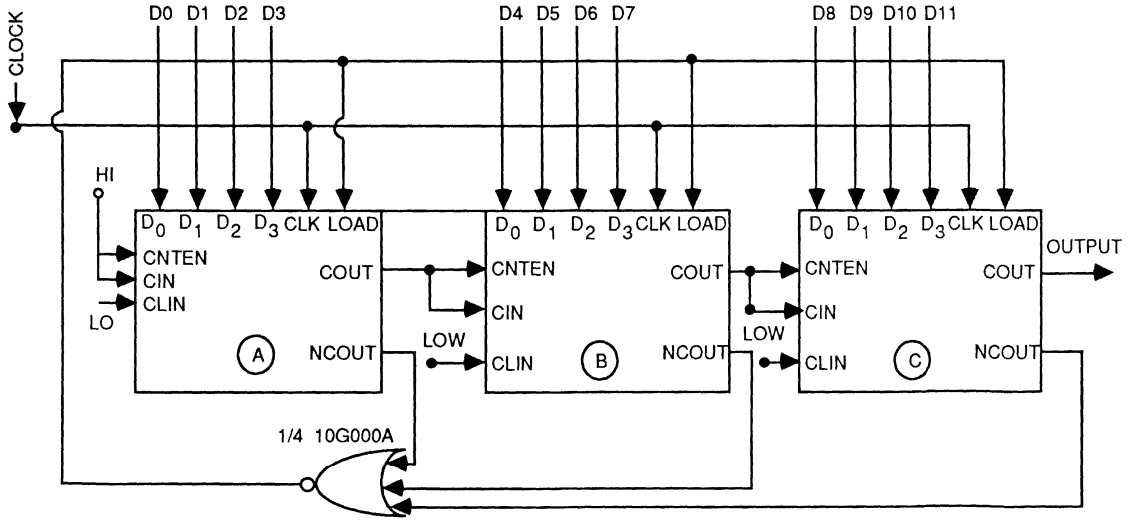
IMPLEMENTATION #3

This two stage counter/divider has a simulated capability of greater than 850MHz operation, with divide ratios of up to 256 (Fig. 7). This design is similar to Implementation #1. It employs carry-look-ahead and requires an external NOR gate. CNTR A is always enabled. CNTR B is enabled with the CLOUT signal of CNTR A at the 14th state. CNTR B can also be enabled if a 0FH is loaded into CNTR A, thus immediately generating a COUT signal. The COUT signal of CNTR B is used to drive the LOAD input of CNTR A. This scheme is also capable of synchronously RESETting the counters with an external signal.

CONCLUSION

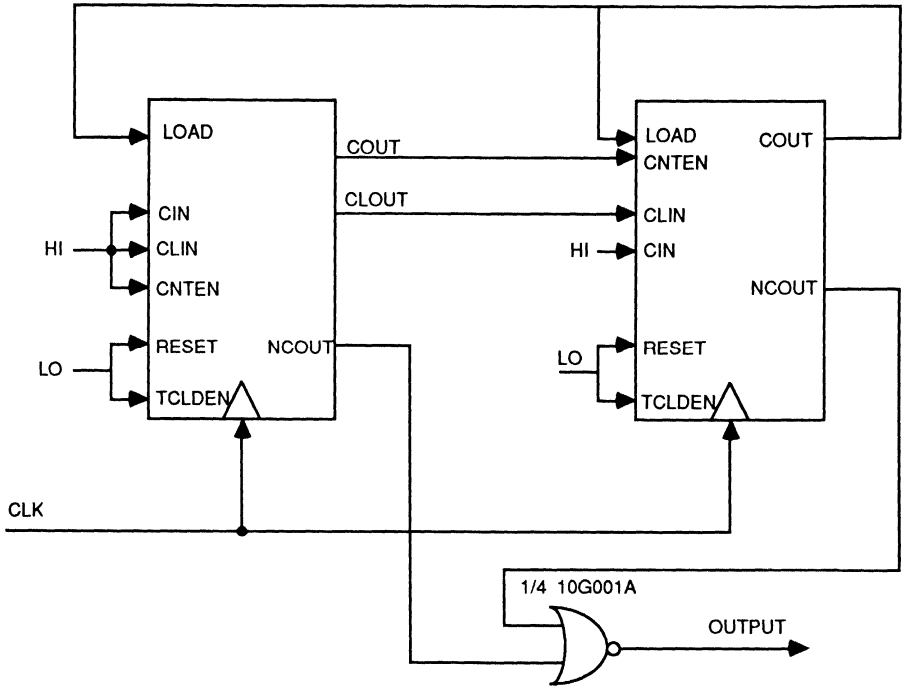
It was shown the the 10G061 Synchronous Counter can be cascaded to form a 12 bit divider, capable of divide ratios of up to 4096 with typical clock frequencies up to 650MHz. A two stage 8 bit counter-capable of achieving typically 850 MHz performance was also shown. It is important that in designing such counters, board delays and circuit placement play a critical role in achieving maximum performance. The circuits shown are ideal for most frequency synthesizer applications.

FIGURE 6. Implementation # 2



A = Least significant stage
C = Most significant stage

FIGURE 7. Implementation # 3



Application and Performance of GigaBit's 40 I/O Chip Carrier

Application Brief #1

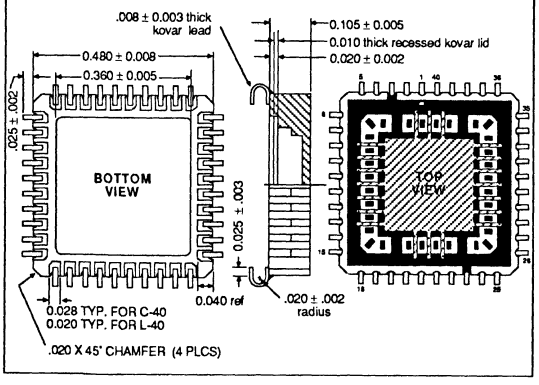
INTRODUCTION

This application brief will discuss the application and performance of GigaBit Logic's 40 I/O leadless and leaded chip carriers designed specifically for PicoLogic™ and NanoRam™ digital GaAs IC families. These packages (referred to as L-40 and C-40, respectively) have design features which permit electrical and thermal device characteristics unrealizable in traditional IC packages. This information will enable PicoLogic and NanoRam users to get the most performance out of their devices and will also be of use to GigaBit foundry customers who wish to use this package with their own custom and semi-custom designs.

PACKAGE DESIGN

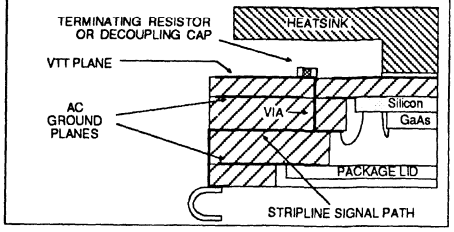
The L-40 and C-40 packages are JEDEC standard outline, custom designed multi-layer, co-fired alumina ceramic cavity-down chip carriers (Note: cavity-down means that the die is attached to the underside of the package top surface and faces down towards the pc board). A mechanical drawing for the two packages is shown in **Figure 1**. Note that the package body (excluding leads) is identical for both leaded and leadless versions with the exception that the pad width on the C-40 package is 0.028" (versus 0.020" for the L-40) to allow for lead attachment tolerances.

FIGURE 1: MECHANICAL DRAWINGS



Typically, a silicon substrate is placed in the package cavity beneath the GaAs die. This silicon IC is primarily used to provide low inductance power supply decoupling capacitors in very close proximity to the GaAs IC. A cross-sectional assembly drawing of the C-40 package showing the silicon and GaAs ICs is shown in **Figure 2**.

FIGURE 2: PACKAGE CROSS-SECTION



Electrical Considerations

The signal and power fan-outs from die bonding pad to package lead are controlled impedance (50-60 Ω) low loss stripline transmission lines. The line widths are 8 mils, typical, with reference planes formed by the package seal ring layer and die attach metallization, 35 and 30 mils, respectively from the signal lines. The reference planes are programmable during wirebonding and are typically tied to VTT. Worse case inter-line voltage coupling is about 3.2%, or about -15 dB. Maximum one-way propagation delay is about 60 ps. Maximum line capacitance is about 1 pF.

Two of the package I/Os (pins 3 and 23) are fixed at VTT potential. Metallized castellations bring VTT up to the package top surface, forming a VTT ground plane. Vias on all but 6 (numbers 4, 17, 18, 24, 37, and 38) of the remaining 38 pins travel from the stripline lead fan-out to the package top surface. This is shown in Figure 2. Terminating resistors or decoupling capacitors can then be placed (with solder or conductive epoxy) between the I/O via and the VTT plane for inputs and power supplies, respectively. A dielectric layer is screened on the package top surface, over the center of the VTT ground plane and in fingers between the vias as shown in the cross-hatched pattern of Figure 1. Thin metallization patterns exist under the dielectric fingers, between the inner VTT plane and the outer VTT ring. The dielectric pattern in the center provides isolation for an optional heatsink (described below) and the dielectric fingers isolate the vias and serve as solder dams.

Thermal Considerations

The L-40 and C-40 are cavity down packages, designed to be used with heatsinks attached to the package top surface. In this configuration, there is only a 20 mil thick ceramic layer between the device and heatsink. Junction to heatsink thermal resistances as low as 7 °C/W are thus realizable, depending on die size. Two heatsinks have been designed to be used with the L-40 and C-40 packages: GigaBit part numbers 90GHSK-40-A and 90GHSK-40-B. These heatsinks (with effective surface areas of 12 and 24 sq cm, respectively) have studs on the bottom to attach to the center of the package top surface and provide clearance for chip resistors and capacitors. The

thermal characteristics of the packages and heatsinks are thoroughly discussed in GigaBit Application Note 3: **Thermal Management of PicoLogic and NanoRam Digital GaAs IC Families.**

PACKAGE USE AND CHARACTERISTICS

Socketing

The footprint is a JEDEC standard outline (Standard MS-009 for 0.040" center packages), allowing the use of off-the-shelf DC and burn-in sockets (i.e., Plastronics® P/N P2040S or Textool® P/N 240-5084) for the leadless package. A high-speed socket, capable of up to 2 GHz operation is planned. This socket is based on a metal-on-elastomer contact technology.

The performance of the leaded version of the package is virtually the same as the leadless version because the internal construction is identical.

Terminating Resistors and Decoupling Capacitors

Top surface passive components are not required, but this option can improve high frequency device performance. Terminating inputs on the package reduces worse case unterminated stub lengths from about 60 ps to about 20ps, with capacitive stubs (i.e., package input capacitance) likewise reduced by a factor of 3 to about .33 pF, maximum. Top surface decoupling capacitors will have about one third the 3.5 nH series inductance of pc board level capacitors.

The top surface vias are on 35 mil centers, requiring resistors and capacitors which are about 30 mils wide or less. Resistors such as Mini-Systems MSR-21 or equivalent work well. They are 20 mils wide by 40 mils long and 10 mils thick. The capacitors inside the package range from about 100 pF to 250 pF per supply, so 1000 pF or greater are preferred for the package top surface. Standard capacitors are available up to 2200 pF in an X-7R dielectric in a 30 mil wide by 40 mils long by 30 mils thick format. The Johanson R09 size is one example.

Added benefits resulting from the use of top surface terminating and decoupling components include increased board level package density (and thus, decreased propagation delays) and simplified pc board layout.

Package Electrical Measurements

Figure 3 shows measured package one-way voltage signal thru-loss as a function of frequency. It is seen that the package has less than 0.5 dB of thru-loss up to 3 GHz (i.e., 90% of the voltage amplitude is maintained.) **Figure 4** shows output rise and fall times of a 10G012A complemetary driver/comparator in the leadless package (the corrected vertical scale is 200 mv/div because a 20 dB attenuation pad was used on the sampling oscilloscope). The 20-80% rise and fall times are both seen to be less than 100 ps. **Figure 5** shows normalized output swings for the same device with both board level and package level terminating resistors. The improvement in voltage swing is seen to be modest at low frequencies, but fairly significant above about 2 GHz. Even at low frequencies, waveform fidelity can be improved by using package level passive components. It should be noted that all measurements quoted in this application brief were taken with a prototype of the elastomeric socket mentioned above.

FIGURE 3: PACKAGE THRU-LOSS (VOLTAGE) VS. FREQUENCY

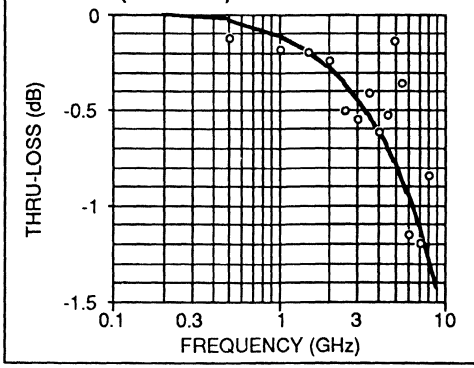


FIGURE 4: PACKAGED DEVICE RISE AND FALL TIMES

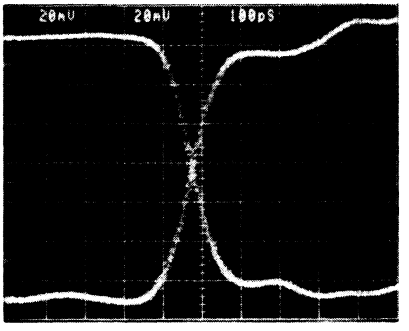
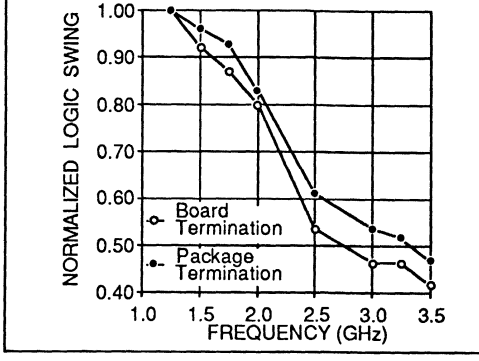


FIGURE 5: PACKAGE AND BOARD LEVEL INPUT TERMINATION



Minimizing Clock Skew Through Use of the 10G010 and 10G011B Fanout Buffers

Application Brief #2 By Carl Eggert Deierling

INTRODUCTION

A major concern in the design of high speed logic systems is the arrival of a given signal at two different destinations with a delay between arrival times: signal skew. Some delays are predictable, permitting cancellation schemes to be employed, however **indeterminate** skew will directly reduce operating speed. Two application areas are immediately evident where the same signal must be widely distributed in a logic design. The first of these is clock distribution. In a synchronous system, logic is partitioned such that a common clock drives each group. Other groups may be driven with the opposite phase of the clock, and precise phasing of the clock is critical to achieve maximum performance. Clock skew will directly reduce the system bandwidth. A second area of design which requires precise timing is bus applications. Memory arrays are a good example of this. A thorough discussion of skew and techniques for minimizing it as it relates to memory arrays, may be found in GigaBit's Application Note 5[1].

FANOUT BUFFER CONCEPTS

Any high speed part possessing multiple identical outputs can be used to distribute signals to multiple devices with a minimum of temporal skew among outputs, if the part is designed with most of the the circuit delay common to all outputs. GigaBit Logic has two such devices in the PicoLogic™ family of GaAs ICs: the 10G010 and 10G011B Dual Quad Output Fanout Buffers. The logical functions perfomed by the two parts differ; there are different types of inputs on each part with different delay specifications. **Figure 1** illustrates the delays with maximum variations associated with each of the elements of a Fanout Buffer. To simplify the discussion, a single device over a given operating environment has been selected as the example. The logic delay variations given in **Figure 1** are for the data inputs of the 10G010M-2 over the full -55 to +125°C temperature range. Reference should be made to the data sheets of the two parts for precise total delay figures over less severe commercial environments, as applicable. Since input and output package delay and output source follower delays are identical for both parts as identified in Figure 1, LOGIC BLOCK delays can be readily derived as the total delays less the package delays and source follower delay. As can be seen from this figure, the maximum possible skew among the four outputs on one half of the IC is less than 15 ps (10 ps due to input and output bond wire length differences plus 5 ps due to output source follower FET variation). Due to the monolithic nature of the duals, parametric variations which would result in differences in delays between the two halves is minimal, accounting for at most an additional 40 ps. Unfortunately, production measurement equipment cannot confirm these miniscule delay differences, hence the skew specifications given in the

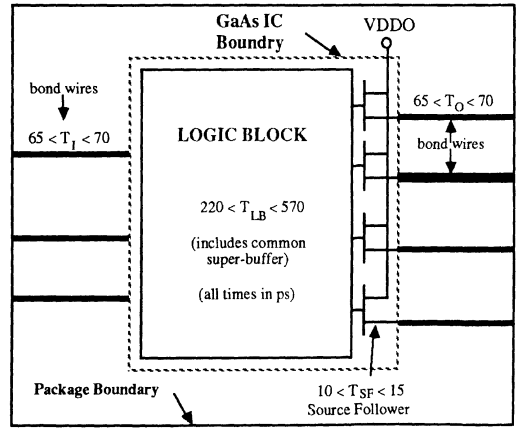


Figure 1. Skew allocation for 10G010M-2 over temperature range of -55 to 125°C.

data sheets are overly conservative.

CRITICAL CIRCUIT BOARD LAYOUT CONSIDERATIONS

Most high gain **combinatorial** IC's have the potential for instability. This may be easily noted if CMOS, TTL or ECL devices are biased at threshold. ECL oscillations are generally caused by negative input impedance, and have been "cured" by adding a series resistor at the inputs. Other typical logic circuits oscillate due to feedback from output to input. Components which have a multiplicity of outputs switching simultaneously obviously have an even greater propensity to oscillate. GaAs differs from silicon in this respect only as to the frequency of oscillation; the outputs are switching at 5 to 10 volts per nanosecond generating high levels of both conducted and radiated EMI. The internal delays are considerably less than a nanosecond, which when added to the external delays results in the π or 2π radians of phase shift required to sustain oscillations for inverting and non-inverting operation respectively, at frequencies well in excess of 1 GHz. Oscillation of a digital part when biased at threshold is not uncommon and will generally not prove deleterious to proper operation. However, in the case of the Fanout Buffer (especially the 10G011B), such oscillations may be excited by input signals occurring near subharmonics of the natural frequency of oscillation. These oscillations are not entirely damped out as the gain is reduced due to its being in high or low states. Although these oscillations appear on the output high or low states at an insignificant amplitude, the oscillation is sustained internally. This oscillation at the input then either reinforces or subtracts from the input signal, thereby effectively either advancing or retarding it, resulting in output jitter or phase noise. This effect can be quite pronounced when the signal is at subharmonics of the 1.1 to 1.3 GHz natural frequency of oscillation of the 10G011B (See Fig. 2).

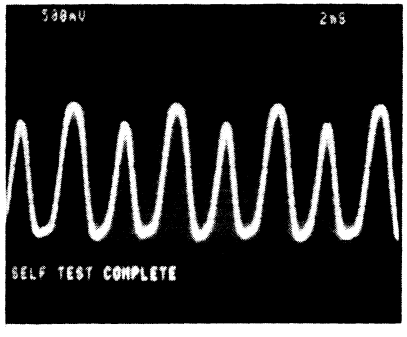


Figure 2. 10G011A Ouput Phase Jitter

Precautions must be taken to minimize output signal coupling back into the inputs with such a phase relationship as to cause instability. This instability in the 10G011B, which drives multiple outputs in phase with the input, generally manifests itself as a tendency for the output to exhibit a jitter or phase noise as previously discussed. However under some severe conditions, such as when power supply decoupling is faulty, or heavy coupling exists between inputs and outputs, the oscillation frequency appears on the output waveform. This oscillation of approximately 1.2GHz is induced by coupling from output to input, depending on the relationship of the signal period and the circuit delays and various parasitics and common mode signals. It is even possible for standing waves to appear on ground planes thereby coupling undesired signals. For this reason it is essential that power plane decoupling recommendations found in Application Note 2[2] be diligently followed. Additionally it has been found that the part type, package, input pins, input levels, frequencies, and output pins all play a factor in this jitter.

The 10G010 is least likely to exhibit these characteristics in real systems, hence it is recommended for all applications except those where the specific gating function of the 10G011B is required. Either 40 pin package has been found to be far superior to either of the 36 pin packages with the 36 pin Flat Pack being the least stable. For the 10G011B, the EN input is least likely to cause this problem, and the IN input is less likely to cause the problem than the GATE input. It is mandatory that the GATE input and desirable that the IN input be driven with GaAs levels (>1.0V p-p). Even with these precautions, certain frequencies will exhibit output jitter. The system implications of this be-

havior must be empirically evaluated by the user. Preferred signal input options for both the 10G010 and the 10G011B are indicated in **Table 1.** If all four outputs are not required, the A Outputs (on the sides of the packages) should not be used.

A key ingredient in preventing oscillation in any part is to reduce the effect of any undesired signals which might couple into the inputs. A way to do this is to capitalize on the common mode rejection capabilites of the IC's. This is particularly true for devices possessing differential inputs, such as the 10G002, 10G004, 10G010, 10G012B, 10G021A and 10G041A. Even in the absence of differential inputs, the VBB reference input may be used to minimize common mode noise. **Figure 3** illustrates the proper techniques for reducing the effect of common mode input signals for both a-c and d-c coupled signals for devices with and without differential inputs. As shown, the shield of the coax of the input signal is decoupled to the VBB and/or to the negative input of the differential stage. This coax shield represents the return ground plane of a printed circuit board. This would be the ground (power) plane immediately adjacent to the signal trace. In the case of stripline, both planes surrounding the signal trace should be capacitively coupled to the VBB or unused differential input.

One word of caution applys to a-c coupled inputs for any device. If the signal has a low frequency component, the resistor capacitor combination must have a time constant several times the duration of the longest string of 1's or 0's to prevent base line shift. If the signal will be absent for some time, the capacitor will charge in such a direction as to establish the input (inputs for differential input devices) at threshold. As stated earlier most digital devices will oscillate if their inputs are biased at threshold. Therefore, it is desirable to apply an intentional offset to the inputs. This may be accomplished by putting a 1K resistor between the signal input pin and VSS if the quiescent state of the signal input is low. This will add -100mv of offset to the input pin (for RT = 50Ω). Alternately, a 620 Ω resistor could be connected to VDD to provide a positive offset when the quiescent state of the signal is high. The termination resistor could be increased in value sufficiently to maintain a Thevinen equivalent to better match the characteristic impedance. Another possible option if this offset and baseline drift is undesired is to provide a pull down or pull up resistor to a voltage with a clamp to limit the low level or high level excursions for signals with 1.5v p-p swings respectively. This is also illustrated at the bottom of **Figure 3**.

TABLE 1

10G011B INPUT RECOMMENDATIONS

REQUIRED FUNCTION	INPUT PIN		
	IN	GATE	EN
Single Input Buffer	H	L	Sig
AND Buffer	Sig*	L	Sig
OR Buffer	Sig*	Sig*	H
OR-AND Buffer	Sig*	Sig*	Sig

* PicoLogic™ levels (1 Vp-p min.) recommended.
† PicoLogic™ levels mandatory. Avoid signal width (of either polarity) less than 2 ns.

10G010 INPUT RECOMMENDATIONS

REQUIRED FUNCTION	INPUT PIN			
	A	B	SEL +	SEL -
Single Input Buffer	L L	H Sig	Sig H	VBB L
Inverting Buffer	L L	H Sig	VBB VBB	Sig H
Multiplexing Buffer	Sig1	Sig2	VBB	Contr

SUMMARY

The 10G010 and 10G011A Fanout Buffers are widely employed in systems for driving GaAs, ECL, TTL and CMOS circuits where either minimum skew, sharp transition times or large capacitive drive features are required. Because both devices drive many outputs in phase with the input, the potential for the devices exhibit output phase jitter or oscillation is present given the limitations of real boards on which they are mounted. Therefore, it is essential that careful layout, decoupling and common mode signal rejection practices be adopted when using these devices. The discussion in this Brief regarding phase jitter should be

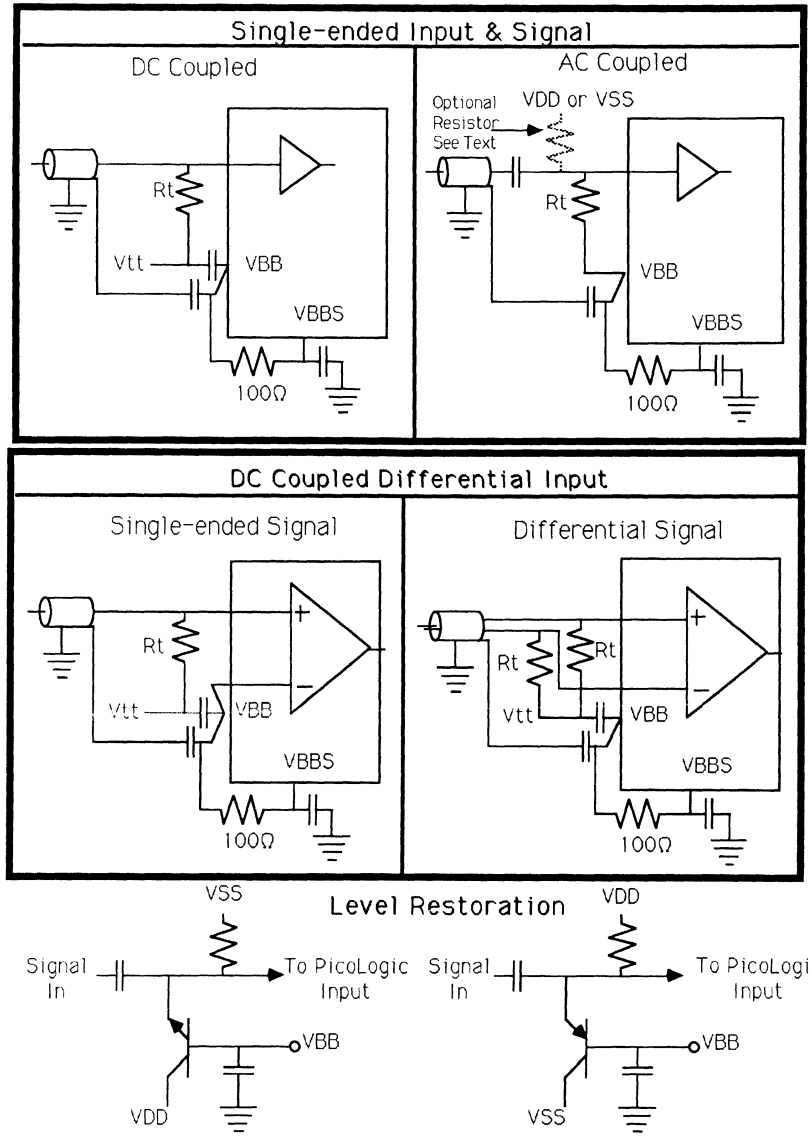


Figure 3. Techniques for reducing the effect of common mode input signal for AC and DC coupled signals.

used to provide guidance in their proper application.

References

1. "Guidelines for the Use of the 12G014 400MHz Registered RAM", Carl Eggert Deierling, GigaBit Logic, October, 1987.
2. "Guidelines for the Use of Digital GaAs ICs", Carl Eggert Deierling, GigaBit Logic,January, 1987.
3. "Interfacing PicoLogic™ and NanoRam™ ICs to Other Logic Families", Carl Eggert Deierling, GigaBit Logic, August, 1986.

Decoupling and Termination Recommendations for PicoLogic™ and NanoRam™ GaAs ICs

Application Brief #3 By: Jack Guedj

INTRODUCTION

In high-speed systems, power supply decoupling is sometimes best solved empirically. The nature of the board design, the components used and the frequency of operation are some of the factors that will determine decoupling requirements. This application brief discusses a rigorous approach to power supply decoupling based on transient current flows. Simpler decoupling schemes can also yield acceptable results. When prototyping, we recommend extensive use of decoupling capacitors. For production designs, where board complexity and parts count are important factors, it is advisable to empirically determine the minimum number of required decoupling capacitors.

This application brief also describes the proper approach to signal line termination for boards implemented with GigaBit's GaAs ICs. To highlight this discussion, we will use the 90GUPB Universal Prototyping Board. For more information on the 90GUPB consult the 90GKIT datasheet.

90GUPB UNIVERSAL PROTOTYPING BOARD

The 90GUPB is a 16-site printed board. It contains 8 sites for 36 or 40 lead PicoLogic™ and/or NanoRam™ ICs, and 8 sites for .300" or .400" wide DIP ICs with up to 24 pins. The 90GUPB has dedicated voltage planes for every voltage conveyed to the circuits (VDD, VTT, VSS, and VEE/VCC). When the board is properly wired, these planes enable the circuits to operate in a good noise-free enviroment. Moreover, the 90GUPB uses via holes between power planes in order to provide VDD and VTT in close proximity to each GaAs IC footprint (See Fig. 1and 2). Therefore, decoupling capacitors and termination resistors can be placed right at the package. This provides a good input match and minimizes the effects of lead inductance for higher power supply noise inmunity.

POWER SUPPLY DECOUPLING

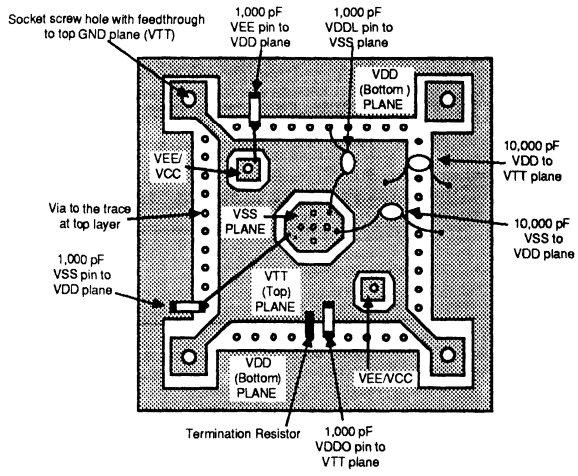
I. Decoupling of IC Package Pins to Power Supply Planes:

Most PicoLogic™ standard products have VSS, VDDL, VDDO, VEE and VBB power supply pins. These pins are decoupled inside the package with 100 to 200 pF to provide bypassing as close to the die as possible. Nevertheless, we recommend external decoupling for higher noise immunity. As a general rule, decoupling follows DC and transient current flows. A basic CDFL (Capacitor Diode FET Logic) schematic for a 2-input NOR gate (Fig. 3) illustrates the current flows (bold lines). Figure 4 summarizes the decoupling discussed in the following text.

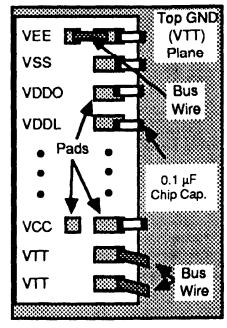
VEE (-5.2 V typ.) provides the most negative potential used for a current source. It has relatively low DC and transient currents. VEE pins should be decoupled to the VDD plane with 1,000 pF chip capacitors.

VSS (-3.4 V typ.) acts as the source supply for all logic switching circuitry. It should be maintained as noise-free and as well regulated as possible. Both heavy DC and transient currents will flow from VDDL to VSS. VSS pins should be decoupled to the VDD plane with 1,000 pF chip capacitors.

VDDL is normally the external logic ground connection. As a reciprocal of the previous paragraph, all VDDL pins should be decoupled to the VSS plane. Since the VSS plane can only be reached in the central area of the bottom GaAs IC site on the 90GUPB, a

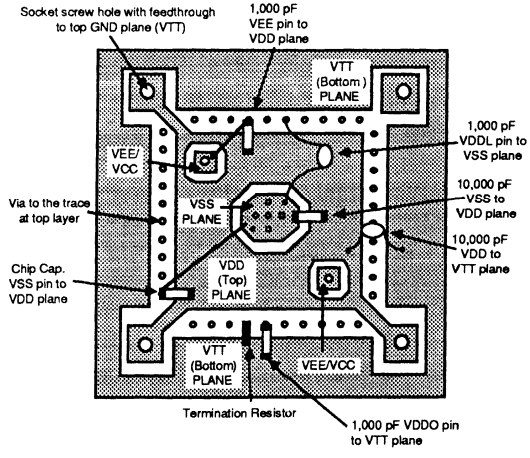


a) Bottom view of GaAs IC site

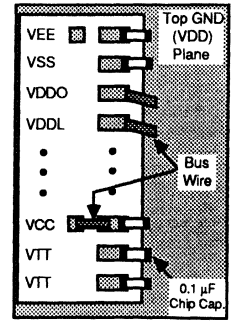


b) Power supply decoupling (Not shown: a 0.1 µF chip capacitor between the VSS entry points and the VDD plane at the bottom of the board)

Figure 1. Bottom view of the GaAs IC site and power supply connections on the 90GUPB VTT = Ground (Top Plane); VDD = +2 V (Bottom Plane)



a) Bottom view of GaAs IC site



b) Power supply decoupling

Figure 2. Bottom view of the GaAs IC site and power supply connections on the 90GUPB VDD = Ground (Top Plane); VTT = -2 V (Bottom Plane)

1,000 pF leaded capacitor should be used to connect all VDDL pins to the VSS plane.

VDDO is the output driver ground pin. Since the output is terminated to VTT (usually with a 50Ω resistor), DC and transient currents will flow from VDDO to VTT. Therefore, all VDDO pins should be decoupled to the VTT plane with 1,000 pF chip capacitors.

VBB is the reference input voltage to the IC's input threshold tracking circuit. Since the signal and return

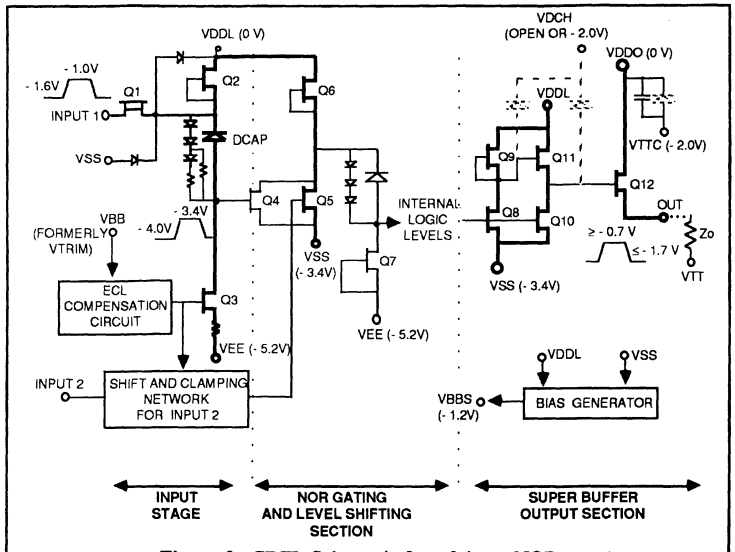


Figure 3: CDFL Schematic for a 2-input NOR gate (current flows represented by bold lines)

path (coaxial shield or ground plane) may possess common noise, the VBB pin should be decoupled to the ground plane (VTT or VDD) with 1,000 pF chip capacitors.

II Decoupling of Power Supply Planes at the Circuit Site Level:

It is important to decouple the power supply planes close to each IC's power supply pins. This decoupling should be done with larger capacitors to filter lower frequencies and larger parasitic currents swings.

VSS: The VSS plane at the circuit site is available in the central area of the IC, on the bottom plane of the 90GUPB (see Fig. 1 and 2). It should be decoupled to theVDD plane with a 10,000 pF leadless or leaded capacitor (see Figure 1 and 2).

VDD: The VDD plane at the circuit site is available around the pins of the IC, on the bottom plane of the 90GUPB (Fig. 1 and 2). It should be decoupled to the VTT plane with a 10,000 pF leaded capacitor.

III. Decoupling of Power Supply Planes at the Board Level:

At the board level, decoupling should protect the board from low frequency noise generated by the power supply buses. For this reason, we recommend the use of 0.1 µF chip capacitors at the board power entry points (Fig. 1b and 2b).

All supplies should be decoupled to the top ground plane (VDD or VTT) at the power entry points. If the top plane is VTT, VSS should also be decoupled to VDD with a 0.1 µF chip capacitor at the bottom of the 90GUPB.

IV. Power Supply Considerations:

Power supplies should be turned on simultaneously. In a prototyping environment, if power supplies are controlled sequentially, VSS should be the last power supply to be turned on and the first power supply to be turned off. It is recommended to use a protective diode in systems pulling large currents through VEE. This happens mainly when PicoLogic™ ICs are used in conjunction with many ECL devices. As shown in Fig. 5, if VEE is suddenly disabled, V1 is going to be at a potential close to VDD and a large current will then flow from V1 to VSS through the on-chip diode decoupling capacitors, now forward biased. If the current is large enough, these decoupling capacitors may short.

The protection diode should be placed reverse biased between VEE and VSS (Fig. 5) so that, even if the VEE supply is lost, the VEE voltage will be maintained a diode drop below VSS, preventing the on-chip capacitors from shorting. Its current handling should be commensurate with the current pulled from the VEE power supply. For protection diodes with slow forward recovery time, a 100 µF electrolitic capacitor should be placed in parallel with the protection diode to prevent occurence of a spike.

SIGNAL INPUT/OUTPUT TERMINATIONS

I Signal Input Terminations:

Signal input pins can be unused, tied high or low, or connected to the output pin of the driving circuit.

Signal input pins tied high should be connected to VDD. Signal input pins tied low should be connected to VTT or VSS.

Unused input pins can be left open. Nevertheless, for protection against stray noise coupling and for lower power consumption, we recommend that inputs of unused gates be biased such that the corresponding outputs are high (see Fig. 4, NOR gate #2).

Signal input pins connected to the output of a driving circuit must be terminated to VTT with the characteristic impedance of the transmission line, 50Ω in most cases (see Fig. 4, NOR gate #3). This termination prevents reflections ("ringing") that could modify the state of the input or degrade the edge rates of the signal. In addition, this termination acts as a pull-down resistance for output source follower FETs of the driving circuit which would be floating otherwise and could not switch low (see Fig. 3).

II Signal Output Terminations:

Signal output pins can be unused or connected to the input pin of the driven logic. Unused signal output pins should be left open. Connected output pins should be terminated at the input of the driven logic as explained in paragraph I.

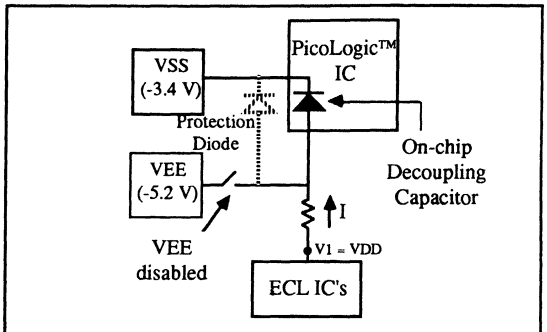


Figure 5: Diode Protection

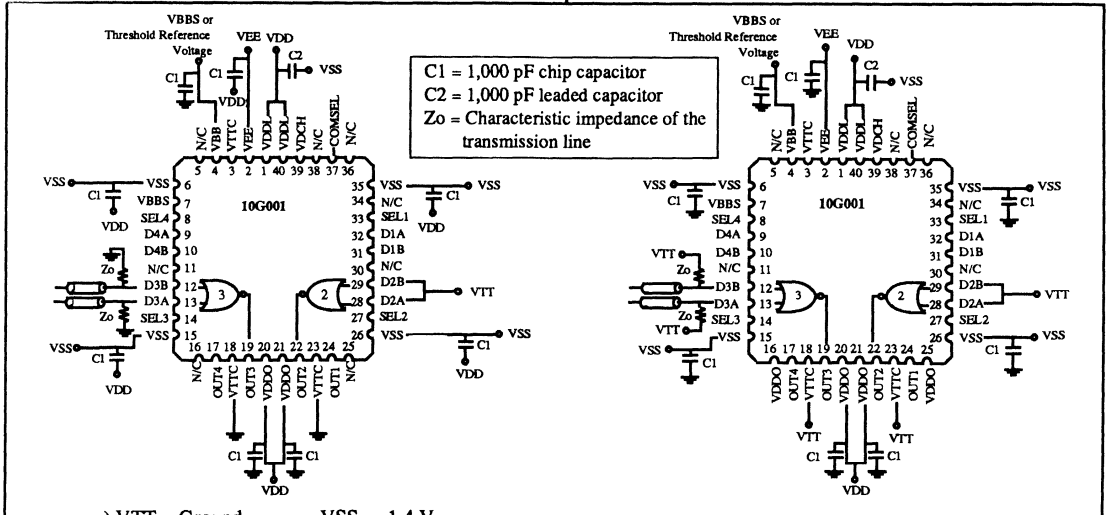


Figure 4: Decoupling of Package Pins to Power Supply Planes for a 10G001 Quad 2-input NOR Gate

Exclusive-OR Inputs Give You Many Uses for GaAs Flip-Flop

Article Reprint #19 By: Carl Eggert Deierling

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Introduction

The 10G024 Quad Flip Flop, a recent addition to GigaBit's expanding GaAs SSI and MSI PicoLogic™ family of standard products, possesses unique XOR D inputs. At first glance, it might appear that providing XOR inputs on the D inputs of a Flip Flop would be of little utility; however these two examples will illustrate the value of this feature. The logic diagram of the 10G024 is given in Figure 1. A high level on the SEL input will result in the inverted (A) input being selected and a low will result in the non-inverted (B) input being selected. Both true and complement outputs are available to further enhance its flexibility. This input structure may be configured in various fashions to extend versatility. Tying the two inputs A* and B together creates one input of an XOR (hereafter referred to as IN), with the other input being provided by the SEL line as illustrated in Figure 2. A simple analysis of the the resulting truth table will show that feedback from the Q output to IN will yield a "T" (Toggle Flip Flop) with the SEL input being the Toggle control. Feeding the Q output back to the SEL input will yield a synchronous S-R (Set and Reset Flip Flop) with A* providing the RESET input and B providing the SET input. Both independent clocks and a clock common to all four sections are available.

This article illustrates methods by which the XOR inputs may be used to expand the 10G061 Synchronous Counter by up to three bits or may be used to supplement the XOR input of the 10G022 to generate Pseudo-random Codes or implement CRC or other encoding schemes at high speeds.

PN Codes and Cyclic Redundancy Checks

An important function which is frequently implemented with XOR's and shift registers is the generation of PN (Pseudo-random Noise) codes. The 10G022 is an eight-bit serial/parallel register which may be configured with an internal XOR at the input of the LSB (see Fig 3). While this is capable of generating some PN codes, the single XOR input for each of the eight bits severely limits the available codes, precluding the generation of many prime polynomials. Another application for a prime polynomial division is CRC (Cyclic-Redundancy Code). See the box for a brief description of CRC and its function.

Since the flip-flops in the 10G024 can implement the XOR function it may be used as the

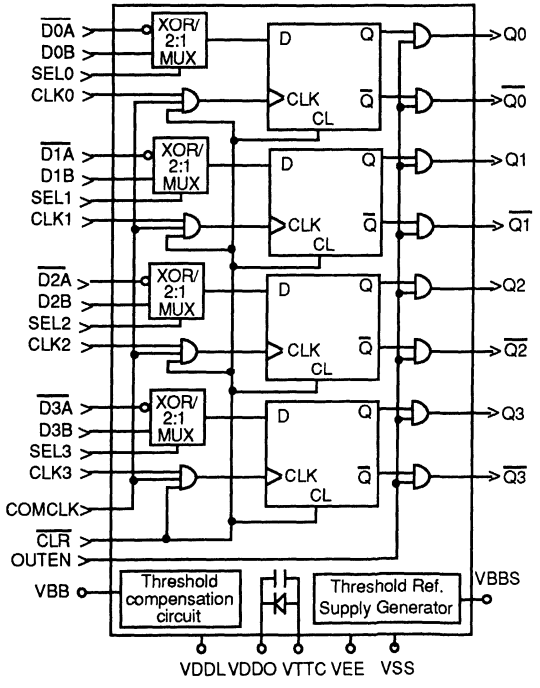


FIGURE 1. 10G024 Block Diagram

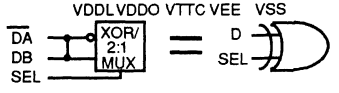


FIGURE 2: Tying the two inputs to create one XOR input

basis for construction of a CRC generator without the need for external XOR gates and the attendant inter and intra chip delays. Figure 4 is the logic diagram of a CRC 16 Checker and Generator, which implements the polynomial $X^{16}+X^{15}+X^2+1$. For simplicity the 11 stages between 3 and 15 are not shown since there are no feedback paths. Note that the 10G022 8 bit shift register could be used for 8 of these bits thereby saving package count as illustrated in Fig. 5.

The circuit shown in these figures implement the required function using the complementary outputs of the flip flop and the complement of the Serial Data In and feedback data, due to the fact that it is necessary to obtain the residue of the register at the completion of the reception of the data and check bits. Although this sensing of zero could be implemented with the 10G045 Parity Checker and Octal Comparator, it may more simply be achieved by simply wire-ORing all of the outputs as shown. If any of the outputs is non-zero the resultant 1 indicates that an error has occurred. When wire-ORing this large number of outputs the termination resistor should be returned to V_{ss} (-3.4 volts) to prevent the sum of all output leakage currents from pulling the output above V_{OL} even when all outputs are low. An alternative to this is to avoid the use of any parts to sense this level which might be susceptible to failure if V_{OL} is above specifications (-1.8 volts). Many ECL parts and most PicoLogic parts do not exhibit this susceptibility.

However, if the outputs were wire OR-ed, they could not be used for completing the shift register. This problem was solved for the 10G024 by implementing the polynomial using the complementary outputs of the flip flops instead of the true outputs. By tying the unused input of the XOR high (to ground) instead of low, the other input is complemented, and the resultant polynomial is as though the true outputs were used. Note that the gating for the serial data input and the serial output of the 10G022 are also complemented again correcting for the complement of the outputs.

For error detection, the register is initialized with a reset and serial data including the appended CRC character is sampled by the DATA-IN input. Once the last check bit is entered, the contents of the register should be zero if no transmission errors have occurred. Note that the Ethernet polynomial is a special case which leaves a hexadecimal residue of C7 04 DD 7B, in the register and would mandate the use of four 10G045's or their ECL counterparts wired as byte comparators to detect this code.

To generate CRC the register is initialized with a reset and the data is sampled by the polynomial generator to perform the modulo division by holding Annex Check Word Low. Data is also driven to the output through the output 2:1 multiplexer. A multiplexing flip flop could be utilized to reclock the output data. At the completion of the transmission of all data bits, the Annex Check Word should be taken high and the appropriate number of 0's must be clocked into the

TABLE 1

Typical Connections		Number of Devices Required 10G024	10G022
LRC 8	X^8+1	2	0
CRC 12	$X^{12}+X^{11}+X^3+X^2+X+1$	1	1
CRC 16	$X^{16}+X^{15}+X^2+1$	2	1
CRC 16 Reverse	$X^{16}+X^{14}+X+1$	2	1
CRC-CCITT	$X^{16}+X^{12}+X^5+1$	2	1
CRC-CCITT Reverse	$X^{16}+X^{11}+X^4+1$	2	1
Ethernet Polynomial	$X^{32}+X^{26}+X^{23}+X^{22}+X^{16}+$ $X^{12}+X^{11}+X^{10}+X^8+X^7+X^5+X^4+X^2+X+1$	8	0
Ethernet Residue	$X^{32}+X^{31}+X^{27}+X^{26}+X^{25}+X^{19}+$ $X^{16}+X^{15}+X^{13}+X^{12}+X^{11}+X^9+$ $X^7+X^6+X^5+X^4+X^2+X+1$	8	0

input at the sending end. For example, CRC 12 would require 12 clocks and CRC 16 would require 16 clocks. Under these conditions the residue remaining after the modulo division will be shifted out of the register and appended to the end of the message as the check bits. Some of the more commonly used polynomials in use with the number of components required for implementing the function are listed in Table 1.

Similarly the 32nd order or the 48th order polynomials could be constructed from two 10G022's and four or eight 10G024's respectively, however at this or the Ethernet chip counts a standard cell implementation would generally be the preferred solution, unless low volumes proscribe ASIC NRE costs.

Synchronous Counter Expansion

The 10G061 is a 4-Bit Synchronous Counter with advanced Carry Look Ahead features and provisions for full programmability to permit maximum speed synchronous counting as a programmable counter extendible to multiple nibbles, with a minimum of additional hardware. Figure 6 is a block diagram of this function.

Figure 7 illustrates the scheme employed to expand one or more 10G061 counters by two bits at the MSB end. The expansion at the LSB end is trivial if board propagation delays are considered. For this reason the discussion will be limited to the expansion at the MSB end of the counter string.

Due to the fact that the COUT and NCOUT outputs of the last 10G061 in a counter chain accurately reflect the status of the entire counter string, they may be used to control whether the 10G024 toggles on the clock by controlling whether the input to the flip flop itself is the true or complement of its present state. The ability of an XOR to provide either a true or complement of its input, as controlled by the other input, thus forms the necessary logic to make synchronous counting possible.

There are several timing considerations which must be observed to maximize synchronous clocking frequency. The slow version of the 10G024 was selected since the 10G061 limits performance for this application.

Table 2 lists the specified maximum pertinent delay paths for both the 10G061 and the 10G024 over the commercial 0 to 85°C case temperature range for the speed grade indicated. It should be noted that the data sheet specifies clock to all output paths of equal delay (1200ps) for the 10G061, however the actual delays are less than this for all but the NCOUT. However since this application remains limited by the NCOUT Delay this fact is inconsequential.

A key requirement for any flip flop to toggle is that the summation of the appropriate $t_{su} + t_d + t_t$ (pc board trace) must be less than the clock period. The designer has no control over the t_{su} and the t_d, other than selecting a different speed grade part, however he must carefully establish and control the t_t trace delay. It may be seen from the 10G024 pinout of Figure 8 that the proximity of Q3 to SEL3 and Q2 to SEL2 minimize the trace lengths and hence the t_t. It should also be noted that the wrap-around path can go to the SEL inputs equally as well as to the D inputs since the logic is acting as a two input XOR. The most critical path in

Table 2

Worst Case Times over Temperature		10G061-2	10G024-3	
Clock to Output Delay -	(t_d)	1,200	1,050	ps
Set-Up Time (Sel-Clock)	(t_{su})	N/A	-40	ps
Set-Up Time (Data-Clock)	(t_{su})	325	-40(+10)*	ps

The 10G024 data to clock set-up time is specified at -40 ps, however the necessary tying of these two pins to implement the XOR function may add as much as an additional 50 ps delay and is represented here as additional set-up time. Note that internal custom wire bonding of the A and B inputs will virtually eliminate this 50 ps delay.

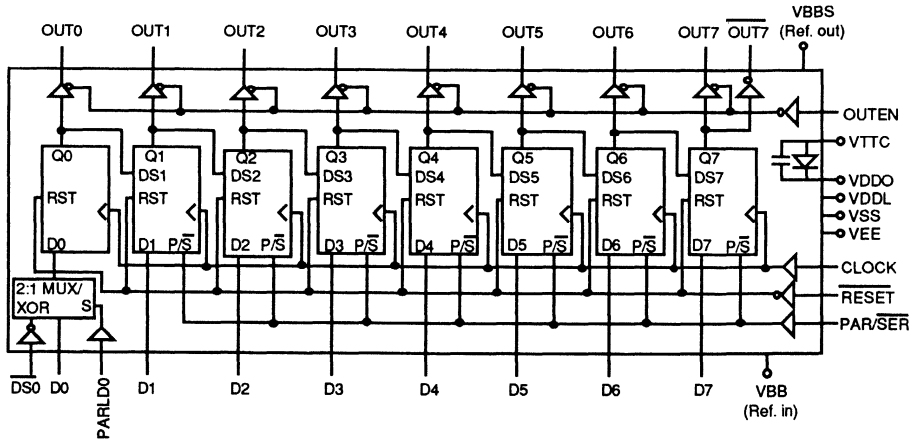
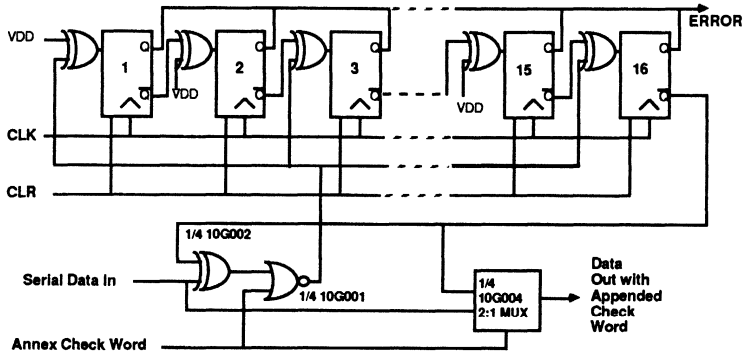


FIGURE 3: 10G022 Block Diagram



POLYNOMIAL: $X^{16} + X^{15} + X^2 + 1$

FIGURE 4. CRC-16 Checker/Generator using four 10G024 flipflops

CYCLIC REDUNDANCY CHECKS
Algebraic Coding Theory, Berlekamp, McGraw Hill, 1968

Cyclic redundancy encoding and decoding schemes have long been recognized as an efficient method to detect errors in a serial digital data transmission systems. A single check word is generated at the transmitter as the remainder resulting from dividing the block of data by a selected non-divisible polynomial. This remainder is then annexed to the block of data being transmitted. This block of data and the appended check bits are divided by the same polynomial at the terminus and the resultant residue will be predictible (zero in most cases) provided no errors have occurred in either the block of data or the appended check bits. This provides a much more reliable method for detecting errors than a simple parity check with substantially lower bandwidth overhead. The number of errors which will be detected with assurity is dependent on the block size and the polynomial selected. The probability of detection of an even larger number of errors is a function of the number of errors, the polynomial selected, and the block size. Although the number of polynomials which could be selected to perform this modulo division at any given degree may be theoretically large, existing standards generally govern the polynomials selected, with certain industries selecting "their own". Higher speed requirements, even exceeding the 100 MHz FDDI standard, place ever greater demands on encoding and decoding speeds.

this case is the wire-ORed output of Q2A's Q* and NCOUT, particularly the NCOUT path to the input SEL input of Q2B, which has been identified with an asterisk. Since this is the maximum logic delay path, minimization of board trace delay will yield direct performance benefits.

Summary

The unusual XOR input of the 10G024 provides a building block for implementing a CRC Checker and Generator capable of operation to 800 MHz depending on board layout and the desired polynomial. Its flexibility to operate as a Toggle flip flop with enable or as a Synchronous Set/Reset flip flop can have various other applications where system operating speeds approaching 1GHz are required.

For all high speed applications a careful layout is required to minimize and equalize board delays where necessary. The minimum trace distance of approximately 0.3" represents approximately 50 ps or 60 ps on microstrip or stripline glass epoxy substrate respectively. Other board materials may be selected to further enhance performance.

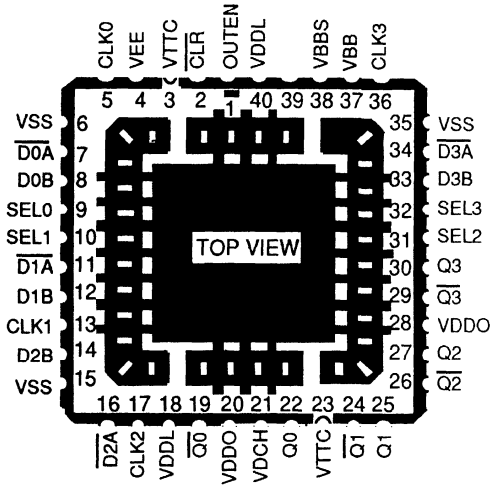


FIGURE 8: 10G024 Pinout

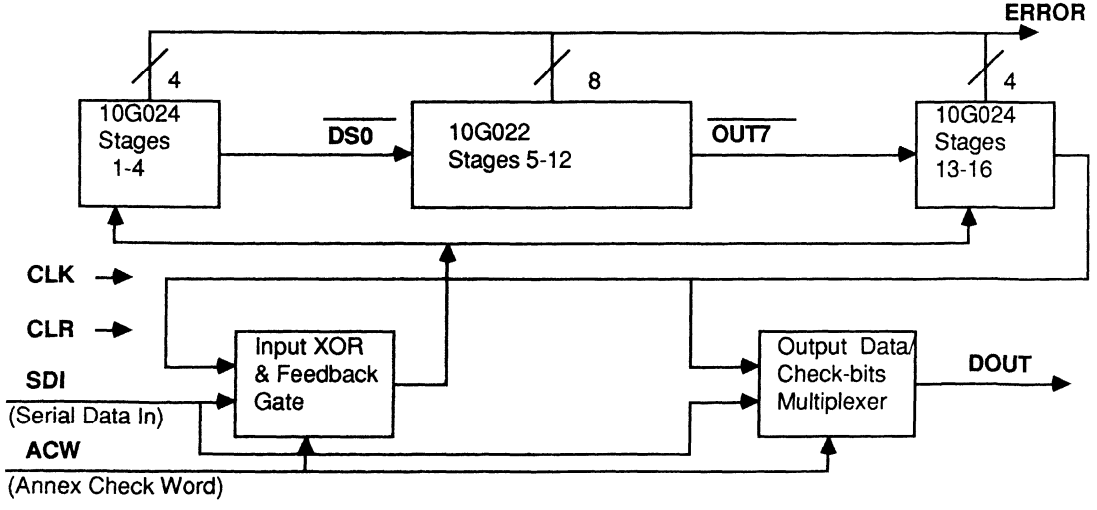


FIGURE 5: CRC-16 Using a 10G022 and 10G024s

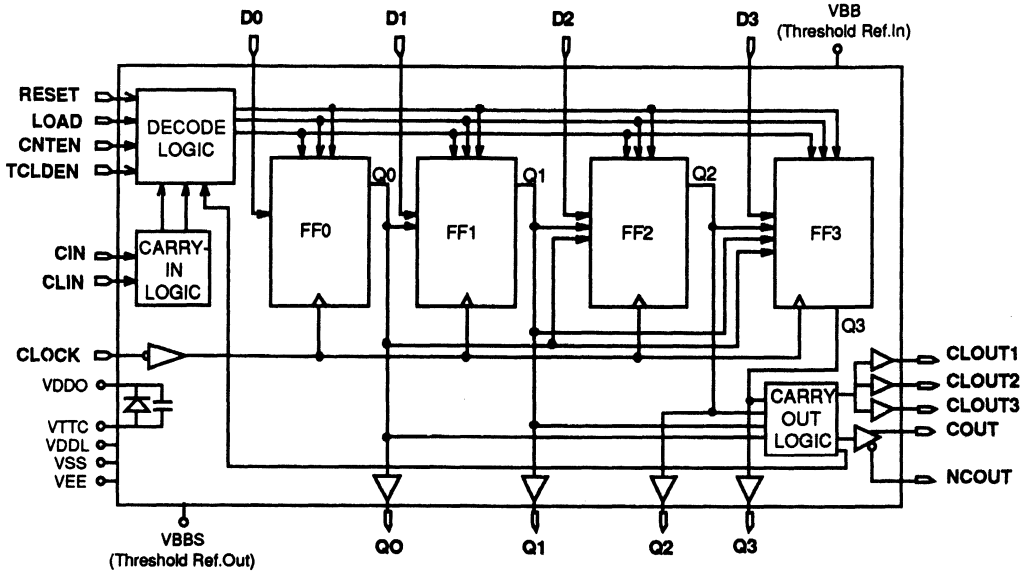
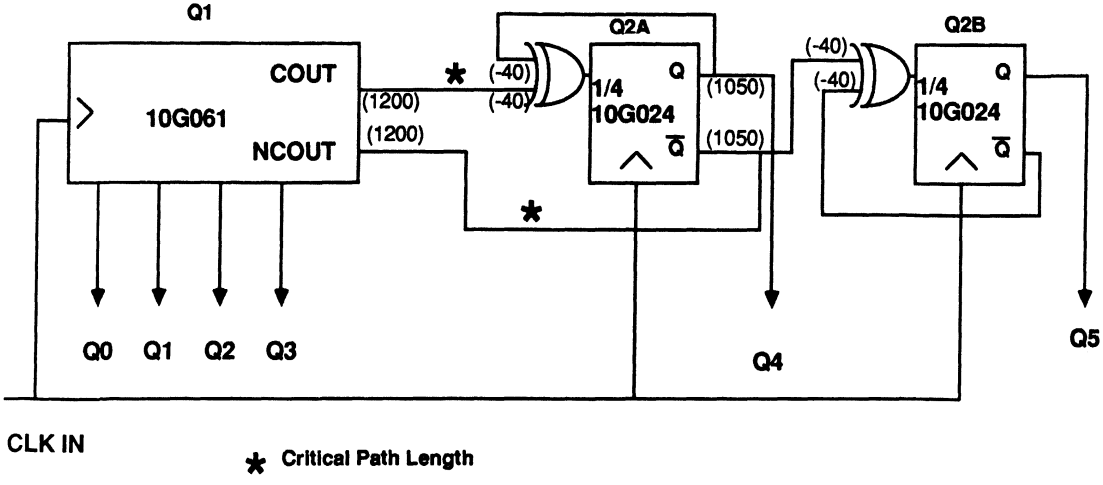


FIGURE 6: 10G061 Block Diagram



FIFURE 7: The 10G024 can expand one or more 10G061 4-bit synchronous counters by 2 bits at the MSB end.

APPLICATION OF THE 16G040 CLOCK AND DATA RECOVERY CIRCUIT

Application Note #7 By: Carl Eggert Deierling

I. INTRODUCTION

The normal nature of data processed by logic is in the NRZ (Non-Return-to-Zero) form. A bit remains either high or low for an entire clock cycle, thus the bandwidth necessary to pass this data is only one-half the data rate. RZ (Return-to-Zero) schemes must have a complete 1-0 transition for every bit equal to 1, thus requiring bandwidth equal to the data rate. Many low frequency serial communications schemes use the NRZ format and assume complete clock accuracy between the transmitting ends. Some of these, such as asynchronous communication schemes used for low data rate modems at 300 and 1200 Baud, use a START bit and STOP bit for each word of 6,7,8, or 9 bits in length. This represents roughly a 22 -33% overhead and requires oversampling at several times the data rate. Higher baud rate modems are available (e.g. 4800, 9600 Baud and 19.2 kilobaud) which send characters in larger synchronous blocks; a large preamble including SYNC characters to synchronize the block obviates the START and STOP bits. All of the aforementioned employ oversampling methods as opposed to clock recovery schemes. Clock recovery at lower data rates may be performed by using Manchester or Miller encoding schemes which are "self clocking" schemes. A transition occurs during every clock cycle, simplifying clock recovery. RZ and Manchester encoding methods however require that bandwidth be equal to the data rate, since a complete 1-0 cycle must occur during a single bit time (A Manchester encoder and decoder scheme using PicoLogic™ was shown to operate in excess of 400 MBaud by T.G. Palkert[1]). Miller encoding, while not doubling bandwidth requirements, imposes difficult encoding and decoding algorithms due to the fact that consecutive zeros are encoded as transitions at the edges of the clock and ones are encoded as transitions in the center of the clock period; the polarity of the transition conveys no information. **Figure 1** illustrates the various encoding forms discussed above with the polarity exchanged from the customary telecommunications convention employed to show a "ONE" as a high.

At extremely high data rates, transmission of NRZ data is thus extremely important since twice the data rate can be supported for a given system bandwidth. Likewise, the large overheads associated with asynchronous communications schemes is wasteful of precious bandwidth, and oversampling at multiples of the data rate is impractical at gigabaud data rates. For this reason a clock recovery scheme which will operate from NRZ data at gigabaud rates is an important element in fiber optic communications. An approach which has been popular for some time employs a Surface Acoustic Wave (SAW) resonator which is tooled for a fixed frequency. It offers an extremely high Q at this frequency, and the incoming data operating at (or at a subharmonic of) the resonant frequency of this SAW resonator will excite it into oscillation. Disadvantages of this approach are high cost, loss of clock with loss of data, intolerance to eye closure, and lack of flexibility. For any given application at a certain frequency a new resonator must be designed and tooled. Cost, and size are recurring constraints on their use, while non-recurring engineering costs and development time militate against their design-in. GigaBit Logic has developed the 16G040 integrated circuit and prototyping and OEM modules employing a phase-lock-loop (PLL) which can be used for recovering the clock from NRZ data operating in excess of one gigabaud. The use of the 16G040 and the 90GCDR will be described in detail in the following discussion.

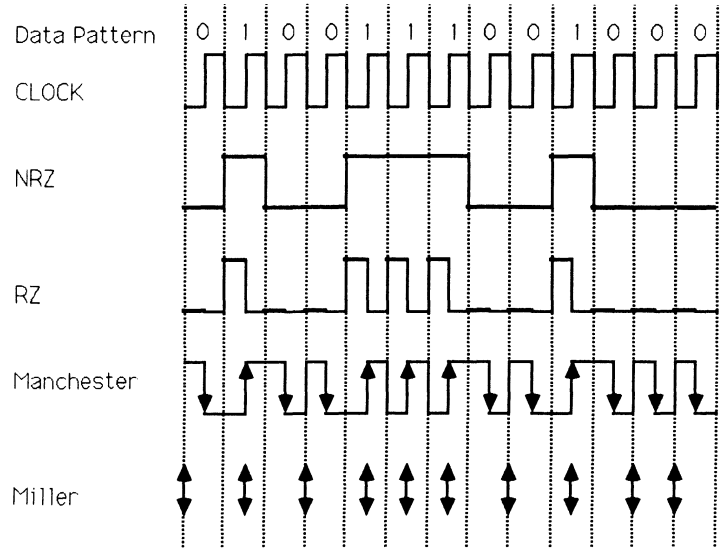
II. PHASE-LOCKED LOOPS AS CLOCK RECOVERY ELEMENTS

This application note will not attempt to reiterate the myriad technical literature readily available on PLL[2,3,4,5], but will instead provide an overview and emphasize the aspects unique to 16G040 operation at high frequencies using data instead of a reference oscillator. (Refer to the Appendix for PLL equations applicable to the 90GCDR board and to the 16G040 data sheet for additional relevant information.) A major advantage of a PLL is its ability to suppress noise superimposed on its input signal. Therefore this technique is a natural for fiber optic applications where the data eye may be small due to noise and distortion.

Phase-Locked-Loops (PLL's) have long been used in synthesizing clocks of selectable frequencies from a fixed reference frequency. The basic concept is to use a phase frequency comparator (PFC) to compare a reference frequency (R) to a VCO oscillator frequency (V), and generate a signal of polarity and amplitude proportional to the phase difference between the two sources. After amplification and low pass filtering, this output will provide an error signal to correct the VCO. One or the other of the frequencies will generally be divided by a programmable counter, depending on whether the desired output is higher or lower than the available reference frequency. Type 3 and type 4 PFCs both generate a signal which indicates whether the VCO's phase is leading or lagging that of the reference and whether it's frequency is greater than or less than the reference source, causing the VCO to be slowed or accelerated respectively.

It would appear that applying this PLL principle to clock recovery is natural. The incoming data can provide the reference (R) and the VCO will be locked to it. This VCO then becoming the recovered clock. A difficulty arises due to the fact that the data received is not a continuous string of alternating ones and zeros. A conventional PFC will interpret the absence of a data transition as the VCO severely leading the reference, and will attempt to "correct" the VCO by slowing it . The 16G040 uses a clocked scheme to circumvent this problem.

FIGURE 1: Miscellaneous Serial Data PCM Methods



Bold Lines and Arrow Heads indicate Significant Level or Transition

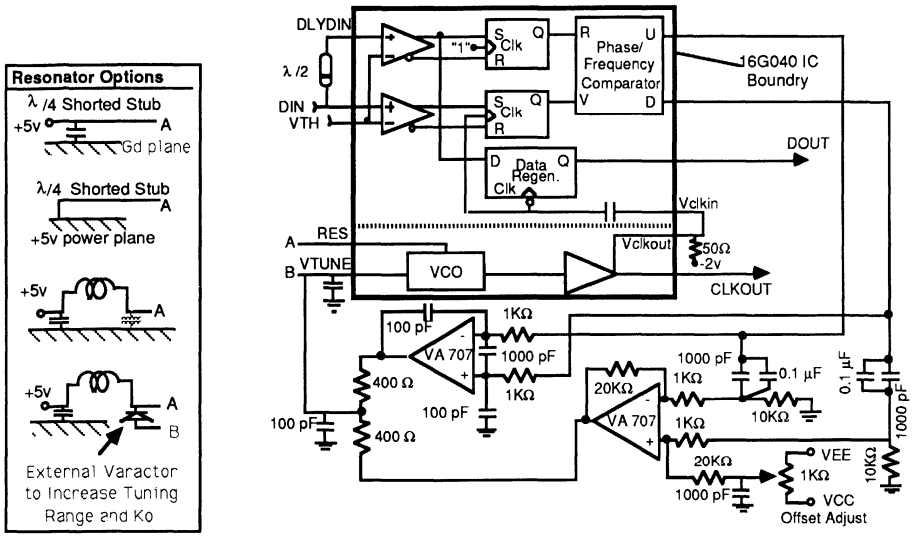
III. ELEMENTS OF A CLOCK AND DATA RECOVERY CIRCUIT

Figure 2 is a block diagram of a typical clock recovery PLL system employing the 16G040. There are three major ingredients: VCO, loop filter with its amplifier, and clocked PFC, with the 16G040 providing all necessary elements except for an external delay line, the loop filter, and the resonator necessary to establish the VCO center frequency. Each of these three major blocks will be individually described.

A. Voltage Controlled Oscillator

The VCO (see **Figure 3.**) is designed so as to provide complete flexibility of frequency. The oscillator itself consists of a tran-

FIGURE 2: 16G040 Clock & Data Recovery Block Diagram



sistor whose drain is connected to the RES(inator) pin. This drain also has an internal 0.5 to 1.5 pf varactor (actually implemented with three series diodes for reasons to be discussed later) connected between the RES pin and the VTUNE pin. To permit a wide range of oscillating frequencies, the inductance necessary for parallel resonance (with the varactor and package capacitance of approximately 1.5 pf) must be supplied by the user. This inductor may take the form of a lumped element inductor at frequencies below approximately 750 MHz, or as a shorted stub slightly shorter than λ/4, providing the required inductance at frequencies above 750 MHz. Operation with both air core and high frequency high Q ferrite tuned slug core inductors has been verified. A lumped element capacitor may also be connected to the resonator input to further reduce the frequency, however it should be noted that additional capacitance will reduce the VCO gain and range. Placing a varactor between the RESonator pin and the VTUNE pin will decrease the frequency and increase the VCO gain and tuning range. The VCO has two source follower outputs, one of which (VCLKOUT) is generally fed to the Phase Frequency Comparator, where it reclocks the incoming data, and the other (CLKOUT) is supplied as the recovered external clock source. Since these are conventional source follower outputs with PicoLogic™ levels, both outputs must either be terminated to a negative supply or pulled down at the source to a negative supply if series termination is employed.

VCO RANGE AND GAIN

The tuning range of the VCO with a fixed tank circuit will limit the maximum frequency range over which the part may capture and hold lock. Since the only variable is the varactor with a range between 0.5 and 1.5 pf, a small percentage of the reactive component, the tuning range is restricted. It has a range of approximately ±50 MHz at 1 GHz (±5%); ± 15 MHz at 600 MHz (2.5 %), and 1.5 MHz at 100 MHz. It would appear that the percentage tuning range would be identical at all frequencies, however the lead inductance of the package in series with the parasitic capacitance adds a +jωL to the -j/ωC, effectively canceling some of the parasitic capacitance at the higher frequencies and increasing the effect of the varactor capacitance. The temperature coefficient of the VCO with its resonator will generally range between -30 to -60 KHz/°C at 400 MHz if not otherwise compensated. This includes both the temperature coefficient of the

circuit as well as the temperature coefficient of the λ/4 stub, which will elongate with increasing temperature. A readily available negative tempco capacitor (e.g. N750) can be used to compensate for this drift at low frequencies. At higher frequencies where additional capacitance could not be used, the tuning range is sufficiently large to accommodate the drift. It should be noted that a varactor could also be employed which would increase the tuning range, however use of same will decrease stability and therefore prove undesirable in many cases.

Since the capacitance of a varactor is highly non-linear with applied voltage, the gain of the VCO is not fixed even at a given frequency. In this case the varactor consists of three series diodes, whose anode is brought off chip as VTUNE, and whose cathode goes to the drain of the oscillator to form the parallel resonant circuit with the external stub or inductor. This drain must be supplied with VCC = +5 volts through the inductor or stub. The swing on the drain of this transistor will nearly encompass the range between 0 and + 10 volts. If the control voltage VTUNE is taken positive, it is possible for the diodes to become forward biased as the drain swings to ground, thereby greatly reducing the Q of the circuit and killing the oscillator. For this reason it is essential to limit the maximum VTUNE amplitude to approximately +2.5 volts, the drop of the three diodes when conducting.

The low reverse bias state of a varactor diode is also the condition of maximum capacitance and the region of maximum varactor gain $K_v = \partial C/\partial V$. The gain of the VCO, K_o is related to the gain of the varactor according to the resonant circuit equation $f_o = (1/2\pi)\sqrt{LC}$, hence K_o is also nonlinear (although not as severely due to the square root in the equation) and also restricted from reaching its maximum value at the most positive VTUNE voltages. In the VTUNE range which is viable for this part (-5 to +2.5 volts), K_o may be calculated for any frequency using the aforementioned tuning ranges. K_o is generally expressed in MHz/Volt, but because the VCO can operate over a wide range of frequencies and the gain is a function of frequency and voltage, it should actually be referred to as Ko(f,v) to denote this frequency dependence. The curve of Ko(f,v) versus frequency for the packaged device is given in the data sheet. To permit example equations to be employed the nominal value of Ko at 600 MHz will be used and for simplicity Ko(f,v) will be hereafter be referred to as Ko. It has been determined that the Δf is approximately 30 MHz for the maximum V of 7.5 volts; Ko = 4 MHz/Volt @ 600 MHz. One word of caution applies. The VCO could operate anywhere within its range; the nonlinear relationship between VTUNE and the Capacitance could be as much as 4:1 over the range of operation, hence Ko could vary by a factor of 2:1 at a given frequency due to the fact that the resonant frequency is proportional to the square root of the capacitance. This factor must be taken into account when ascertaining loop stability.

TUNING

The VCO should be tuned to the desired clock frequency (i.e.the incoming NRZ data rate or twice the RZ or Manchester data rates) with zero volts on VTUNE at the middle of the temperature range antici-

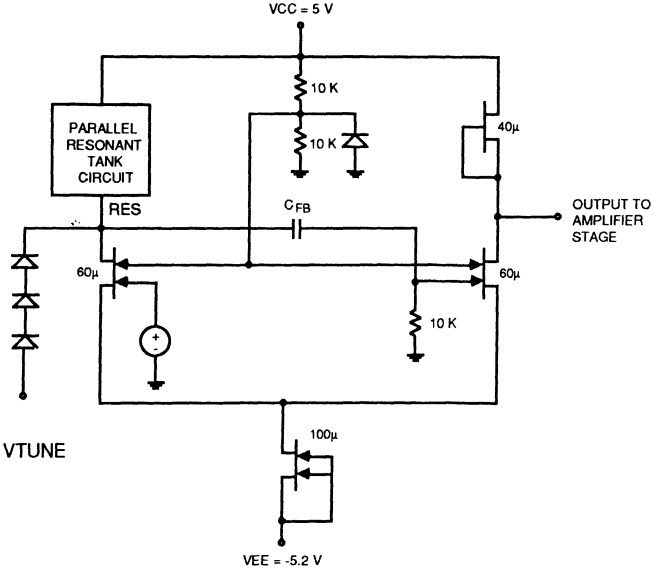


FIGURE 3: Schematic of the 16G040 VCO

Figure 4a. Pre-filter Equivalence to Minimize Transient Response Requirements of OPAMP

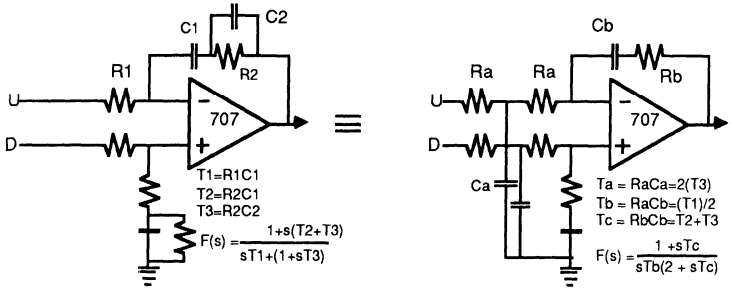
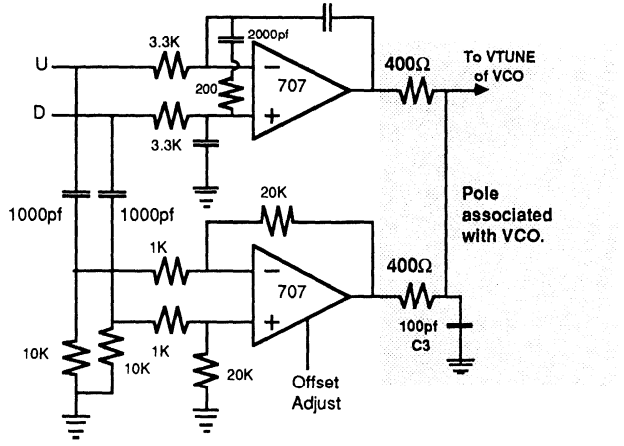


Figure 4b. Dual Path Loop Filter to Assure Retention of Beat Note



pated. This may be readily accomplished by shorting VTUNE to ground (VDD) and adjusting the tank circuit for resonance. The 90GCDR demonstration board provides a length of microstrip transmission line adjacent to a VCC plane which may be used as a resonator for data rates to 1 gigabit per second. A piece of wire or braid may be used to short between the microstrip and the VCC plane, providing both the stub and the VCC bias essential to proper operation of the VCO. This "short" may be slid along the line using a pencil eraser to locate the proper position for the desired frequency, and subsequently soldered in place. Either tunable inductors or capacitors may be used to adjust the center frequency with a lumped element tank circuit, but as previously stated, VCC must be applied to the "cold" end of the tank circuit. One feature of the stub is that a capacitor could be placed at any location on the microstrip, which will result in a transformer action of the capacitor. The capacitance for a given value capacitor will be reduced as it is moved from the IC towards the "cold" end of the stub.

QUALITY FACTOR REQUIREMENTS

At high frequencies the gain of the oscillator will be reduced, hence a higher Q is required. For this reason high frequency ferrite slug tuned inductors with inherently lower Q will cease to provide oscillation at frequencies above a few hundred MHz. Air core inductors may be either elongated or compressed to provide a degree of tuning, or many types of variable

capacitors have been designed for these frequencies. One other additional effect should be noted at higher frequencies relating to the Q of the circuit board. The dielectric for the quarter wave stub used as a resonator should be of a lower loss material than glass epoxy if operation above a few hundred MHz is required. The 90GCDR board utilizes a PTFE material for the top layer, and the characteristic impedance Z_0 is set to approximately 30Ω. This lower impedance maintains a higher Q in the presence of dispersion or other losses which could be represented on an equivalent circuit as a shunt resistor. It has also been found that plating the microstrip with gold may actually have a detrimental effect on the Q. Generally, a rather thick layer of Ni is plated on the Cu to act as a barrier before the thin layer of Au is plated. However at the frequencies of interest the skin effect manifests itself. Since the Au is so thin, a large percentage of the signal is displaced into the Ni; a rather poor conductor, resulting in a lossy, low Q resonator. Two solutions to this dilemma are possible. One is to avoid all plating and suffer the consequences of poor appearance as copper oxidation sets in; the second is to use an Ag barrier rather than Ni. If cost were no object the Au plating could be sufficiently thick so as to contain the entire field.

B. Phase Frequency Comparator

The Phase Frequency Comparator section of the 16G040 (See **Figure 2**) consists of a pair of differential comparators followed by a pair of flip flops followed by the Phase Frequency Comparator. This block generates fixed amplitude output pulses on the U and D outputs whose duration is proportional to the phase difference between the internal R and V signals. The flip flop which develops the V (for VCO) signal derives its data input from the incoming data stream through the pin labeled DIN. This flip flop is clocked by the VCO which is externally connected to the VCLKIN pin thence internally a-c coupled to the clock of the flip flop. This internal capacitor is sufficiently large to support frequencies to below 10 MHz. This flip flop regenerates as its V output, the data input signal delayed in time by VCLKIN. Data externally delayed by a half bit time is applied to the second, unclocked, flip flop which generates the R (for Reference) input to the Phase Frequency Comparator. The R and V inputs to the phase frequency comparator, when in phase, will result in equal amplitude and duration pulses on the U and D outputs, which when subtracted and integrated by the loop filter will yield zero error signal being applied to the VCO. If these two signals are in phase and DLYDIN is delayed 1/4 to 1/2 bit time from DIN, the clock will sample the data midpoint in its stable state, i.e. the center of the setup and hold time window of the V flip flop. This will yield the maximum $\pm \pi$ radians range; shorter delay times will result in earlier sampling reducing the range, however functionality will be maintained. Longer than half bit time delays will result in poor operation from the PFC and should be avoided. If data remains in either the high or low states the registers will both retain that state and both the U and D outputs of the PFC will thus remain low; a no-error condition, providing no correction signal to the VCO, hence maintaining the frequency at status quo. DC offsets in the OPAMP or PFC outputs, as well as initial tuning of the VCO not falling precisely at midrange, will all contribute to a slow drift in the absence of data transitions. The 16G040 and 90GCDR board have been verified with a 2^{23}-1 pseudo-random noise code to assure that a string of twenty-three 1's or 0's could be tolerated without the loss of lock. In most cases stability of the aforementioned elements is not this critical due to a much less stringent encoding scheme employed as described earlier.

The PFC has source follower outputs with active pull-downs, however external pulldown resistors are essential to proper operation. Since a zero error condition is represented by both the U and D outputs of the PFC being in a stable, well-defined low state, the pulldown circuit on the output can have a significant impact on the levels, and is thus critical to proper operation. The schematic for the CDR board (See the 16G040 Data Sheet) illustrates a circuit which has been found to yield equal low levels for both the U and D outputs as seen by the amplifier after the voltage divider action. Any differences in output low levels will represent a continuous error, which must be corrected by the PLL. The data inputs can be either a-c or d-c coupled. If a-c coupled and if VTH is biased at

precisely -1.3 volts the PFC will generally direct the VCO to go to the low frequency end of its range in the absence of data inputs (i.e. larger signals on D than on U. With no input signal VTH should be adjusted until both outputs go and remain low in the absence of data transitions for either the d-c or a-c coupled cases.

The gain of the PFC will generally be relatively constant over the entire operating range, except for a reduction to approximately 1/3 normal at the cross-over point. This results from that fact that near the null position of the comparator the pulses from the U and D outputs are extremely narrow, and the 150 to 200 ps rise and fall times are so slow as to reduce the $\int Vdt$ for narrow pulses,. Output edge rates are insignificant for larger errors represented by wider pulses from U and/or D. Note that these edge rates are significantly faster than that achievable with silicon based IC's leading to vastly superior performance for this GaAs part. The detector gain of the PFC for large signals is represented by K_d and typically equals 0.2 v/rad or 3.3 mv/degree, however as mentioned earlier, a gain reduction of 1/3 at the null point will be realized.

One other gain factor exists which is completely application dependent. This is the richness of the clock contained in the data. An alternating pattern of 1's and 0's would have a gain factor of 0.5 (1/2M) due to the fact that the incoming NRZ data has a transition only half as often as the VCO clock. The term 1/(M) may be defined to be the number of data transitions received divided by the maximum possible number (i.e.alternate 1's and 0's). If, for example, transitions occur on average half of the possible times, 1/2M is reduced to 0.25; if data has only one transition every 8 bits this yields a 1/2M factor of 0.0625 by which K_d must be multiplied. Unfortunately this may vary considerably in a given system, but as before, all possible values must satisfy the stability criterion. The constraints which low values of M place on the loop filter should not be overlooked. This factor defined as M is analogous to the VCO division factor N found in synthesizer equations, and will have identical effects on operation. During acquisition it would be desirable to increase M to near unity to assist in the acquisition process. If M may be a low value once the the clock recovery system is locked, a slow loop filter will be required to prevent loss of lock during absence of data, thus increasing the time to capture.

It is desirable to maintain this factor M at a maximum average as well as reduce the maximum length of 1's or 0's called the maximum "run length" (Y). Since NRZ data itself places no such restrictions, some alternate scheme must be employed. Elimination of DC and low frequency components not only improves the performance of a clock and data recovery system, but it also improves the performance of the fiberoptic or electromagnetic transmission line links. Two alternate schemes which have been employed are scrambling or mixing the data with a pseudo-random code, and encoding the data into a transmission code. In the first case, a pseudo random code is XOR-ed with the outgoing serial data stream. This could be accomplished by using the 10G022 as a P/N generator and the 10G002 as the XOR. At the receiving end of the transmission, this same P/N code synchronized to that of the transmitting end is XOR-ed with the recovered scrambled data using the same two parts. This will descramble the data received and recover the original data. This scrambling method a disadvantage: an incoming data stream which equals, during a given interval L, the P/N code or the compliment of the P/N code generated, will when XOR'ed with this identical code result in a run length equal to L which is statistically unlimited in length. However this scheme has the advantage of not increasing the bandwidth requirements of the system.

A far preferable method for eliminating low frequency components has been developed through the use of transmission codes. In these schemes the original code is encoded into one of two redundant codes containing one or more additional bits. For example the 5B/6B code converts the unencoded 5 bits into one of two 6 bit codes. The code selected for transmission is based on the historical value of the data previously transmitted. A plurality of 1's will result in the code being selected which has a majority of 0's. The receiving end requires less intelligence and no cognizance of past history, since either of these codes is decoded back to the original unencoded data. The only disadvantage to this scheme is the required logic for encoding and decoding, and the increase in band-

width requirements. Five bits are transmitted for each four bits of data resulting in a 25% overhead. This 5B/6B code is quite popular, however it requires additional high speed logic to interface to the byte—multiple byte-wide world. Since information is generally transmitted in packets containing pre-defined fields which are modulo eight bits, the 4B/5B code can be used on a nibble basis, however this code while guaranteeing a maximum run length (Y) of 4 does not completely eliminate d-c components. Larger codes such as 8B/10B are most compatible with byte oriented elements. To avoid the longer runlength of 8 which would be inherent in this code, IBM6has developed an 8B/10B code which is comprised of a 3B/4B and a 5B/6B code with a resulting maximum run length of 5.

Another factor which must be considered relating to the input data is the low frequency component of this data. If the input data is a-c coupled then all capacitors relating to this data must be of sufficient size to avoid baseline wander. For example the 90GCDR board has AC coupled input data and decoupling at the bottom of the termination resistor as well as a-c coupled outputs. Capacitors C4, 5, 6, and C49 are all examples of capacitors which should have reactance <<50Ω at the lowest data rate. (Refer to the 90GCDR schematic in the 16G040 data sheet)

C. Loop Filter and Operational Amplifier

This is the part of the circuit which permits complete customization to meet system requirements. Tradeoffs between capture speed and loss of lock time, as well as the ability to alter these pre- and post-lock, are all facilitated by the loop filter. The loop filter is generally active in modern PLL circuits. In this case, U and D outputs from the PFC must be subtracted from one another and integrated. Therefore, an operational amplifier used as a differential summing integrator is required. It is important to have the passive elements of this integrator determine, to the maximum possible extent, the poles and zeros of the entire PLL, since discrete component R's and C's possess precise stable values. This contrasts with the vagaries of active circuits, poles and zeros caused by f_t's, parasitic capacitances, active output and input impedances, etc. which may be temperature and voltage dependent as well as be subject to processing variables. Most active integrators are designed to be second order, possessing a pole at 0 or some low frequency and a zero at some intermediate frequency.

90GCDR LOOP FILTER EXAMPLE

Reference the Appendix for the loop filter used in the 90GCDR. A high frequency pole, which is low enough to dominate over the omnipresent parasitic pole of the VCO, appears between the output of the OPAMP and the input to the VCO and, while given in the figure and shown on the Bode plot as T3, is considered to be associated with the VCO, not the loop filter. Due to the pole associated with the VCO the order of any PLL is always one greater than the order of the loop filter. In the case of the 90GCDR, the output of the loop filter goes to the VTUNE input of VCO which is the anode of the varactor. One element of this pole is an external capacitor (C3) of 100 pf, which must be connected between VTUNE and a good RF ground since this capacitor is in series with the varactor and should have negligible reactance compared to the capacitance of the varactor to maintain Ko, the VCO gain. In this case the bandwidth of the VCO is quite high compared to this last pole, since GaAs is the substrate and low bandwidth filters are employed to reduce jitter. Note that for the 16G040, the U output of the PFC drives the - input while the D output drives the + input of the OPAMP. As the output of the OPAMP goes in a positive direction the bias across the varactor is reduced, it's capacitance increased and the frequency is thus reduced. Reference the Appendix for additional quantitative data on the loop filter employed by the 90GCDR. The first parasitic pole of most OPAMPs will generally be less than 1 MHz. The amplifier selected, the VA707, has its first pole at 8 MHz and unity gain bandwidth to 200 MHz when lightly loaded. Other undesired poles should be at frequencies well beyond the last pole of the entire PLL such that the gain is so low as to make them negligible.

OPERATIONAL AMPLIFIER TRANSIENT LIMITATIONS

The inputs to the OPAMP emanate from the phase

frequency comparator portion of the circuit. These outputs have slew rates approaching 100 V/μs, far in excess of the capability of the inputs of a conventional silicon OPAMP (even the VA-707 OPAMP manufactured by VTC) to track properly. Although this OPAMP is extremely fast by silicon standards, the input slew rate remains an issue. Schemes are available to limit the input slew rate seen by the amplifier by incorporating a low pass R-C-R "Tee" pre-filter prior to the input of the OPAMP. Proper design will yield an equivalent circuit to that of a conventional third order active design. A pre-filter circuit may be incorporated with a new second order active filter design such that the overall transfer function F(S) equals that of the original as described by Przedpelski[7] and illustrated in **Figure 4a**. However the final pole caused by the RC from the output of the OPAMP to the VTUNE, and, as previously mentioned necessary, would result in a third order filter or fourth order PLL. Unfortunately, this fourth order PLL becomes extremely complex, hence this pre-filter scheme has not been implemented, but benefits are anticipated.

OPERATIONAL AMPLIFIER SATURATION LIMITATIONS

One other factor can influence the performance of the operational amplifier in this application. If the amplifier is driven into either the upper limit (dictated by the string of three diodes shown in figure 2) or the lower limit imposed by the negative power supply rail of the OPAMP, it will become saturated and its gain reduced to zero. This will inhibit the beat notes (difference between VCO and the frequency of incoming data) from passing through the amplifier and assisting in the acquisition process. For this reason the circuit given for the 90GCDR loop filter design mail fail to capture if the OPAMP is pegged, limiting its capture range to below the lock range. An alternative scheme has been devised which will permit passing the beat notes though a second amplifier. This is illustrated in **Figure 4b,** and its operation has been verified demonstrating increased capture range and stability.

IV.CONCLUSIONS

The CDR which is offered in either die, packaged part, prototyping, or OEM module forms is very effective in recovering the clock from NRZ data, and may be used to recover clocks from other data types as well. The high edge rates available from the phase frequency comparator assure adequate gain even with only minor phase differences between received data and the synthesized clock, minimizing clock to data jitter. The PLL nature of the product renders it particularly effective in clock extraction in the presence of noise. While designing the loop filter to properly interface with the 16G040 requires some servo engineering background, many computer programs are available which will assist in this endeavor. Indeed, it has been noted[8] that, contrary to the norm, synthesis is easier than analysis using existing closed form equations. The availability of pre-designed loop filters and OEM and prototyping modules which may be customized by GigaBit Logic for a particular data rate, nature, and capture requirement, relieves the user from this task.

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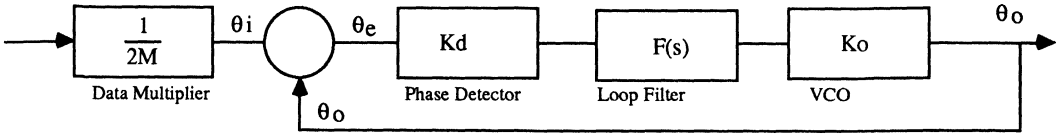
APPENDIX

Phase Locked Loop Equations



ω_n = Natural Frequency = $\sqrt{\frac{KoKd}{T1}}$ $\quad \zeta$ = Damping Factor = $\frac{T2}{2}\sqrt{\frac{(KoKd)}{T1}}$

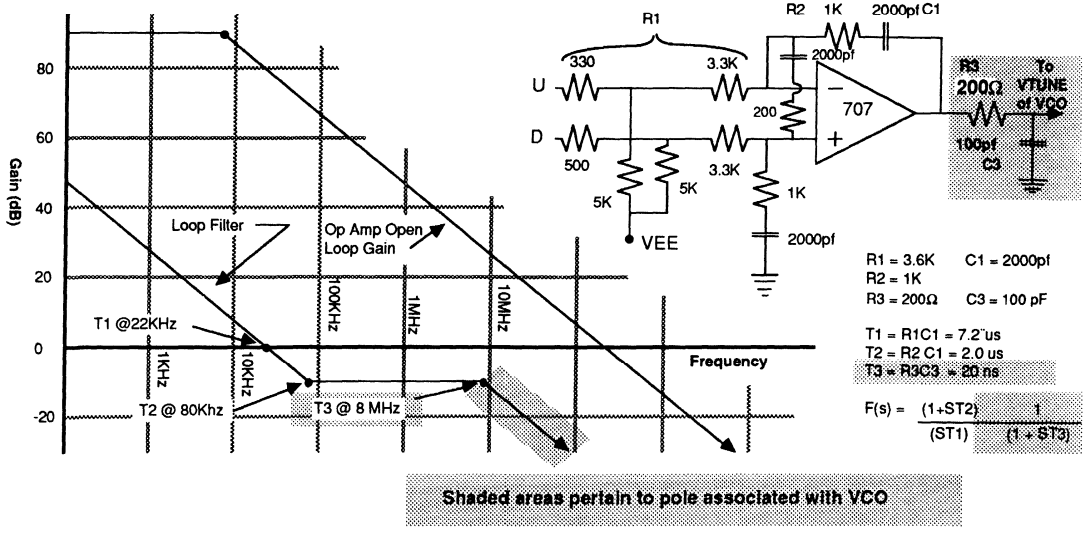
$$H(s) = \frac{2\zeta\omega_n s + \omega_n^2}{S^2 + 2\zeta\omega_n s + \omega_n^2}$$

Lock Range = $\Delta\omega_L = 2\pi\zeta\omega_n$

Pull-in Range = $\Delta\omega_p = \pi\sqrt{2\zeta\omega_n KoKd}$

Hold Range and Tracking Range are limited only by VCO Range

Bode Plot of 90GCDR Second Order Loop Filter with VCO Pole Shown



GaAs IC TESTING METHODS

TABLE OF CONTENTS

GaAs IC Testing Methods

I. Standard Test Flow

Production IC testing at GBL consists of 2 major testing processes, DC testing (performed at probe, pre-, and post-burnin), and AC testing (performed at final test on packaged parts). The exact test flow varies somewhat with the type of product (standard PicoLogic, extended temperature tested devices, or ASIC's), but the general DC and AC test methods used are common to all.

II. Product Characterization

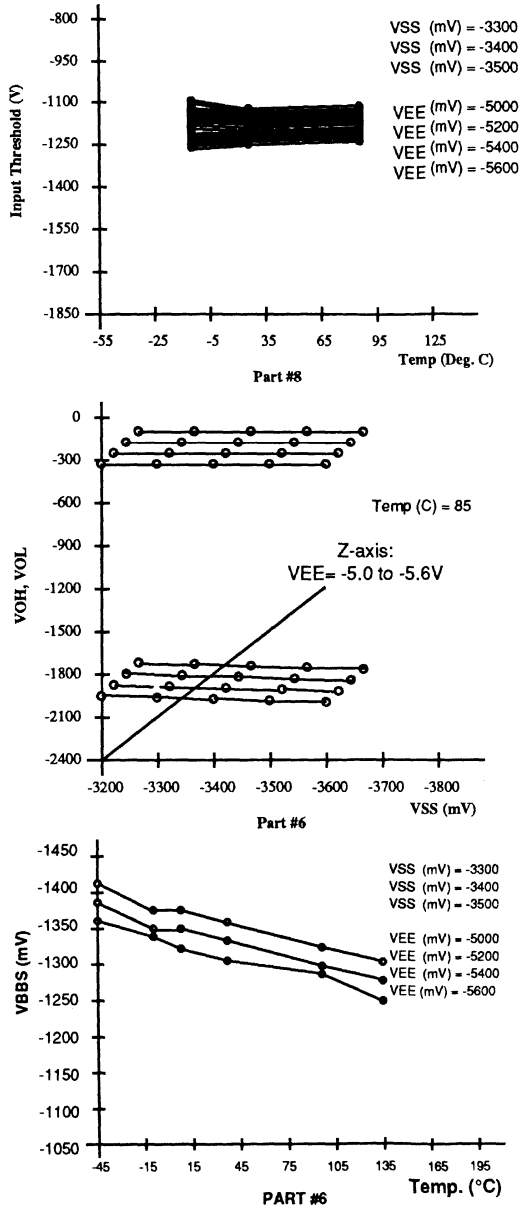
GigaBit Logic products are characterized thoroughly prior to release to production. This characterization measures product performance over supply voltage and temperature extremes and includes product samples taken from material representing a wide range of wafer process variation. The characterization process is structured in such a way that products which have successfully run the characterization "gauntlet" will yield well and perform well in production. The measurement data collected during characterization is used to formulate the product specifications and provides the basis for the guardbanded tests used in production to assure full adherence to spec (see Figs. 1 and 2).

Product Characterization Supply/Temperature Matrix

VSS	VEE	Temperature
-3.2V	-5.0V	125°C
-3.3V	-5.2V	85°C
-3.4V	-5.4V	25°C
-3.5V	-5.6V	0°C
-3.6V		-40°C
		-55°C

Products are characterized at all combinations of the voltages and temperature in the table above. Characterization samples represent a range of process parameter values within the acceptable process limits.

Figure 1.



Products are characterized over extremes of supply and temperature to establish specs and test guardbands.

Figure 2.

The characterization data is used to validate key assumptions made regarding production test requirements for each product. These assumptions are:

- Validity of using guardbanded limits during room temp testing to assure full temp range performance.
- Validity of testing selected AC parameters to guarantee performance to all AC parameters in the product spec.

III. DC Test Methodology

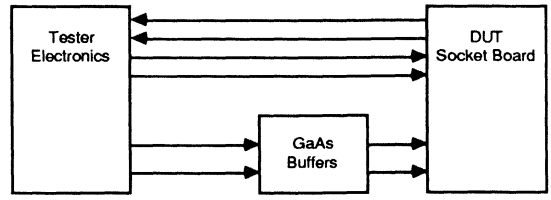
What GigaBit refers to as "DC testing" is really all parametric and functional testing performed at test vector rates significantly less than the spec'd clock rate of the product. For digital GaAs IC's operating at 1 to 2 GHz, this definition of "DC test" includes virtually any testing that could be accomplished on present commercially available (10 MHz to 100 MHz vector rate) test equipment. The purpose of "DC test" is to measure DC parametrics (power supply and I/O parameters) and to check the logical functionality of the IC at slow speed. GBL has found this test procedure to be very effective at probe, pre-, and post-burnin test points for the following reasons:

-The equipment used is readily available and relatively inexpensive. (GBL uses Megatest Q2/52 and ASIX testers.)
-Production products which pass DC test at these test points have high yields at AC test. (Greater than 90% of the parts will fall into an acceptable "speed bin" at AC test.)

IV. DC Test Issues

At DC test, the testing of GaAs IC's is relatively straightforward. The equipment is basically the same as is used for silicon digital IC's. Some additional care must be taken in constructing loadboards, socketboards, and probecards to assure proper supply bypassing and maintain fast edge rates for DUT clock signals (see Fig. 3). Use of chip caps as close as possible to DUT supply nodes, and use of coax lines on

DC Test Hardware Configuration



Tester drivers should be buffered to provide fast edge-rate signals to critical DUT inputs such as clock inputs. GaAs IC's such as 10G002, 10G004, 10G012, or 16G061 are possible buffers. The Tektronix PG502 Pulse Generator (< 1Nsec rise and fall times) is another alternative.

Figure 3

critical DUT input lines is advisable. If driving a clock input on the DUT with a slow slew-rate (>1 ns) tester driver channel, it may be necessary to buffer the driver with a GaAs buffer circuit to sharpen the edge rate of the clock. (GBL PicoLogic parts 10G002, 10G004, 10G012, or the new 16G061 are useful for this purpose.)

Test vector programming and timing is easier, in theory, than it would be for silicon parts since no AC parameter testing is to be done. However, care must be taken in setting up simple vector timing so as not to run afoul of the GaAs DUT's capability of interpreting ringing transients as multiple clocks or of viewing slightly skewed data channels within a single vector time as multiple vectors. As noted previously, signal integrity on clock lines is very important. It is also important to remember that the test programmer's usual view of "simultaneously" occurring events within a vector time is not valid for parts which can clock twice within a nanosecond. Recognize the limitations of the tester's capability to place signal edges accurately and provide appropriate timing margins. Keep clocks and DUT input strobe signals well apart in time from address or data (see Fig. 4).

V. AC Test Methodology

AC testing at GBL is performed using high frequency signal generators, oscilloscopes, and an increasing

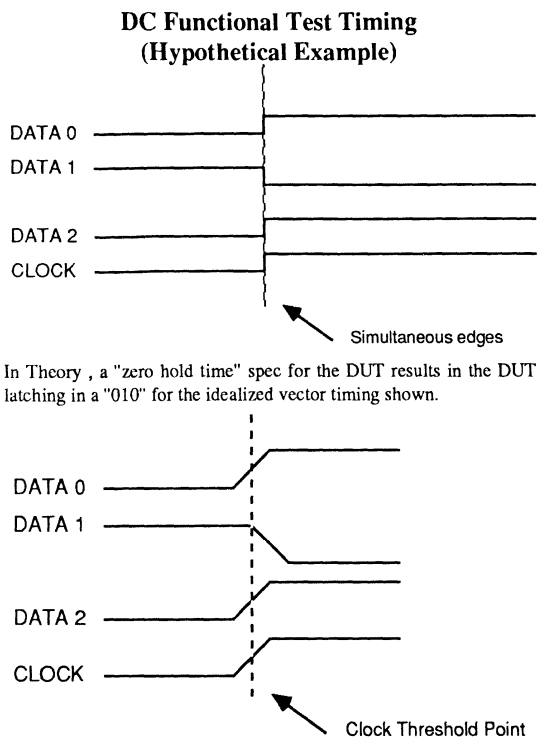


Figure 4

signal generators, oscilloscopes, and an increasing amount of GaAs IC interface circuitry. In production, tests for a particular product consist of a few key timing parameters such as Fmax, prop delays, setup and hold times, and rise and fall times. Exhaustive functional tests are generally not performed due to the cost and complexity associated with such testing "at speed".

A typical setup consists of a computer/test controller, a signal generator to provide clocks to the interface circuitry and/or the DUT, a scope to measure DUT response, and a custom-built test fixture (see Fig. 5). The test fixture provides signal routing functions and buffers data transmitted between the DUT and the computer. The test setup's capability typically mimics what might be done by an engineer sitting at a lab bench. Outputs are checked one a a time as various input stimuli are applied. For simple parts, the input stimulus is usually provided by toggling a single input with all other inputs held static so as to propagate the toggling signal thru a particular logic path to an output. All paths are tested individually in this manner. For more complex parts, GaAs circuitry is used to provide input "vectors" to the DUT and exercise it in a way which better approximates its actual operation.

As previously noted, the focus of AC testing is AC parametrics rather than exhaustive functional testing. This is acceptable given the current level of GaAs device complexity and the strong correlation of high speed functionality to the thoroughness of functional testing done previously at DC test points. As more GaAs digital functions applicable in test circuitry become available, more sophisticated test interfaces and complete testers will be built. AC tests will gradually incorporate more "at speed" functional testing and more parallel testing of output signals to accommodate increasingly complex DUT's.

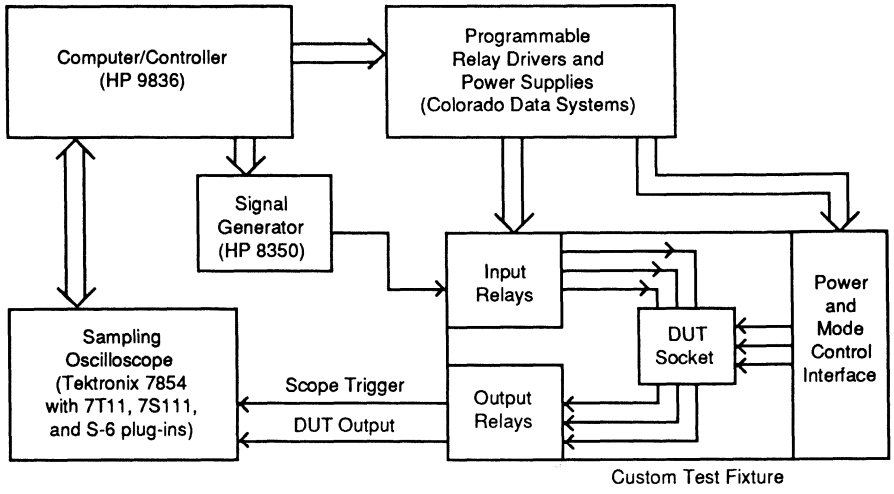
VI. AC Test Issues

Issues at AC test are dominated by 2 major considerations, DUT signal integrity and measurement system performance.

Signal Integrity

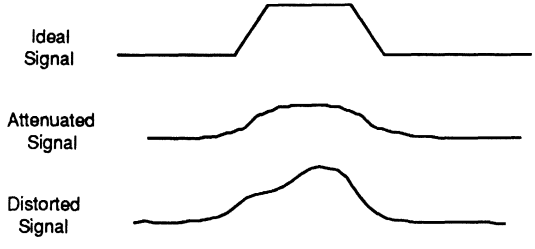
Problems can occur if input signal rise and fall times are too long, if impedance mismatch at system interconnects attenuate the signal (DUT socket contact resistance, for example), or if poor quality transmission lines attenuate or distort the signal. Signal sources should be capable of providing < 200 pSec rise and fall times, or should be buffered with GaAs circuitry. It is extremely important that signals be transmitted in a controlled, 50 ohm environment. Use of 50 ohm coax or microstrip lines is mandatory. Input terminations should be 50 ohm chip resistors mounted as close to the DUT as possible. Test system interconnects should be via SMA's, RF relays, etc, and should be minimized in number to maintain signal integrity (see Fig. 6).

AC Test Hardwire Configuration



A typical setup for AC test is shown above. The custom test fixture provides the means of interfacing all power, slow speed data (DUT "mode control") and high speed signals to the DUT.

Figure 5



Propagation of high frequency signals through transmission lines, RF relays and various interconnections results in degradation of the signal waveform due to attenuation of the fundamental and/or harmonic components of the waveform, distortion resulting from reflections, poor quality transmission media, etc. Measurement problems arise from the resulting slowed edge rates, decreased amplitudes, and distorted peaks.

Figure 6

DUT socketing is a major interconnect problem. GigaBit knows of no socket manufacturer providing a reliable high speed test socket. GBL has developed prototyping sockets which have very good high speed electrical characteristics, but which are not designed to be low insertion force, multiple insertion test sockets (See Fig. 7). Test sockets currently in use at GBL are in-house customized versions of commercial test sockets which incorporate features of our 90GSKT40L prototyping sockets . Although electrical performance is good, these sockets have less than desired lifetimes in multiple insertion use. New, longer life test socket designs are currently in development.

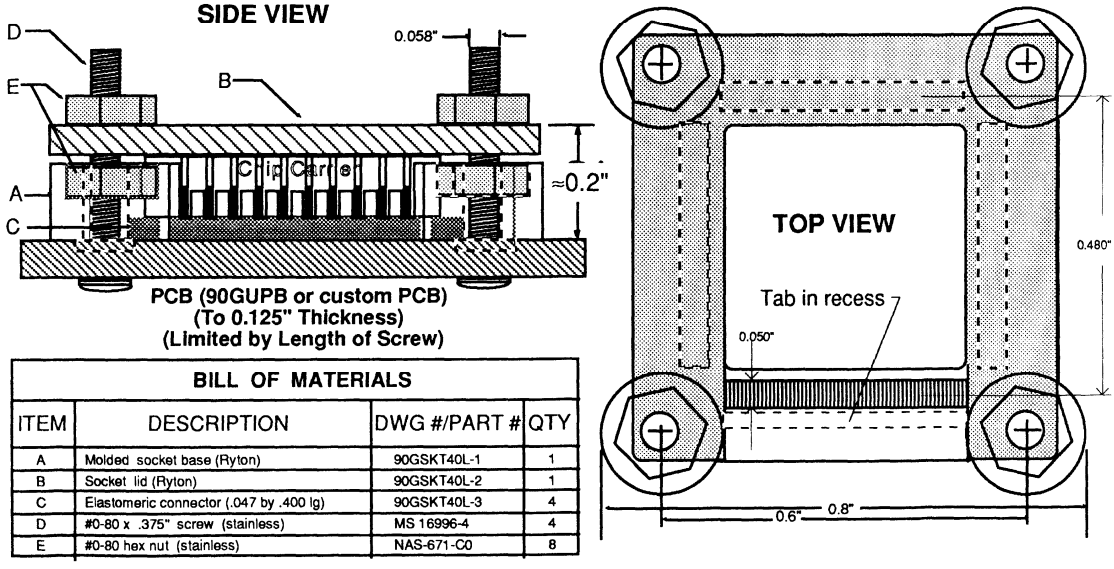
Measurement System Performance

Care must be taken in the measurement of AC parameters to recognize measurment system limitations and work around them to maximize the accuracy, repeatability, and "cost effectiveness" of the measurements. Variations in DUT output waveforms can cause prob-

lems unless the measurement system has the resolution and the mathematical processing capability to "filter" the data and calculate parameters properly.

It must be remembered that the AC parameters to be measured are relatively close in magnitude to the accuracy and resolution limits of most equipment. The process of "accurizing" the measurements often presents tradeoffs of accuracy vs. test execution time. It is important to understand the performance specifications of the measurement equipment being used in order to apply the appropriate level of multi-sampling and averaging techniques for the measurement at hand.

90GSKT40L High Speed Socket



BILL OF MATERIALS

ITEM	DESCRIPTION	DWG #/PART #	QTY
A	Molded socket base (Ryton)	90GSKT40L-1	1
B	Socket lid (Ryton)	90GSKT40L-2	1
C	Elastomeric connector (.047 by .400 lg)	90GSKT40L-3	4
D	#0-80 x .375" screw (stainless)	MS 16996-4	4
E	#0-80 hex nut (stainless)	NAS-671-C0	8

The 90GSKT40L prototyping socket provides a means of socketing the 40 I/O type "L" LCC package. (See the 90GSKT40L datasheet for more details. Test sockets with good high frequency characteristics have been built using components from this socket assembly and "latch over" type retaining mechanisms from commercially available low-frequency sockets.

Figure 7

GaAs IC Reliability and Quality Assurance Handbook

By
Ram Venkataraman

Second Edition - April 1988

Table of Contents

Table of Contents

List of Figures

List of Tables

PREFACE

Quality and reliability are fundamental requirements for the components of modern electronic equipment. The increased complexity of computer, communication, instrumentation, military and aerospace systems has raised enormously the reliability expectation of ICs. One of the uppermost user concerns of any new technology is its reliability. Hence, demonstrating the reliability of a new product family that springs from a new technology becomes all the more relevant. GigaBit Logic recognizes this fact and from its inception has evolved a strong commitment to the highest product quality and reliability.

This handbook is an updated version of GigaBit's first Reliability and Quality Assurance Report released in August 1986. This is also the first comprehensive reliability document for the digital GaAs IC industry.

We describe our approaches and procedures for generating and maintaining product quality and reliability. The reliability test results presented in this handbook show that GigaBit Logic's GaAs IC technology and product family are inherently reliable. In each chapter we have highlighted the similarities as well as the salient differences between the GaAs IC and a comparative silicon IC. This will enable the reader to see the superlative performance and reliability of our GaAs IC family.

This handbook consists of ten chapters and three appendices with explanatory figures and tables throughout the text. The first chapter "Technical Summary" is a synopsis of our quality & reliability philosophy, programs and results to date. The five chapters that follow deal in greater detail with the technology, quality assurance program, wafer fab controls, packaging and testing. The next three chapters deal with reliability theory, the reliability program and the results that we have to date. The final chapter is a summary of our conclusions and is based upon our reliability data. Handling recommendations, process control monitor (PCM) structures and references are provided as appendices.

This update incorporates the reliability statistics to date. It can be readily seen that the failure rate in FITS has improved greatly since the last report. Reliability data has also been added on our new PicoLogic devices such as shift registers and decade counters. Lifetest data on our 1K RAM, the first commercial LSI in the GaAs IC industry, has been provided. Other additions relate to new process options such as Low Pinch-off Depletion (LPD), High Margin E/D (HMED) and Enhancement/Depletion (E/D) and the activation energy results.

In the future, we plan to periodically update the reliability data in the handbook. In addition, as new products are added to the PicoLogic family, life test results will be expanded to include them.

CHAPTER I

TECHNICAL SUMMARY

GaAs Technology

Gallium arsenide, with its intrinsic high electron mobility, and semi-insulating properties has long been envisioned as the basis for future high-speed IC Technology. GigaBit Logic's PicoLogic™ family of digital ICs, have realized that vision, employing the depletion mode MESFET (D-MESFET) technology. D-MESFET is the most mature, most proven and reliable GaAs technology. D-MESFET devices are "normally on" devices requiring a negative gate potential to deplete (pinch-off) the carriers through the channel region and turn the device off. The active device regions are formed by selective ion implantation into semi-insulating GaAs wafers. The process is relatively simple with six critical mask steps. Planar device structures are achieved using "silicon-like" process steps and state-of-the-art silicon VLSI fab equipment. The gate length is typically 1μm.

The PicoLogic family is based on the Capacitor Diode FET Logic (CDFL) circuit approach and provides ultra high-speed performance with internal gate delays of 75 to 150ps with moderate power dissipation. At present, the PicoLogic family consists of SSI (NOR gates, comparators, precision D flip-flops, fanout buffers, ripple counters, variable modulus dividers) and MSI (Decoders, shift registers, synchronous counters, parity checkers, carry look ahead units, multiplexers and demultiplexers) level digital ICs. In addition, complex circuits combining digital and analog circuit elements are also available for communication (Clock and Data Recovery Circuit, Phase Frequency Comparator) and high speed ATE (Pin Driver, Time Vernier) applications.

GigaBit's leadership product - the world's first LSI complexity, commercially available 1K Static RAM (12G014) featuring an advanced registered, self-timed architecture with equal 2.5 ns read and write cycle times, is also manufactured with the D-MESFET process and an additional process step to realize cermet resistors.

In addition to the D-MESFET process, GigaBit Logic offers a recessed gate E/D (Enhancement/Depletion mode) process to its foundery customers. Key to the manufacturability, performance yield and reliability of this E/D process is insured by preserving the nucleus of the proven D-MESFET manufacturing process. Device performance is greatly enhanced through addition of a highly reproducible gate recessing step, common to both the E and D-mode devices, and the judicious optimization of several key process steps.

Reliability Philosophy

Although digital GaAs ICs have been in development for some time, they have only been commercially available since 1984. The technology has made a transition from R & D to manufacturing, but before a new technology can be considered ready for use in demanding applications, it must have undergone a comprehensive reliability assessment. GigaBit Logic, being one of the pioneers and leaders in GaAs technology, believes that a base-line reliability assessment is essential to assure our customers that system reliability will be equal to or better than the silicon counterpart.

Note: PicoLogic™ is a trademark of GigaBit Logic, Inc.

GigaBit's reliability philosophy can be summed up as:

- GigaBit firmly believes that reliability must be "built-into" and not "tested-on" a product.

Our Quality Assurance and Reliability Program has evolved with the twin objectives of:

- Building reliability into the product.
- Demonstrating the high-performance and high-reliability of our new technology.

"Building-In" Reliability

One of the ways to ensure that reliability is "built-in" is to control the quality at each process step. In accordance with this philosophy, reliability is built-in at the design stage and throughout the process sequence. Very conservative design rules based on a worst-case, full-temperature modeling ensures reliable operation. In particular, metal line widths and spacings are defined to preclude current and field induced electromigration. Quality programs related to fab processing consist of exhaustive evaluation of GaAs semi-insulating wafers, in-process controls, statistical feedback to process steps, a significant amount of chip level testing and stringent die visual inspection, in accordance with MIL-STD-883C methods.

Reliability Test Strategy

Recognizing the fact that the technology is new, GigaBit has launched a comprehensive 3-level reliability test program to assess the process, device and product reliability levels:

1. Wafer level tests - long term storage test at 250°C, in nitrogen ambient.

2. Discrete device tests - life tests on FETs, diodes, ring oscillators, and MIS capacitors.

3. Integrated circuit life tests and activation energy experiments.

This strategy ensures that process, design and complexity related failure modes and mechanisms are revealed at an early stage and corrected. It is also used to qualify process and design changes or additions.

Reliability Test Summary

As a result of this carefully designed program to both design-in and verify device reliability, the following storage and life tests results can be reported for the PicoLogic family.

- Wafer Storage Tests

  - 50 wafers from 20 different Fab lots processed over a two-year period were subjected to up to 2000 hour storage at 250°C (N_2). The cumulative device hours have exceeded over 4 million hours.

  - 32 Process Control Monitor (PCM) test patterns on each wafer were tested at 24, 96, 168, 336, 504, 840, 1000 and 2000 hours.

  - Key parameters such as V_P, I_{DSS}, G_M and K value of the FET, V_F, V_{BR} and Ideality of the diode, ohmic contact resistance and backgating characteristics showed a variation of $\leq \pm 5\%$.

- Discrete Device Life Tests

  - Extended life tests on 32 FETS for over 7,500 hours at T_J = 150°C showed excellent parametric stability at all test points.

- Integrated Circuit Life Tests

  - Life tests in the form of static burn-in at T_J = 150°C on 20 different SSI/MSI level ICs were conducted from 1500 to 8500 hours.

  - Cumulative device hours logged to date is 4 million hours.

  - Life time calculations show that a failure rate better than 25 FITS can be achieved at T_J = 100°C.
    (1 FIT = Failure in 10^9 hours)

For more detailed reliability data by product, please refer to Chapter IX, Reliability Results.

The reliability test results presented in this report show that our GaAs IC family has an inherently high level of reliability. GigaBit Logic is committed to continuously improving the reliability level of our products, by "building-in" reliability.

CHAPTER II

TECHNOLOGY DESCRIPTION

GaAs vs. Silicon Performance

Gallium Arsenide has been endowed by nature with fundamental physical and electrical characteristics that make it an ideal material for ultra-high speed ICs. Table 1 compares these properties with silicon, and also indicates the advantages of GaAs over silicon. [1]

The electron mobility of GaAs transistor channels is much higher than in correspondingly doped silicon device channels, and these mobilities are realized at lower applied electric fields. Because GaAs is a semi-insulating material (not semi-conducting) the parasitic capacitances (which force silicon IC manufacturers to junction or oxide isolate their transistors to avoid a loss of speed) are greatly reduced.

Table 1

Comparison of GaAs and Silicon ICs

Material	GaAs	Silicon	GaAs Advantage
• N - Channel Electron Mobility	4000-5000 cm^2/V-S	800-1,000 cm^2/V-S	5 to 6 X Greater Mobility
• Electric Field at Peak Electron Velocity	7KV/cm	30KV/cm	Potential for Lower Power Dissipation
• Saturated Electron Velocity	2.2 X 10^7cm/s(Peak)	6.5 X 10^6cm/s	Faster Switching
• Wafer Resistivity (Max)	$10^9\Omega$ - cm	10^5 - $10^6\Omega$ - cm	Semi - Insulating Substrate
• Energy Bandgap	1.4eV	1.1eV	Potential for Higher Temp. Operation, High Reliability and Greater Radiation Tolerance
Process	**GaAs**	**Silicon**	**GaAs Advantage**
• Device Structures	Schottky Barrier	MOS & Bipolar	No Surface Effects
• Lithography (Mask Dimensions)	0.8 µm Gate Length	1.25 µm Gate Length	Higher Density
• Metallization	Au, Ti, Pt based	Al and Polysilicon based	Freedom from Electro - Migration
Performance	**GaAs (PicoLogic)**	**Bipolar (100K ECL)**	**GaAs Advantage**
• Speed - Power Product	0.9pJ	5pJ	High Speed - Low Power
• Gain - Bandwidth Product	10 - 15 GHz	5GHz	Higher Clock Rates
• Clock or Data Rates	1 - 3 GHz (Max.)	150 - 600 MHz (Max.)	Improved Performance
• Output Rise & Fall Times	150 - 250 ps (Max.)	1ns (Max.)	Improved Performance
• Gate Propagation Delay	75 - 150 ps (Max.)	300 - 500 ps (Max.)	Improved Performance

A special mention needs to be made regarding the saturation of drift velocity as a function of the electric field. The electron velocity versus the electric field dependence for GaAs is non-monotonic with a peak velocity of 2.2 X 10^7 cm/S at approximately 3KV/cm. Because of this velocity overshoot, GaAs devices switch faster than they would if the velocity rose monotonically to the saturation limit of 1.1 X 10^7 cm/S. This is especially true for GaAs devices with small gate lengths. In comparison, silicon has a monotonic rise of drift velocity versus the electric field and saturates at 6.5 X 10^6 cm/S.

Reliability Advantages of GaAs

The lower electric field of GaAs at peak electron velocity results in lower power dissipation for the same speed and function compared to silicon. From a reliability viewpoint, this results in fewer thermally activated failures and field-induced electromigration. Dielectric failures due to high electric fields are also greatly minimized. Another significant reliability advantage of GaAs over silicon comes from the higher energy bandgap (1.4eV). This enables higher temperature operation and greater radiation tolerance. The semi-insulating substrate also contributes to reliability, due to its freedom from parasitic leakage paths and consequent circuit failures.

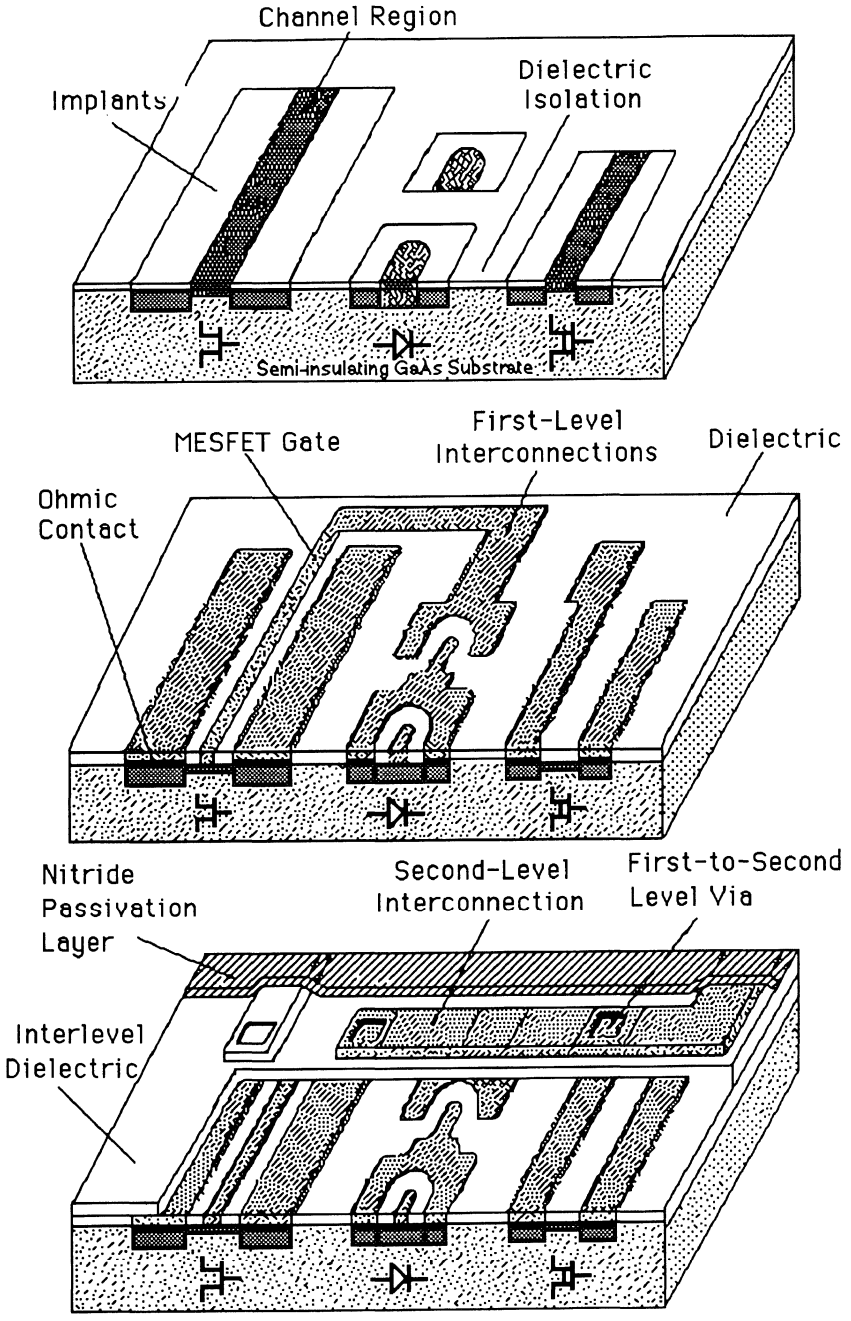
The Metal-Semiconductor Field-Effect Transistor (MESFET) technology employed by GigaBit has distinctive characteristics which enhance reliability. The MESFET is a bulk current conduction, majority carrier device structure. The semi-insulating substrate prohibits charge collection and thus provides superlative radiation tolerance. In addition, the absence of gate oxide (non-MOS) prevents the occurrence of threshold shift effects. The majority carrier devices are more reliable since life time degradation is not a problem. This results in a device structure that is generally free from surface charge effects and failures due to ionic contamination. A gold based metal system with titanium and platinum diffusion barriers provides a high degree of freedom from current and field-induced electromigration. Gold germanium ohmic contacts have been used in GaAs microwave devices for years with proven reliability. Planar cross-overs and filled vias ensure that the isolation between the first and second level metal, as well as the contacts, are highly reliable. The via-fill feature is unique to the PicoLogic family. [2,3]

Process Summary [4]

Figure 1 shows the cross-section of a typical PicoLogic device. The starting material is an undoped 3" GaAs wafer grown using the Liquid Encapsulated Czochralski (LEC) process. Although the dislocation density is higher at this stage compared to silicon, there is no evidence at this point to indicate that dislocations result in yield loss, performance or reliability degradation in our 1 micron D-MESFET structures.

Planar circuits are fabricated by multiple, selectively masked ion implants on a semi-insulation substrate. Individual devices are optimized by using separate implants, while unimplanted GaAs substrate regions provide isolation between devices. Direct step on wafer (DSW) projection photolithography (10X reduction) is used to delineate circuit patterns. Pattern replication is accomplished with dry processing techniques. Planar cross-overs and filled vias between the 2-level metal system provide the electrical circuit interconnections. A passivation layer, deposited by a low temperature Plasma Enhanced Chemical Vapor Deposition (PECVD) technique provides scratch resistance for the completed wafer.

Figure 1. **Cross-Section of a Typical PicoLogic D-MESFET**



Planar ion-implanted D-MESFET fabrication steps showing multiple, localized ion-implanted layers, gates, Schottky barriers, first- and second-level interconnect metallization and nitride scratch protection layer.

CHAPTER III

QUALITY ASSURANCE PROGRAM

GigaBit firmly believes that reliability must be "built-in" and not "tested-on" a product. This is achieved by carrying out the manufacturing process in a clean, controlled environment according to a set of well-defined process specifications, and using state-of-the-art equipment. Incoming materials are closely evaluated to guarantee a higher standard of quality. GigaBit's quality control program includes strict in-process controls and monitors to ensure that the quality criteria is met at each step of the process flow.

GigBit's quality control program is comprised of the following:

- Document Control
- Environmental Monitoring
- Machine Preventive Maintenance and Calibration
- Incoming Material Inspection
- In-process Controls & QA Gates
- Out Going Visual Inspection & Parametric Testing

Document Control

The manufacturing sequence is documented in well defined process specification manuals covering functional areas of material preparation, thin films, lithography, replication, analytical measurements, assembly, packaging, testing and burn-in. This is complemented by specifications covering clean room procedures, wafer handling, safety and vendor materials quality. The quality control organization periodically reviews and audits the process specifications. A well defined ECN (Engineering Change Notice) procedure is used to control any necessary change to the process.

Environmental Monitoring

To build a reliable die, GigaBit begins with a clean, well controlled fabrication area. This is one of the primary concerns of reliability standardization programs and is incorporated in the MIL-M-38510 line certification specifications. Because of the small size of the topographical pattern on the die, the presence of a few particles of dust or other contaminant can cause early failure or parametric degradation. At GigaBit, wafer fabrication is carried out in Class 10 clean rooms as per Federal Standard 209B. This degree of cleanliness is a requirement of state-of-the-art VLSI fabs. Particle counts, temperature, humidity and air velocity are monitored by the quality control organization periodically and corrective action is taken to maintain the environment at Class 10. Particulates, including bacteria count, are monitored periodically in the De-ionized (DI) water system, which is maintained to yield a resistivity greater than 15 M ohms. The assembly process is carried out on Class 100 laminar flow work stations. Electrostatic field is also measured in the Fab Assembly and Test areas periodically.

Machine Preventive Maintenance and Calibration

Wafer fab uses state-of-the-art process equipment known to yield high performance, reliable devices in the silicon VLSI industry. Examples include the 200KV ion-implanter, DC/RF magnetron sputtering equipment, E-beam evaporators, Plasma Enhanced CVD systems, 10X direct-step on wafer (DSW) projection aligners and dry plasma etcher and ion milling equipment. Process equipment is maintained according to a preventive maintenance (PM) schedule. In addition, process equipment and analytical measurement equipment are periodically calibrated against standards. Similar procedures are also followed in the assembly and test areas.

Incoming Materials Inspection

Even the best equipment and rigorous controls can not yield high quality products, if the materials used do not conform to the required quality standards. While mask plates, photoresist, chemicals, dopants, precious metals and packages are procured and inspected to existing silicon industry standards, special mention must be made of GigaBit's GaAs wafer evaluation program, which is discussed in greater detail in Chapter IV, Wafer Fabrication.

In-Process Controls and QA Gates

All through the process sequence, from the raw wafer to the tested IC, there are three distinct quality related activities that continuously occur: Equipment monitoring, Process monitoring and Inspection. Equipment monitoring involves the measurement of machine conditions (pressure, temperature, time, gas flow, etc.). Process monitoring involves the measurement of specific process results (thickness, refractive index, depositon rate, etch rate, etc.) to ensure compliance with the specifications. Inspection involves making analytical measurements and optical examinations against a set of QC criteria.

A QC gate is an inspection point in the process flow where the lot is screened and any components (wafers, dies, etc.) not meeting the QC standards are removed from the manufacturing flow. This is a very significant concept aimed at "building-in" reliability and has been used by military/aerospace component manufacturers for over two decades. Details of the in-process controls and QA gates for the wafer fab and packaging areas are given in chapters IV & V.

Outgoing Visual and Electrical Inspection

Wafers coming out of wafer fab and packaged ICs coming out of the assembly area, are required to meet a rigorous visual and electrical criteria that is stipulated by QC. Visual criteria are based on MIL-STD-883C methods. GigaBit's standard products (PicoLogic and Nanoram family) are tested for DC functional/parametric and AC parameters to guard-banded limits designed to guarantee the datasheet specifications. Foundry wafers are electrically tested on Process Control Monitor (PCM) patterns to customers specifications. ASIC products are also subjected to rigorous DC & AC electrical tests to guarantee the customer's specifications. Details on this inspection are given in Chapters IV, V, & VI.

Chapter IV

WAFER FABRICATION

GaAs Wafer Evaluation

Undoped 3" wafers, grown by the Liquid Encapsulated Czochralski (LEC) process, are procured from several qualified vendors.

Figure 2 shows a flow chart of the material evaluation program. Sample wafers are sent by the vendor from both ends (seed and tail) of each ingot. These samples are inspected for surface quality, capped with a thin layer of sputtered silicon nitride ($Si_3 N_4$) and processed just like regular production wafers. The FET parameters (V_p, K, G_m etc.) , C-V profile, substrate isolation and back gating are measured. The ingot passes qualification only if the samples meet our exacting requirements.

When received, wafers (approximately 80-90) from qualified ingots are subjected to visual (1X, 50X) and Surfscan 4000 inspection as shown in the figure. GigaBit has a leadership role in improving GaAs wafer quality and has a continuous interaction with vendors on quality issues.

Key Process Steps

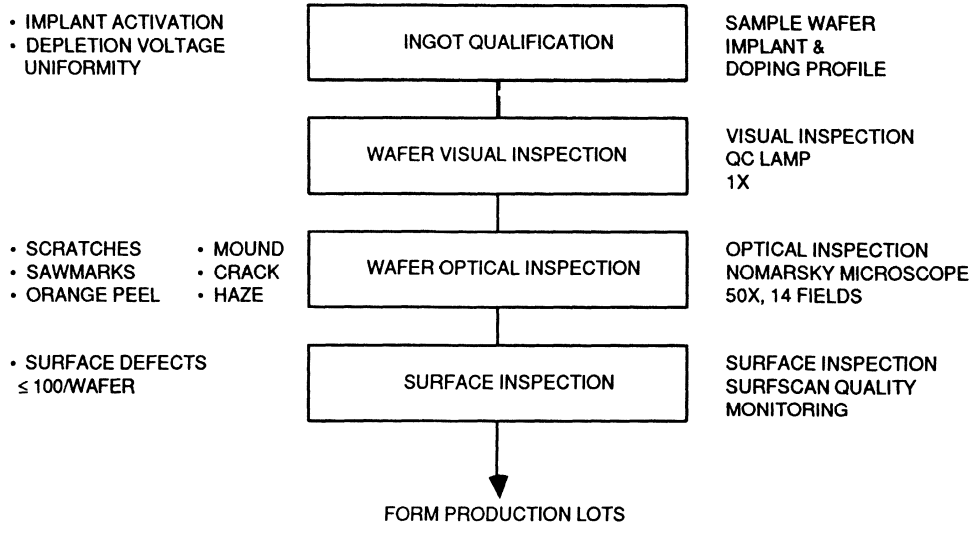
Capping Layer - The first step in the process is the coating of the GaAs substrate with a thin layer of high quality, sputtered silicon nitride (Si_3N_4). This layer prevents the dissociation of GaAs during the later high temperature implant activation annealing process.

Channel Implant - The active layer for a D-FET is created by selectively implanting Si^+ ions through the cap nitride layer using photo resist as the implant mask.

FIGURE 2

MATERIAL EVALUATION FLOW CHART

(GALLIUM ARSENIDE WAFERS)



Source-Drain Implant - A heavily doped N^+ layer is created for the source, drain and diode regions. Surface concentration is kept high to reduce the contact resistance of the ohmic metal contact to the N^+ layer in the latter steps.

Anneal - At this stage the implanted wafers are thermally annealed to both remove the implant damage and to activate the dopant species. GigaBit employs a proprietary Rapid Thermal Anneal (RTA) process.

Ohmic Contact Metallization - Ohmic contact is formed over the the N^+ layers by using Au/Ge-Ni layers deposited by E-Beam evaporation. A lift-off technique is used to define the metal regions. Au/Ge is alloyed to the N^+ layer.

Proton Isolation - Protons (H^+) are implanted between the devices to reduce back-gating.

Schottky Metallization - Schottky barriers for the diodes, gate metallization and first level metal for interconnection are achieved in a single critical step using Ti-Pt-Au layers deposited by E-Beam evaporation and replicated by a dielectric enhanced lift-off.

Interlevel Dielectric - A dense, pin hole free, high quality silicon oxide layer is deposited by a Plasma-Enhanced Chemical Vapor Deposition (PECVD) technique which ensures reliable isolation between the first and second level metal layers.

Second Level Metallization - Second level metal is magnetron sputtered using Ti-Au of sufficient thickness to give low sheet resistance and freedom from electromigration. Ion milling is used to replicate this layer. Vias between first and second level metal are filled, ensuring extremely reliable contact between the two layers. Contact measurements carried out in a total of 24 million vias from 55 wafers have demonstrated that our via fill process is high yielding and reliable at LSI levels of integration.

Third Level Metallization - GigaBit's advanced processes offer third level metallization as an option. Whenever third level metal is used, the second level metal is E-beam evaporated and replicated by a dielectric enhanced lift-off. The third level is magnetron sputtered Ti - Au and is replicated by ion-milling.

Passivation - A passivation layer is deposited by a low temperature, Plasma Enhanced CVD technique. This layer provides handling protection (scratch resistance) for the wafer and individual devices. It has specifically been designed to be a contamination and moisture barrier. The passivation layer is photo masked and plasma etched over the bond pads to expose the metallization. An over etch ensures that no residual glass is left on the pads.

Lithography - There are only 6 critical mask steps which results in fewer lithography related defects. This improves circuit yield and reliability. 10X DSW projection photo lithography with positive resist is used on all steps.

Replication - Dielectrics are replicated with plasma etching, a dry process known for its enhanced reliability in the silicon VLSI industry.

The process of defining the first level metalization is accomplished by delineating photoresist patterns, plasma etching the underlying dielectric, evaporating the appropriate metal, followed by the photoresist lift-off step. This enhanced lift-off results in planar, precisely aligned metal structures with high yields.

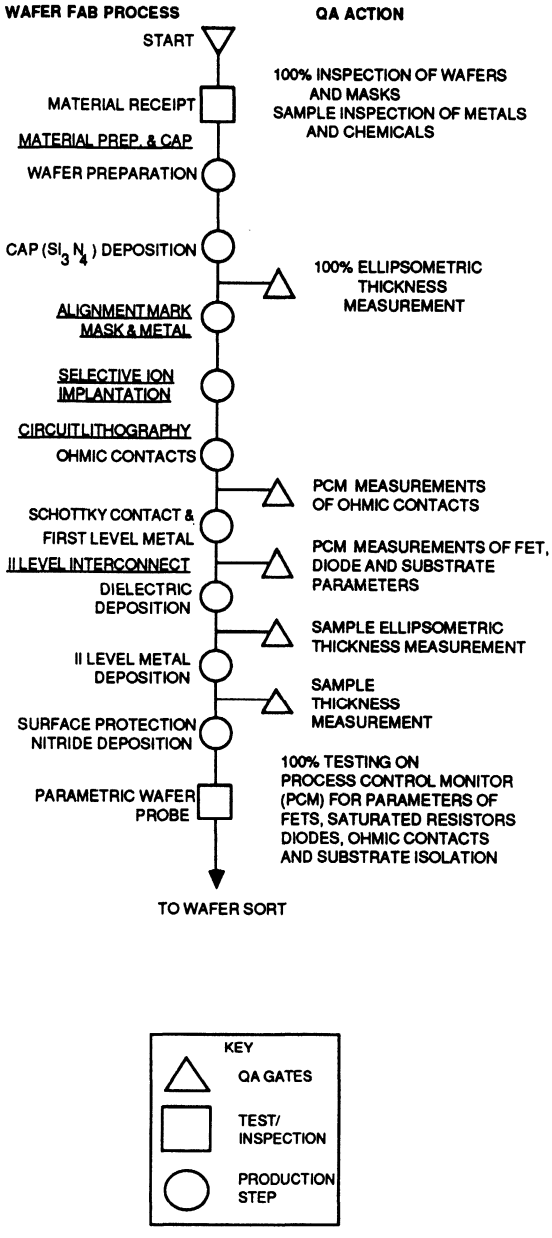
Planar Process - The dielectrics used in this planar technology serve to protect the GaAs surface and are also an integral part of the high-yielding enhanced lift-off process. After the first level contacts and interconnects are fabricated, another planar surface is formed as a result of choosing the thickness of the dielectrics and metals to be similar. This approach results in a smooth planar surface greatly facilitating highly reliable multilayer interconnect structures. In addition, to make connections between the first and second level metals, via windows are etched into the interlevel dielectric and filled with metal (equal in thickness to the interlevel dielectric). This via-fill process results in highly reliable interconnection between the first and second level metal. A similar process is used to connect the second and third level metal.

In-Process Monitors & QA Gates

Figure 3 shows a flow chart of the wafer fab process, inspection steps and the quality control gates. At each process step there are three quality related activities: Equipment monitoring, Process Monitoring and Inspection. Table 2 shows the equipment monitors and process attributes for some of the key process steps. Visual inspection is carried out using a Nomarsky phase contrast microscope with high magnification (400X & above). At each process step critical attributes are measured and plotted in the Mean Range (X-R) format. The Statistical Process Control (SPC) technique is used to define the upper and lower control limits (UCL and LCL), for each process monitor.

Process steps where a QA gate is shown in the flow chart, are points where the lot is screened partially or fully. Wafers not meeting the quality

FIGURE 3
WAFER FAB PROCESS FLOW CHART
(For a 2 Level Metal Process)



requirements at that point are removed from the manufacturing flow.

Parametric Testing

Wafer parametric testing is done on Process Control Monitor (PCM) test patterns on the wafer at three stages in the fab process: ohmic, Schottky metallization and final test.

PCM data provides the critical link between the device design/modeling and the fabrication process. This data is also used to grade the outgoing wafer quality and thus serves as a measure of the fab's performance. Extensive parametric testing and statistical analysis is a special feature of GigaBit's process quality efforts. This is of great interest to our Foundry customers, for whom the end product is the wafer itself.

PCM patterns are arranged as a set of 2X11 probe pads in special regions between each field (a group of die on the wafer). The number of patterns on each wafer is dependent on the size of the reticle frame and ranges from 42 to 52 patterns. Figure 4 shows the DC and AC PCM patterns used in standard product wafers.

An explanation of the patterns, parameters and method of measurement is given in Appendix II. It can readily be seen that DC parametric testing covers the FET, Schottky diode, ohmic contact, implanted layer and isolation. AC testing is done on an 11 stage ring oscillator, in the form of interconnected NOR gates. A sample of the parameters tested and typical values are given in Table 3.

Parametric testing is done on a Testar 4000 controlled by an IBM PC. This (industry standard precision) tester is known for its accuracy and repeatability.

An ohmic stage test is done after the implants and ohmic contacts have been processed, to ensure that the correct implant sheet resistance and ohmic contact resistance have been achieved. Wafers not meeting the specification are rejected at this stage.

The Schottky stage test is more elaborate. Basic FET and diode parameters such as V_P, I_{DSS}, G_m, K, V_F, V_{BR}, are measured at this stage. This test is also used as a gate to reject materials not likely to meet the parametric specifications at final PCM test, based on GigaBit's statistically correlated data.

Prior to final parametric testing, all wafers are subjected to a stabilization bake at 250°C under parameters and reveals abnormal ohmic contact and

Table 2
Equipment Monitors and Process Attributes

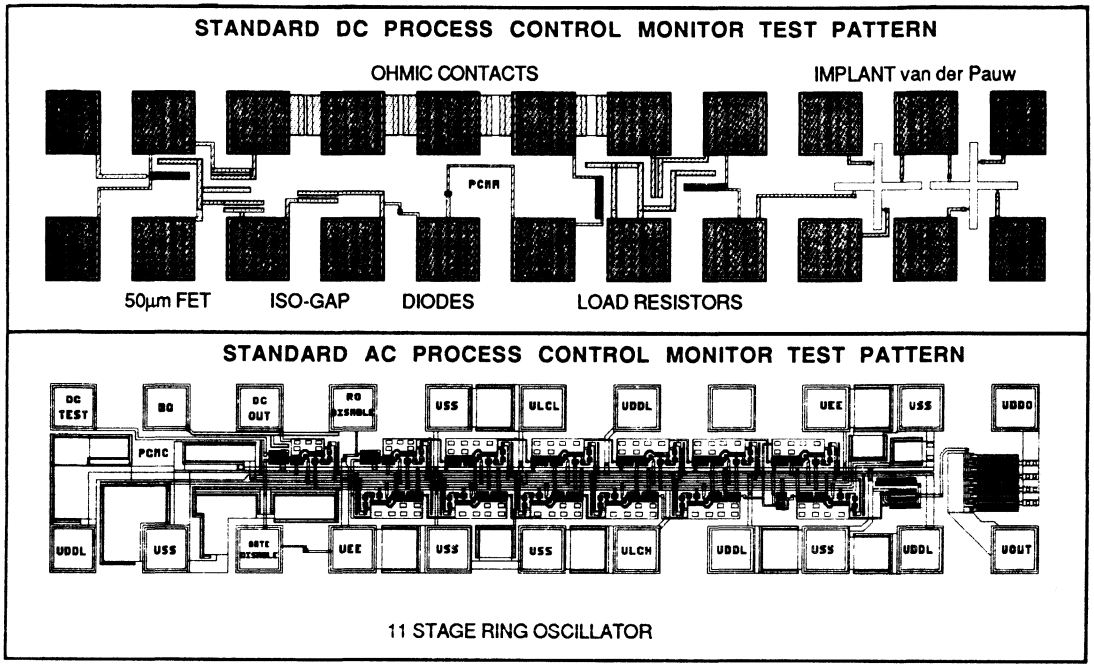
Process Step	Equipment Monitor	Process Attribute
Si_3N_4 Cap	Pressure Temperature	Thickness Refractive Index
Ion Implant	Energy Dose	C-V Profile (Depletion Voltage, Depth)
Masking	Contrast Exposure Spinner Speed	Critical Dimensions Overlay Accuracy Resist Thickness Visual Defects Repeated Mask Defects SEM Analysis of feature size
Replication (Plasma & Ion Mill)	RF Power Pressure Temperature	Etch Rate Visual Quality
Thin Films (Metals & Dielectrics)	Temperature Gas Flow	Thickness Refractive Index Etch Rate Stress Composition Visual Quality

Table 3
Sample of PCM Parameters Tested and Typical Values For D-MESFET Process

Pattern	Symbol	Parameter	Typical Value	Unit
FET (50μm)	V_P	Pinch-Off Voltage	-1.0	V
	I_{DSS}	Drain-Source Current	3.7	mA
	K_e	K_e Value (external)	105	$\mu A/V^2\mu m$
	G_m	Transconductance	155	mS/mm
	R_{ON}	On Resistance	140	ohms
Schottky Diode	N	Ideality	<1.2	-
	V_F	Forward Voltage	0.77	V
	V_{BR}	Reverse Breakdown Voltage	>6	V
TLM	R_C	Contact Resistance	0.25	ohm-mm
	R_{S+}	N^+ Sheet Resistance	400	ohms/sq.
Ring Oscillator	$(T_D)_{RO}$	Gate Delay	<100	ps

FIGURE 4

PCM Patterns



back-gating problems, if any, in the wafer.

The final parametric testing is very comprehensive and includes tests for isolation, backgating, diode ideality, etc. In addition, an 11 stage ring oscillator pattern is tested to ensure that the discrete devices (FETS & Diodes) forming the oscillator support operation at the minimum design frequency. Parametric specifications are controlled by QC and are periodically revised in order to improve circuit performance and yield.

Each parameter (such as V_P, G_m. . .) is statistically analyzed over each wafer and lot for mean value, standard deviation and distribution histogram. This data is archived in hard disc and serves as an excellent indicator of the process improvement over time. It is also used to revise design rules, if needed, to improve the performance of the device.

Outgoing Visual Inspection

Wafers meeting the PCM specifications are visually inspected for attributes such as second level metal quality, lift-off quality, dielectric appearance, particulates, scratches, alignment, etc. A Nomarsky phase contrast microscope is used at 50X and 200X for this inspection. While Method 2010.7 of MIL-STD-883C [7] is used as a general guideline, it is our experience that the visual criteria for GaAs wafers have to be different from those for silicon (bipolar and MOS). GigaBit has an ongoing program to correlate visual defects with critical die failures, as revealed by a wafer map from electrical testing.

CHAPTER V

PACKAGING

A major factor contributing to the reliability of an IC is the package it is housed in. The package provides support to the die and enables it to meet various environmental stresses such as vibration, acceleration, thermal shock, and temperature cycling. It also provides the electrical interface to the outside world.

PicoLogic Packages

GigaBit assembles GaAs ICs in three primary package types (See Figure 5).

a. 0.400" square 36 lead flat pack (FP)
b. 0.400" square 36 lead, cavity-up ceramic leadless chip carrier (LCC)
c. 0.480" square 40 lead, cavity-down leadless or C-lead chip carrier

NOTE: Cavity-up and cavity-down refers to package configurations where the die is attached to the package bottom and top surfaces respectively. A high performance 68 I/O package is available for ASIC products.

These packages are standard 40 mil pitch JEDEC equivalent packages. Electrically, they provide a matched 50Ω transmission line environment (between the die and the PCB) and can support 3GHz operation and 100ps rise and fall time signals. All three packages are gold plated to provide corrosion free reliable contacts under high humidity environments. All of these packages are suitable for mounting on PCBs using standard Surface Mount Technology (SMT) soldering techniques.

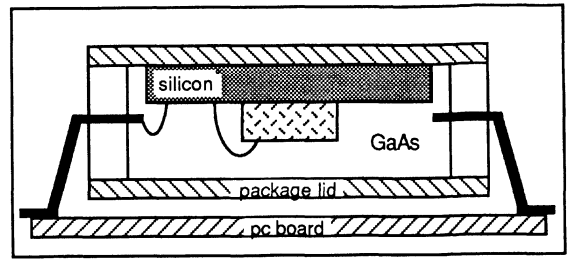
High Speed Considerations

When using ultra fast GaAs ICs, the package design is crucial to achieve the performance that is inherent to GaAs. For example, take the situation where a GaAs chip operates at a 100ps gate delay. The package must have very short delays (<100ps) in order to guarantee the highest performance at the system level. Noise and cross-talk are paramount packaging concerns. The package must minimize cross-talk and power supply noise caused by very fast rise and fall times (typically 150ps). Another important packaging consideration is ringing. To minimize ringing and Voltage Standing Wave Ratio (VSWR) the package loading of transmission lines must be kept to a minimum. Thus, running at ultra high speeds (3GHz clock rates) puts many stringent requirements on chip packaging. [5]

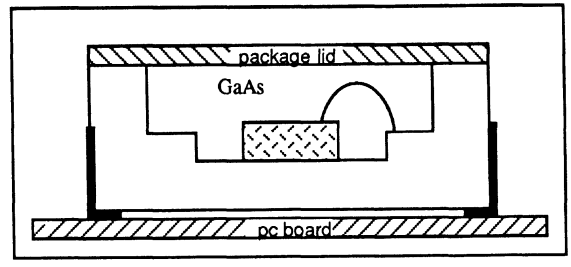
FIGURE 5

PicoLogic Packages

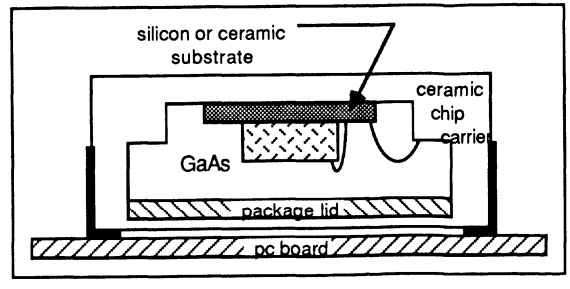
36 LEAD FLATPACK



36 I/O CERAMIC LCC



40 I/O CERAMIC LEADLESS OR LEADED CHIP CARRI



GigaBit packages are designed to reduce delay, loading, cross-talk and power supply noise. They also provide an internal ground plane for shielding and internal by-passing capacitors to reduce power supply noise. The chip carriers are based on a multilayer ceramic technology or on a GigaBit proprietary silicon chip carrier technology. In one, the GaAs die is attached to the ceramic chip carrier, which has tungsten-filled thermal vias from the die-attach cavity to the package bottom. In the second, the GaAs die is mounted on a silicon substrate which in turn is mounted on the LCC. Because of its low thermal resistivity relative to both ceramic and GaAs, the silicon acts as a heat spreader. The two LCCs have roughly equivalent thermal characteristics--that is, the effect of the silicon is roughly equivalent to that of the thermal vias. Die attach is currently performed with a thermally conductive silver-filled epoxy; known for its die-shear strength, stability and low out-gassing.

Thermal Issues

From a reliability viewpoint, the most important package consideration is the thermal resistance of the package. The thermal resistance of the IC from die surface to ambient determines the operating die temperature under a specified power dissipation, and the long-term reliability under actual use.

Thermal management of GaAs ICs is necessary in order to ensure long term system reliability and performance. The objective is to keep the individual transistor junction temperatures as low as possible across the IC to ensure optimum reliability. With this in mind, GigaBit recommends that the junction temperatures of commercial products be maintained at or below 125°C so that MTBF's of several million hours can be realized. Junction temperatures lower than this will result in longer life times while higher temperatures may reduce the life expectancy..

The thermal characteristics of GaAs ICs are similar to those of silicon bipolar ECL ICs. The thermal conductivity of GaAs is low (approximately 1/3 to 1/5 that of silicon). The board level packing density of GaAs ICs will be typically higher to preserve the shortest propagation delays. Despite these differences, the thermal management techniques required for GaAs ICs are very similar to those required for surface mount silicon bipolar devices.

Junction temperatures of GaAs ICs can be related to device power dissipation by the following approximate relationship:

$$T_J = T_A + 10°C + (\theta_{SC} + \theta_{CA})P_D$$

where T_J =Maximum junction temperature (°C)
T_A=Maximum ambient temperature (°C)
P_D=Maximum device power dissipation (W)
θ_{SC}=Die surface to case thermal resistance (°C/W)
θ_{CA}=Case to ambient thermal resistance (°C/W)

θ_{SC} is determined largely by the package design whereas θ_{CA} is dominated by system level considerations such as device spacing, board spacing and cooling air flow rate.

THE USE OF HEATSINKING IS STRONGLY RECOMMENDED FOR PICOLOGIC ICS THAT DISSIPATE MORE THAN 1 WATT.

The die surface to case thermal resistance varies among the three package options shown in Figure 5, due to differences in construction. Please refer to GigaBit Application Note 3, "Thermal Management of PicoLogic and NanoRam GaAs Digital IC Families" [6], for a more detailed description of the thermal resistance components and thermal management techniques.

In general, most PicoLogic ICs will require heat sinking and forced air in high density system environments. In many cases, a small heatsink and 600 lfpm air flow will be sufficient. In low density prototyping environments, a heatsink alone may be adequate.

Assembly Process

Assembly of the GaAs die and silicon substrate is carried out on class 100 laminar flow work stations. A flow chart of the test and assembly process is shown in Figure 6. It can be readily seen that the assembly methods - saw, die-attach, wire bond and lid seal - are identical to those of multi-lead silicon LSI packages. In fact, identical equipment is used to carry out the process steps. However, due to the high fragility of the GaAs wafer and die, special techniques are used to prevent breakage and microcracks on the die.

In particular, the wafer sawing and gold wire thermosonic ball bonding are optimized to ensure that no microcracks are induced in the die during these steps. A 1 mil gold wire is bonded from the GaAs die to the package by thermosonic ball bonding techniques, yielding a high bond strength. All packages are hermetically sealed using industry standart Au-Sn solder sealing.

The QC gates in the assembly process assure the die and wire bond strength and visual quality of the lot. A periodic sample bond-pull test is done by QC to insure the bonding integrity. Also, a 100% optical inspection is carried out in accordance with MIL-STD-883C Method 2010.7 [7].

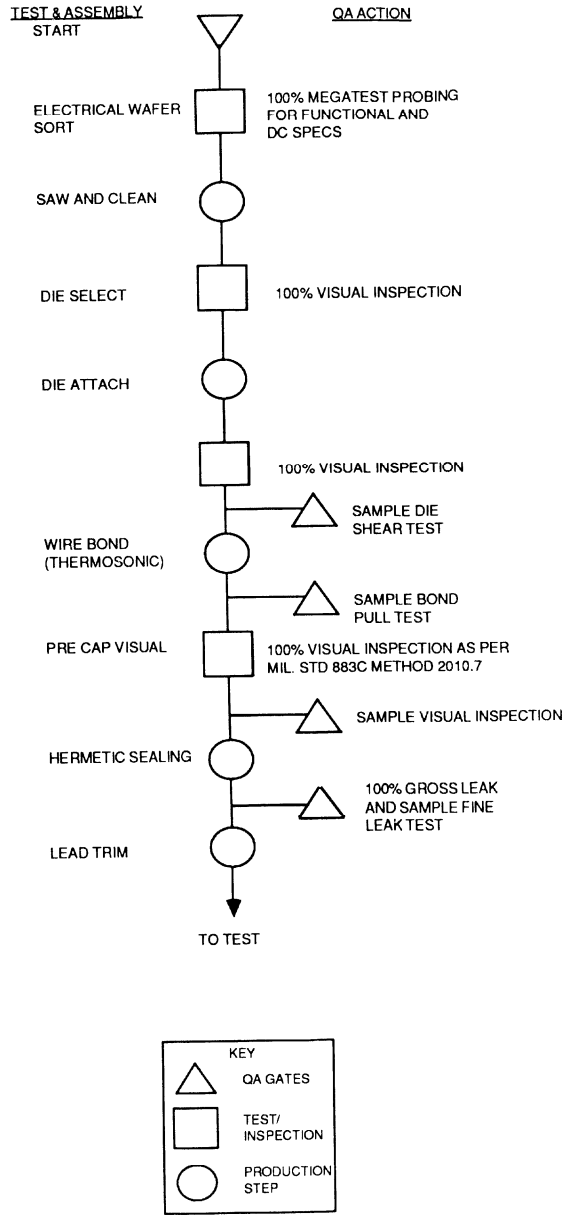
ESD protection is ensured during assembly operation by controlling the humidity of the area and also by the use of anti-static tops on work benches. Wrist straps are worn by all operators in the assembly and test areas.

Package Reliability

PicoLogic ICs have been subjected to life tests in the form of static burn-in, totaling greater than 4 million device hours. No package or assembly related failures have been observed to date. Environmental screens - thermal shock, temperature cycling and acceleration - have been conducted on different package types and have shown the packages to be reliable. A program is ongoing to qualify selected PicoLogic ICs to Class-B requirements of MIL-STD-883C.

FIGURE 6

Wafer Sort & Assembly - Flow Chart



CHAPTER VI

TESTING

GigaBit's electrical testing and screening goal is to meet the guaranteed datasheet specifications to tight DPM limits. At the same time, the test plan is designed to analyze the variation in parameters on a statistical basis, and feed back the data to design and process engineering. This helps us achieve our targeted levels of quality and reliability. Testing activity can be divided into wafer sort and packaged IC testing.

WAFER SORT

Wafers meeting the PCM spec and outgoing visual criteria are subjected to 100% DC parametric and functional testing at 1-5 MHz. A state-of-the-art wafer prober, with cassette-to-cassette loading and auto align capability, is used with a Megatest Q2/52 tester. Presently, wafer level testing is done to the same parametric limits as the packaged IC. Rejected die are inked for ease of identification and removal during die sort after sawing.

PACKAGED IC TESTING

Figure 7 gives the flow chart of GigaBit's testing and screening operations.

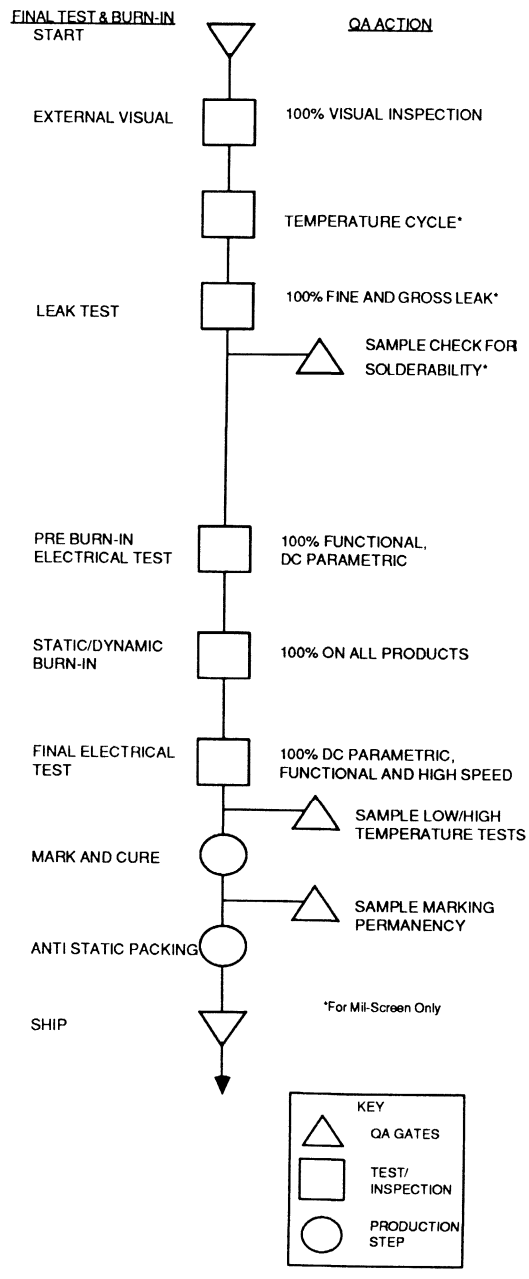
Assembled and packaged ICs are tested 100% using Megatest Q2/52 and in-house (HP computer based) high speed test equipment, in one of the most comprehensive test plans in the GaAs IC industry.

Pre Burn-in Electrical Test

Prior to the burn-in screen, ICs are tested for DC parameters and functional tests at 1-5MHz on a Megatest Q2/52 tester. Megatest Q2/52 is an industry standard digital IC tester, known for its repeatability and accuracy in volume production use. Q2/52 has an 8086-based microcomputer system controller and a PDP 11/23 host computer. Power supplies and drivers have 5mV resolution and ± 10mV (typical) accuracy. Worst case accuracy is better than ± 25mV. Kelvin measurements on all parametric lines ensure accuracy during low voltage and low current measurements. All measurement modules are calibrated weekly using Megatest diagnostic software.

FIGURE 7

Final Test & Burn-In - Flow Chart



Timing calibration is more elaborate and is done once a month with an HP counter and Megatest diagnostic program. The test system is programmed in QTL, a Megatest proprietary high level language. GigaBit has generated a range of test and engineering characterization programs for all PicoLogic ICs. Megatest host computer software provides simple and composite schmoo plotting, wafer mapping, binary/linear searching and datalog capability.

Burn-in Screen

All PicoLogic ICs are subjected to dynamic or static burn-in at 150°C junction temperature for 24, 48 or 168 hours duration, depending on the device type and its infant mortality rate history. This screen guarantees a very high degree of protection from early life failures.

A typical burn-in schematic is shown in Figure 10 of Chapter VIII. Static burn-in is done in GigaBit's in-house burn-in systems. Each product type is subjected to burn-in at different ambient temperatures (in separate ovens) depending on the average power dissipation and package outline of the product. Thus all products receive the burn-in screen at a die temperature of 150°C. REL Inc's Criteria V burn-in systems are used for the dynamic burn-in of parts at clock rates between 2-10MHz.

Post Burn-in Electrical Test

The post burn-in electrical tests are a repeat of the pre burn-in tests, aimed at weeding out the catastrophic and marginal parametric devices. At this stage, test limits are guardbanded to guarantee operation over the 0°C to 85°C temperature range and also to ensure operation over the V_{SS} and V_{EE} ranges given in the datasheet.

High Speed Test

The real challenge in testing GaAs digital ICs is posed by high speed testing at gigahertz clock rates. Since no industry standard high speed testers have been available, GigaBit has developed in-house systems that can be used reliably to test our ICs. These testers consist of an HP 8663A synthesized signal generator, Tektronix sampling oscilloscope/data acquisition unit, a data switching matrix and an ultra high speed device test fixture, interconnected to and controlled by an HP 9836 computer with 1M byte mainframe memory. Test programs are written in HP-Basic. The tester can measure rise/fall times, propagation delays, set up and hold times, as well as the maximum clock frequency of operation. DC voltages can be applied with 20mV resolution. An innovative double differentiation measurement technique allows rise times to be measured at ±30 picosecond accuracy with 5 picosecond resolution. Clock frequency is determined by a binary search, executed by software in 25 MHz increments.

These testers are also used in conjunction with a Temptronix thermostream system to make measurements from -55°C to +125°C, case temperature. V_{SS} and V_{EE} schmoo capability has also been built in. The high speed tester and device test fixtures are periodically calibrated using reference transmission lines. We consider our high speed testing efforts a significant achievement in the area of GaAs IC testing. All high speed test equipments are periodically calibrated by Honeywell to standards traceable to NBS.

Temperature Characterization

Early in the design cycle, each new product is assigned to a product engineer who follows the product through design, test plan generation and production. The product engineer develops the test strategy with the designer, assures full function testability, carries out the characterization of the part and sets appropriate testing guardbands. The product engineer also has the responsibility to obtain conditional and final reliability qualification of the product.

Each new product is characterized over the temperature range of -55°C to +125°C, using a Temptronix thermostream system in conjunction with Megatest (DC/functional) and high speed testers. A statistically significant sample from multiple production lots is taken to represent a range of Vp, Gm and other device parameters. At each temperature test point, V_{SS} and V_{EE} supplies are also varied. GigaBit's proprietary software is used to manage the vast amount of data generated during characterization. This data is used to set appropriate guardbands for room temperature testing and to assure operation within datasheet limits over the 0°C to +85°C temperature range. Each lot is tested by QC on a sample basis at temperature extremes, to verify conformance to the guaranteed specifications.

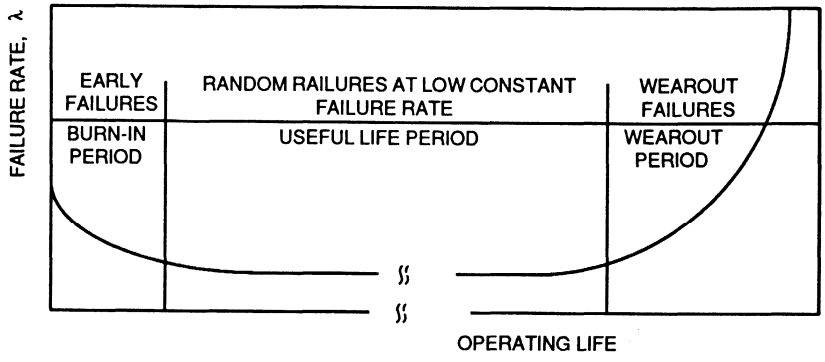
In addition to the above, an outgoing QC program ensures that all parts meet the guaranteed datasheet specifications. GigaBit also conducts elaborate reliability tests. The details of the reliability program are explained in greater detail in Chapter VIII.

CHAPTER VII

RELIABILITY THEORY

Reliability can be defined as "the probability of a device performing a specific function, under the specific conditions for which it was designed, for a specific period of time". From the user viewpoint, reliability can simply be defined as the length of trouble-free operation of the device. Over the years, the semiconductor industry has developed sophisticated screening and life test strategies based on reliability theory. The key concepts of these proven theories, screening and life test strategies have been utilized in the GaAs industry also. GigaBit's reliability goals can best be discussed with reference to the traditional reliability life (bathtub) curve as shown in Figure 8.

Figure 8
Reliability Life Curve (Bathtub)



Bathtub Curve

The reliability of a device is characterized by three phases (astonishingly similar to the life cycle of any living organism): infant mortality, random failure and wear out. When a device is manufactured, there is always a finite probability that there are certain failure mechanisms, which cause it to fail under a relatively moderate stress level. Such devices fail very early in the useful life and are aptly termed infant mortality rejects. Failures in this phase are characterized by gross defects due to poor workmanship, and can be significantly reduced through proper manufacturing controls and screening techniques. Subjecting the devices to voltage stresses, identical to the actual use condition at an elevated temperature, has proved to be an effective screen to weed out infant phase failures. All GigaBit ICs are subjected to a 100% burn-in screen for periods varying from 24 to 168 hours at a junction temperature of 150°C. depending on the maturity and complexity of the part.

The second phase of the bathtub curve is characterized by low failure rates and spans a long period of time. Only random failures, which occur occasionally, are seen in this phase. The useful life region of the device and failure rate is wholly a function of the technology per se and its maturity level on the learning curve.

The final phase is that in which the device "wears out" due to various continuous physical mechanisms such as current flow and temperature, to which the device is subjected during its useful life. It is possible to extend the period at which wear out occurs by using proper design techniques (metal layer clearances, line widths, etc.) and application considerations i.e. limiting the current, die temperature and proper thermal management.

When evaluating different technology options for system design, it is important to examine the actual bathtub curve of the device families from each technology. Key parameters such as the period of infant mortality phase, failure rate during useful life and the time of onset of wear out should be compared.

Failure Rate

During the infant mortality and random failure rate regions, the probability of not having a failure up to a specific point in time, can be expressed by the equation:

$$P_O = e^{-\lambda t}$$

where λ is the failure rate and t is time. λ varies with time during the infant mortality region, but becomes relatively constant during the random failure region. λ is the failure per unit time and is usually expressed in "percent failures per 1000 hours". Other forms of expressing reliability commonly cited are:

FIT $\rightarrow$ Failure in 10^9 hours
MTBF $\rightarrow$ Mean time between failures

It must be noted that FIT and MTBF are specified at a known temperature of operation such as 100°C. At a higher temperature the MTBF would be lower and at a lower temperature, it would be higher.

Statistical Basis

Generally failure rate predictions on a device family are made by subjecting a reasonable number of samples from the population of devices to an extended life test at accelerated test conditions. Hence the statistical concepts of the Central Limit Theorem apply and λ is calculated using the χ^2 (CHI) distribution. [8]

$$\lambda \leq \frac{\chi^2 (\alpha, 2r + 2)}{2nt}$$

where $\alpha = \frac{100 - CL}{100}$

λ = failure rate

CL = confidence limit in percent

r = number of rejects

n = number of devices

t = duration of test

Since the value of any sample of units from a large population will produce a normal distribution (according to the Central Limit Theorem), a 50% confidence limit is the mean of this distribution. A 90% confidence limit is very conservative and results in a higher λ which represents the point at which 90% of the area of the distribution is to the left of that value. (2r + 2) is called the degree of freedom and is a conversion from the random rejects obtained in the life test time period to a form that can be read from χ^2 tables. It is a normal practice in the IC industry to predict failure rates at a 60% confidence limit.

Table 4 shows a sample χ^2 (CHI) distribution table for up to 5 rejections and confidence levels from 50% to 95%.

Table 4

CHI Square Distribution

Degrees of Freedom	Confidence Level %					
	50	60	70	80	90	95
2	1.39	1.83	2.41	3.22	4.61	5.99
4	3.36	4.04	4.88	5.99	7.78	9.49
6	5.35	6.21	7.23	8.56	10.6	12.6
8	7.34	8.35	9.52	11.0	13.4	15.5
10	9.34	10.5	11.8	13.4	16.0	18.3
12	11.3	12.6	14.0	15.8	18.5	21.0

Degrees of Freedom = (2X # of rejects) +2

An example may be useful in calculating failure rate using the χ^2 table. If one reject is seen after 2000 hours, when 50 samples of an IC are subjected to a life test at T_j = 150°C, then the failure rate at a 60% confidence level may be computed from the above table as:

$$\lambda = \frac{4.04}{2X50X2000}$$

$$= 2.02\% \text{ per } 1000 \text{ hours at } 150°C$$

Accelerated Testing

Most integrated circuits have life times in the order of 1-2 million hours at normal operating temperatures. Hence, to demonstrate the life time of a product family with reasonable accuracy, either an abnormally large sample size is required or life tests over an abnormally long period (>10 years) are required. To overcome this anomaly, it is customary to use accelerated temperature testing, which is based on the Arrhenius model for reactions.

Arrhenius Equation

The Arrhenius equation is a special case of the Vant Hoff equation governing the reaction rate of physical and chemical processes. The Arrhenius equation given below, states that the reaction rate increases with temperature:

$R = Ae^{-Ea/kT}$, where

R= reaction rate

A = A constant

Ea = Activation Energy (eV)

k = Boltzmann's constant (8.63×10^{-5} eV/°K)

T = Absolute temperature (°Kelvin) at the site of the reaction

Since the failure mechanisms observed in semiconductor devices can always be related to a physical reaction (eg: electromigration), it is possible to accelerate the onset of such a failure, by conducting life tests at an elevated temperature. Assuming Ea is a constant, a plot of log R against 1/T results in a straight line with slope equal to Ea. Ea may be interpreted as the energy threshold of a particular failure mechanism. It is more convenient to plot the device life time (in-hours) against the operating die temperature (in °C), as shown in Figure 9, for various activation energies. Using this plot, failure rate data taken at one temperature can be translated to another temperature with reasonable accuracy.

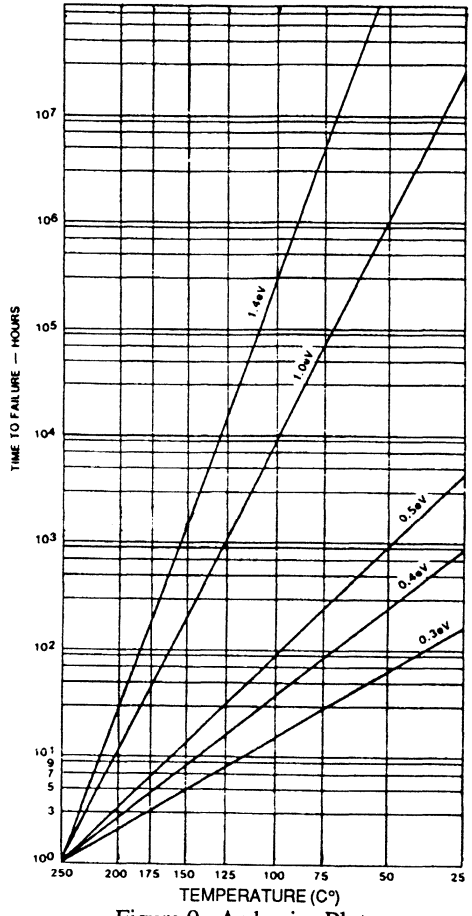


Figure 9. Arrhenius Plot

However, two important factors need to be considered when using accelerated temperature testing to predict failure rates for normal use conditions:

1. The failure modes observed in the accelerated environment must be the same as those observed under actual use conditions.

2. It should be possible with a reasonable degree of accuracy to extrapolate from the accelerated environment to the actual use conditions.

In practice, the above theory is applied in the following sequence to predict the life times of ICs:

Failure Rate Prediction

a. Conduct life tests on sample lots at multiple temperatures (e.g. 150°C, 175°C, 200°C, 225°C).

b. Plot the failure rate of identical failure modes against the reciprocal of the temperature.

c. Calculate the slope of this line to obtain the activation energy for the specific failure mechanisms.

d. Conduct life tests at a specific elevated temperature on a sample of parts, on which failure rate data is required.

e. Calculate the failure rate at elevated temperature.

f. Extrapolate the failure rate (or mean life time) at normal operating temperature using the standard chart of Figure 9, using the lowest activation energy obtained in (c.).

Example: Let us try to predict the failure rate at 100°C for the IC type which showed a failure rate of 2.02% per 1000 hours at 150°C in the earlier example. Let us assume an activation energy of 1.4eV. From the Arrhenius Plot of Figure 9, the acceleration factor between 100°C and 150°C for 1.4eV is:

$$\text{Acceleration Factor} = \frac{\text{Time to fail @ 100°C}}{\text{Time to fail @ 150°C}} = \frac{3 \times 10^5}{2 \times 10^3}$$

$$= 150$$

Since λ(150°C) is known to be 2.02% per 1000 hours, λ(100°C) is obtained be dividing λ(150°C) by the acceleration factor (150 in this case):

$$\lambda(100°C) = 2.02\%/150 \text{ per } 1000 \text{ hours}$$

$$= 0.014\%.$$

CHAPTER VIII

RELIABILITY PROGRAM

GigaBit Logic, being one of the pioneers and leaders in GaAs digital IC technology, believes that a baseline reliability assessment of the new technology is extremely important to assure our customers the highest system reliability. This is important to the user because the failure mechanisms of GaAs IC technology previous to this report, haven't been evaluated. Such failures occur under thermal and/or electrical stress, and will give the user insight into the correct application of these ICs to obviate such failures.

GigaBit has a comprehensive 3-level reliability test program to assess the process, device and product reliability levels:

1. Wafer level tests - storage tests (250°C, N_2 purge)
2. Discrete device tests - (static burn-in)
3. IC life tests - (static/dynamic burn-in) and Activation Energy Studies

This strategy ensures that process, design and complexity related failure modes and mechanisms are revealed at an early stage and corrected. A detailed description is given below:

Wafer Level Storage Tests

It is a well known fact that the reliability of semiconductor devices decrease with increasing temperature. High temperature storage tests have, therefore, been used in silicon MOS/LSI industry to reveal parametric instability, and gross process defects. As in any semiconductor technology, non-optimal process conditions, can cause degradation of devices at higher temperatures. In the case of GaAs devices, thermal stability of metal contacts (ohmic and Schottky barrier) to the GaAs material is probably the most important factor in determining the device reliability. For example degradation of Schottky barrier metals (Ti/Pt/Au) under purely thermal stress has been reported. Thus a well planned high temperature storage test can conveniently serve as a means of assessing the process reliability in general and the metallization reliability in particular.

At GigaBit, this test consists of subjecting wafers to long term high temperature storage at 250°C under nitrogen ambient. Before the start of the test, the following parameters on the PCM sites are measured on a Testar 4000 parametric tester.

FET	Pinch-Off Voltage V_P
	Drain Current I_{DSS}
	Transconductance G_m
	Proportionality Factor K
DIODE	Forward Voltage V_F
	Reverse Voltage V_{BR}
	Ideality N
	Barrier Height
GENERAL	Ohmic Contact Resistance R_C
	Isolation
	Backgating
	Implant Sheet Resistance

These parameters are measured at 42 to 52 sites on each wafer depending on the mask used. From these measurements the mean values and standard deviations (σ) are calculated. Since the ohmic contact and Schottky barrier on gallium arsenide is known to degrade under high thermal stress, wafers are subjected to long term storage tests at 250°C. PCM measurements are repeated at intermediate time points: 24, 96, 168, 336, 504, 840 and 1000 hours.

Tests conducted on sample wafers from 20 lots have shown that all of the basic GaAs device parameters are thermally stable. Based on our initial studies, process improvements were made to keep the change in ohmic contact resistance (R_C) and backgating (BG) within acceptable limits. The current PicoLogic process is seen to be thermally stable at 250°C up to 2000 hours. This is equivalent to millions of hours at normal operating temperatures. Furthermore, no indication of purely thermally activated failure mechanisms have been observed to date. For detailed data please refer to Chapter IX, Reliability Results.

Discrete Device Life Tests

To fully characterize discrete device structures and interconnects, drop-in masks are used to obtain FETS, diodes, vias, cross-overs, etc. with different dimensions representing a broad range of devices. These devices are periodically characterized over the temperature range of -55°C to +125°C and a large statistical data base has been collected which allows us to accurately model the basic structures.

These drop-in devices, which are wire-bondable, are packaged and subjected to long term life tests in the form of static bias at Tj = 150°C. Tests conducted on FETS and ring oscillators have shown that the basic device structures are inherently reliable. Our plan includes life tests on MIS capacitors, cross-overs and vias. For results of these tests, please refer to Chapter IX, Reliability Results.

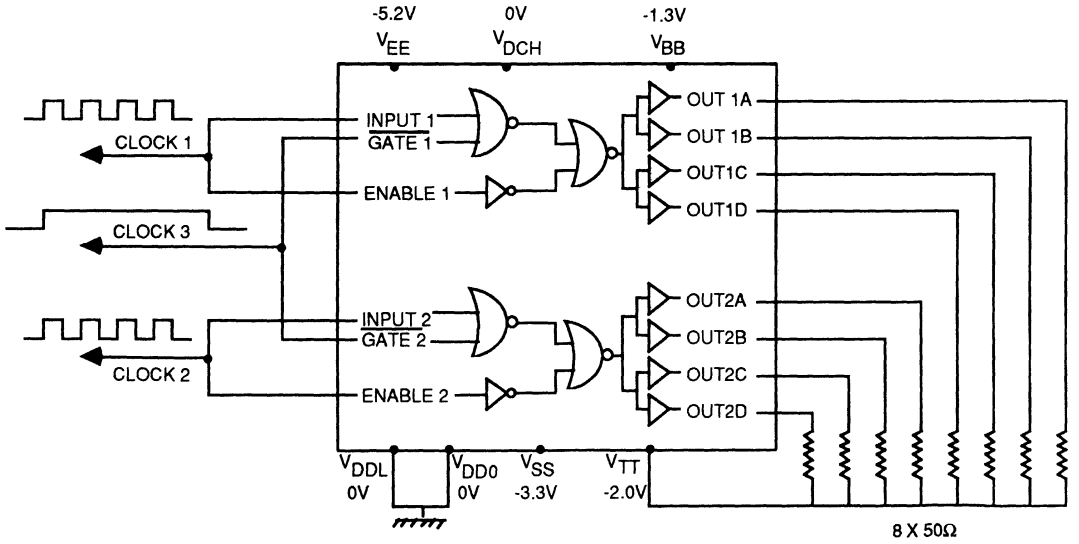
IC Life Tests

Static life tests are standard and consist of forward biasing a maximum number of diodes and transistors in the IC to ensure maximum possible power dissipation. The life test is conducted with a junction temperature of 150°C. DC, functional and high speed tests are carried out on life test samples at zero hour and intermediate time points at 24, 96, 168, 336, 504, 840, 1000, 1500, 2000, 2500... hours. Due to the inherently high activation energy of gallium arsenide devices, it has been found that 1000 hours at T_j = 150°C is not sufficient at normal sample sizes to determine the life time with any reasonable accuracy. On the other hand, if too high a temperature is used in the life test, it may lead to package related failure modes, which are not germane to GaAs ICs. With this in mind, GigaBit has implemented a long duration life test program (≥ 2500 hours life test on PicoLogic parts at T_j = 150°C).

In addition to static life test studies, GigaBit has conducted life tests based on dynamic switching at 2-10 MHz clock rates on 10G065 (7 stage Ripple Counter), 10G012B (Dual Comparator/Complementary Driver) and 10G021A. A typical dynamic/static circuit used for life test and burn-in screening is shown in Figure 10. Life tests have been completed on all current PicoLogic products including Diode and FET arrays and the 1K RAM. Results indicate the inherent high reliability (MTBF ≥ 20 million hours at T_j = 100°C) of PicoLogic GaAs digital ICs using the D-MESFET process. Details are given in Chapter IX, Reliability Results.

Figure 10

Dynamic/Static Burn-In Schematic For 10G011A Fanout Buffer



NOTE: 1. Frequency of Clock1 and Clock2 is 5 MHz(Approx.)
2. Clock3 is at least 1/10 slower than Clock1 and Clock2.
3. For Static Burn-in, Clock1 & Clock2 leads are applied -0.8V and Clock3 lead is applied -1.8V.

Activation Energy Experiments

Most failure mechanisms have a time/temperature relationship, which is reflected in the activation energy of the Arrhenius Model. Failure mechanisms having a lower activation energy, are manifested as electrical failures at earlier time points in the life of the device and can thus limit the useful life of a product. Furthermore, activation energy is used to translate the life time expectation from the higher die-temperature of the life test to actual use conditions.

GigaBit's reliability program includes activation energy experiments in the form of accelerated life tests at T_j = 175°C, 200°C and 225°C. Initial tests used 10G021A as the test vehicle. Currently tests are veing conducted on 10G022 (Shift Register). Results are given in Chapter IX, Reliability Results.

Qualification Procedure

GigaBit's reliability program includes a "Qual Plan" for approving a new process, package or design before the product is released to customers. Key elements of the Qual Plan are

- Process Qual
- Package Qual
- Product Qual

The reliability organization administers a process qual screen prior to making a process change, additon or mask layer revision on a permanent basis. The screen consists of parametric evaluation on two lots over a 500 hour 250°C storage and/or 1000 hour life test at T_j = 150°C. In the same manner, a new package or variant is subjected to a package qual screen derived from MIL-STD-883C method 5005[7]. This screen ensures that the new package can withstand the electrical, mechanical and environmental stress the product is likely to encounter in actual usage.

All new products are qualified for customer release based on a preliminary, conditional and final qual administered by the reliability organization in the form of extended life tests on multiple lots. In parallel with this, Product Engineering carries out extensive characterization on samples from different fab lots. This consists of electrical tests (DC, functional and high speed) over supply voltage extremes and temperature extremes (-55°C, -20°C, 0°C, 25°C, 85°C, 100°C, 125°C).

Periodic Process Reliability Monitors

While long term life tests on typical PicoLogic parts establish the base line reliability of the technology, continuous reliability monitoring of the Fab Process is also necessary to insure that the parts shipped indeed meet the high levels of reliability expected of them. An innovative periodic monitor life test scheme has been introduced. Every other week, sample devices from new Fab lots are assembled and taken up for a 1000 hour life test. DC/Functional test is done at the start and at 168, 336, 504, 840 and 1000 hours. High speed test is conducted at the start and at 1000 hours. If the cumulative rejects exceed the LTPD criteria, the Fab lot from which the samples came from is put on hold, until an analysis as to the cause of failures is done. This scheme is found to be a very effective "real-time" monitor of the process reliability of new Fab lots. Results to date are given in Chapter IX, Reliability Results.

Failure Analysis

Evaluation of life test rejects and feedback to process and design engineering groups is an integral part of GigaBit's reliability program. In addition to electrical testing (DC, functional and high speed) and exhaustive microprobing, Nomarsky phase-contrast microscope (up to 1000x) and Scanning Electron Microscope (SEM) analysis are regularly done on all rejects. An outside analytical laboratory is used when Auger Electron Spectroscopy (AES), Secondary Ion Mass Spectroscopy (SIMS) and Laser Microprobe Mass Analysis (LAMMA) are required to identify the physics of process-related failure mechanisms.

ESD Sensitivity Analysis

Damage to PicoLogic devices can result from inadequate protection from electrostatic discharge (ESD). ESD is known to be a common cause of device failures at all stages of device and equipment manufacture. While MOS structures appear to be the most susceptible to ESD damage, all technologies seem to be ESD sensitive to varying degrees as shown below:

Technology	ESD Sensitive Voltage Range
Bipolar Transistors	380 - 7000V
CMOS	250 - 3000V
ECL	500 - 3000V
GaAs FET	100 - 300V
JFET	140 - 7000V
MOSFET	100 - 200V
Schottky TTL	1000 - 2500V

Damage from ESD can cause either complete device failure by parametric shifts, or device weakness by locally heating, melting or otherwise damaging oxides, junctions or other device components. ESD related failures are more likely to occur during the infant mortality region of the bathtub curve. ESD may also initiate a device weakness or fault that degrades and causes failure with time. In fact, the process of burn-in, which is meant to weed out early failures, increases ESD related failures due to additional handling. Devices are also more sensitive to ESD at higher temperatures.

Extensive studies during the Fab process at GigaBit has shown that the presence of excessive Electrostatic Fields (ESF) can cause degradation of Schottky barrier diodes. This study resulted in upgrading of Fab equipment to reduce ESF. ESF and humidity are monitored at all work stations in the Fab periodically.

GigaBit has implemented an industry standard anti-static environment throughout device assembly, testing and burn-in areas. Each of these areas use anti-static floor mats and table tops and operators wear grounded wrist straps in humidity controlled work areas. In addition, devices are shipped in anti-static containers, surrounded by conductive foam.

GigaBit's reliability program includes ESD evaluation on a periodic basis. Each month samples from production lots are tested for ESD sensitivity on all pins. This test conforms to the human body model recommended in MIL-STD-883C method 3015.2. [7] A summary of results based on the NOR and FOB gates are given below:

- Inputs - all pins 100 - 400V
- Clamps - all pins 300 - 2200V
- Supplies - all pins >1000V

It should be kept in mind that susceptibility to ESD damage at a lower voltage is generic to all ultra fast devices, including GaAs ICs. This is mainly due to the small feature sizes (gate length = 1μm) and low input capacitance. PicoLogic devices use a saturated resistor (gateless FET) in series with each input. This limits the input current to 15mA. In addition, once the part is installed in a circuit, the clamp diodes with their low on resistance and super fast switching speed (600 GHz) provide ESD protection to some extent.

However, the user is requested to take adequate ESD precautions during storage, assembly and testing. Please follow the precautions against ESD damage given in Appendix I, Recommendations for Operation and Handling.

Environmental Tests

Screening of parts for military applications, includes a variety of environmental and mechanical tests, in addition to the electrical tests (at temperature extremes) and the life test. Details of these tests are enshrined in the Group B, C and D test flows of Mil-Std-883C, Method 5004. [7]. Typical environmental tests consist of Temperature Cycling, and Thermal Shock. Mechanical tests are aimed at establishing the package and die-mount/wire bond integrity. Such tests are generally Fine and Gross Leak, Vibration, Acceleration and Bond Strength.

GigaBit has initiated MIL-STD-883C Class-B level tests on typical products in 4 different package types. A preliminary chart, giving the sample size and severity of the proposed Class-B flow is given in Chapter IX.

Radiation Resistance

GaAs integrated circuits are inherently much more radiation resistant than even hardened silicon integrated circuit technologies. The principal reason for GaAs devices' excellent total dose hardness is that there is no oxide or insulator between the gate and channel (as in Si MOSFETs) to charge up in the presence of ionizing radiation, with consequent gross threshold shifts. Even with 100 Mrad total gamma doses, GaAs D-MESFET pinchoff voltage shifts of less than +50 mV have been measured, many orders of magnitude better than Si MOS. Further, because it is extremely difficult to obtain surface inversion (surface channel formation) at GaAs-insulator interfaces, problems with "field oxide" charging causing inter-device isolation failures after exposure to ionizing radiation are not observed in GaAs ICs.

GaAs ICs are usually also very resistant to dose rate-induced upset. The principal reasons for this transient dose rate (γ) hardness are the short minority carrier lifetimes (few ns) and diffusion lengths (few μm), and the fact that the semi-insulating substrate tends to reduce the effective photocurrent charge collection depth. GaAs ICs with excellent resistance to single event upset (SEU) have also been demonstrated. It is

important to point out that both the transient dose rate and SEU hardness levels of GaAs ICs are strongly influenced by circuit design factors and the device selections for their implementation (such as the choice of MIS versus reverse-biased Schottky diode capacitor types, etc.).

Based on the physical characteristics of GaAs and measured results for GaAs ICs, GigaBit Logic ICs should be, with proper design, radiation hard to the following levels:

Total Dose (γ): $>10^7$ Rads (10^8 typical)
Neutron Fluence: $> 10^{14}$ Rads
Transient Dose Rate (γ) (upset): 10^8 Rads/s (10^9 typical)
Transient Dose Rate (γ) (survival): 10^{11} Rads/s

Note: Transient dose rate (γ) (upset) is the maximium ionizing radiation dose rate that can be sustained in normal circuit operation without temporary disruption of circuit function or stored data (ie., the state of flip flops or memory cells). This hardness level is a function of the radiation pulse width, as well as circuit design and implemantation factors.

The 1K RAMs (12G014) are currently undergoing radiation tests through a Government-funded program. Results of radiation hardness will be made available in future reliability updates.

RELIABILITY RESULTS

Wafer Level Storage Tests

More than 50 product wafers sampled from 20 different Fab lots fabricated over a two year period were subjected to high temperature storage tests in nitrogen ambient up to 2000 hours. The goal was to assess the process stability under thermal stress and to find out whether there are any failure mechanisms activated by thermal stress. PCM sites were tested at the intermediate time points of 2, 4, 8, 24, 96, 168, 336, 504, 840, 1000 and 2000 hours.

Summary Results

Test	Sample Size	PCM Sites Tested	Cumulative PCM Site Hours	Reliability Rejects	Para-metric Stability
250°C Storage In Nitrogen Ambient	50 Wafers (From 20 Lots)	800	4.0 Million	0	$< \pm 5\%$

Parametric Stability

Key FET parameters such as Pinch-Of Voltage (V_P), Saturated Drain Current (I_{DSS}) and Transconductance (G_M) showed excellent parametric stability up t 1000 hours. Typical variation in V_P, I_{DSS} and G_M are shown in Figures 11, 12, & 13 respectively. While interpreting these curves, it should be kept in mind that, in accordance with the Arrhenius model for activation, a time period between 100-280 hours at 250°C is equivalent to 2 million hours of useful life at 100°C (an activation energy of 1 to 1.2eV is assumed). Hence the variations in parameters beyond 280 hours will not adversely affect the performance of the IC during its useful life.

FIGURE 11

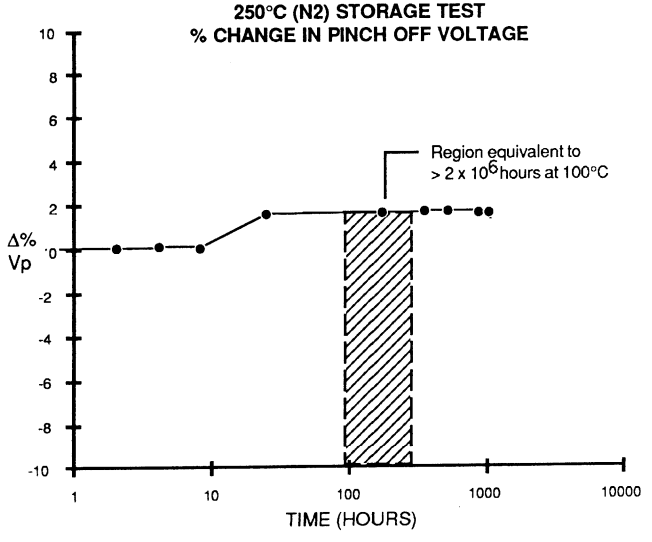


Figure 12

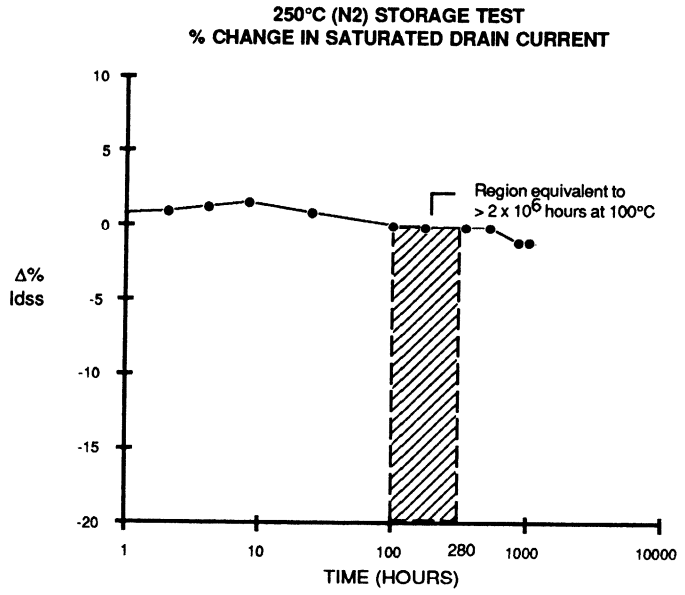
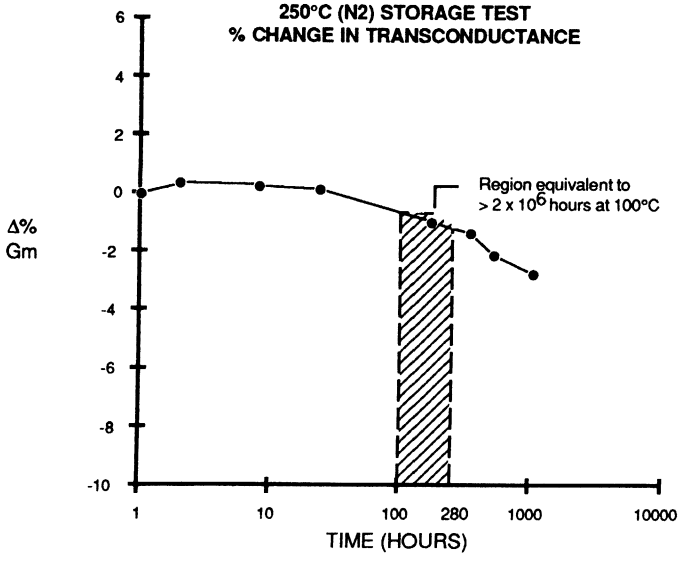


Figure 13



Degradation Mechanisms

No major degradation mechanisms were observed in FET and diode parameters up to 2000 hours. The ohmic contact resistance increases up to 20% but remains well within the spec. limit.

Ohmic contact resistance was measured using the Transmission Line Method (TLM). The TLM pattern consisted of a series of resistors (N^- and N^+ implants) all having a 50μm width, but different lengths.

Special Device Structures

In addition to the generic D-MESFET and diode device structures used in standard GaAs ICs; cermet resistors and MIS capacitors are also available for circuit design, through additional process steps. High resistivity (~0.5 MΩ/square) cermet resistors serve as load resistors in low power 1K SRAM cells. Stability of the resistor value is a key measure of its reliability. Thermal stress tests were carried out on ten 1K RAM wafers up to 504 hours at 200°C. The resistor values (nominally 130K ohm and 1.85M ohm) were measured on test patterns at zero hour and also at 24, 72, 168, 336, and 504 hours. Less than 2% change was observed in the resistor values insuring reliable SRAM cell operation.

High capacitance per unit area (0.8 fF/micron^2) capacitors are fabricated using an ultra thin 400 A Si_3N_4 layer sandwiched between a highly doped n-type region and metal electrode. Capacitor value and leakage current stability under thermal stress, serve as excellent indicators of dielectric integrity and freedom from pin holes. Storage tests were done on ten wafers at 250°C for 504 hours to evaluate the MIS capacitor stability. Results show that the capacitance and leakage current of the MIS capacitor vary by less than ±10%.

Discrete Device Life Tests

FETS with a 50μm gate width and a 0.8μm gate length were fabricated with GigaBit's standard process flow using the FATFET structure of the PE-006 drop-in mask. 32 FETS were assembled in 16 LCC packages as per the GigaBit assembly flow. They were subjected to static life tests at T_j = 150°C. FETS were biased so as to draw I_{DSS} ≈3mA.

Summary Results

Reliability of PE-006 FET:

Test	Sample	Test Duration (Hours)	Cumulative Device Hours	Reliability Rejects	Failure Reasons
T_j =150°C V_{DS}=5V I_{DSS}=3mA	32	7500	0.23 million	3*	Gate-Drain Shorts

*Electrical testing indicated a gate-drain short. Visual examination after de-lidding showed possible migration of metal as the cause for the short in the channel region. Please refer to the Analysis of FET Rejects section for details.

Parametric Stability

Pinch-Off Voltage (V_P), Saturated Drain Current (I_{DSS}), Transconductance (G_M), On-Resistance (R_{ON}), and Source Resistance (R_S) were measured on all of the FETS at zero hours and at 168, 336, 504, 840 and 1000 hours and every 500 hours thereafter up to 7500 hours. All of the FET parameters remained stable to within ±10% of the initial value. Our SPICE simulations have confirmed that this order of variation will not adversely affect the performance of PicoLogic ICs. Typical parametric variations are shown in Figures 14, 15, and 16.

FIGURE 14

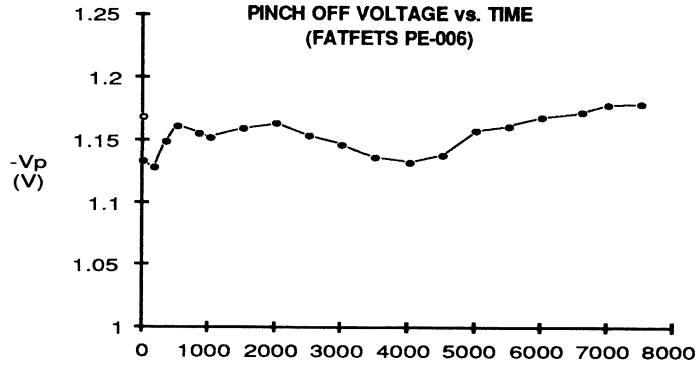


FIGURE 15

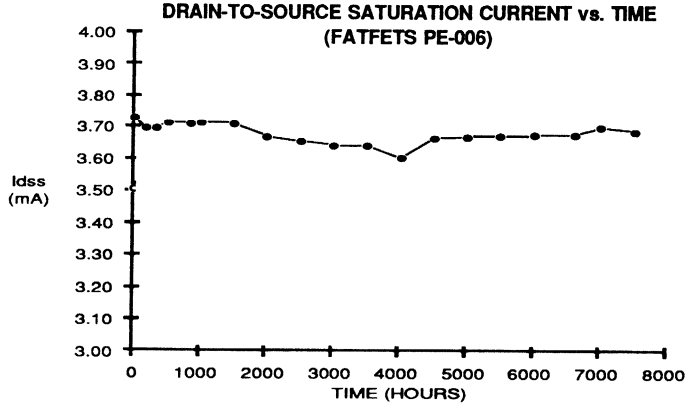
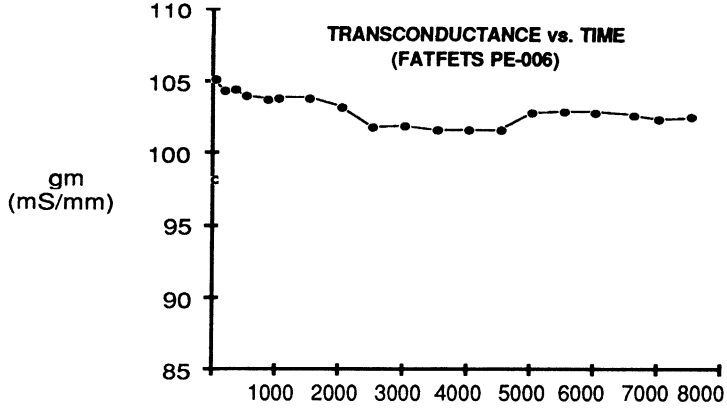


FIGURE 16



Analysis of FET Rejects

The FETS that showed gate-drain shorts beyond 3000 hours were failure analyzed. Nomarsky optical examination at 200X showed movement of metal between the gate and drain. Detailed DPA (Destructive Physical Analysis) was done in an anlaytical laboratory to confirm the source of the mobile metal. X-ray Photoelectron Analysis (XPS) was initially done to ensure that there were no unusual contaminants on the surface of the FETS. Laser microprobe mass analysis (LAMMA) was carried out to examine the composition of the deeper layers. The laser was used to pyrolize material from the sample which was then passed through a time of flight spectrometer for mass analysis. Titanium was found to be the mobile metal and since the activation energy for metal migration is normally very high for titanium, it was concluded that the isolated case of mobile metal was due to the presence of stray contaminants on the GaAs surface. This has been confirmed by repeated tests on similar FETS at elevated temperature (175°C) for 2000 hours. Life tests on PicoLogic parts have shown no indication of mobile metals.

PICOLOGIC IC LIFE TESTS

Infant Mortality Evaluation

One of the key indicators of the infant mortality region of the bathtub curve is the post burn-in yield. A high yield shows that only random failures due to inherent material flaws or workmanship are being screened out. On the other hand, a poor yield, is indicative of serious wafer fab or assembly process deficiencies. In such a case, burn-in may not be an effective screen, since fall-out during early life (at the customer's site) cannot be ruled out. Another indicator worth noting is the failure rate during early life (an additional 168 hours) after the infant region failures have been removed. This certifies the effectiveness of the burn-in screen being used.
Based on burn-in statistics compiled over the last 4 years (June, 1984 through March 1988), PicoLogic ICs have shown the following values:

- Post Burn-In Yield: 98% (average)
- Early Life Failure Rate: 0.05%

Post burn-in yield meets the percent defective allowable (PDA) requirement of MIL-STD-883C, Method 5004.6 for Class B devices. The early life failure rate is comparable to the value obtained for silicon LSI components.

Life Test Results

Results of the PicoLogic life tests are presented in the following sections:

(I) Life Test Criteria
(II) Cumulative Device Hours Summary
(III) Analysis of Life Test Data

Life Test Criteria

Based on GigaBit's experience, we believe that the best way to measure GaAs IC reliability is with the following life test conditions, test criteria and statistical distribution:

1. The temperature of testing is specified as the "junction temperature" (T_j) during life tests. The ambient condition (oven temperature) is adjusted for each product to achieve a T_j of 150°C.

2. The biasing configuration is such as to dissipate the maximum rated power for the IC. Clamp diodes are in the default condition, i.e. reverse bias. All outputs are terminated to V_{TT} (nominal -2.0V) through 50 ohm resistors. Single stage circuits are biased to place the output in a logic 1 state. Life test circuits for static and dynamic stress are shown in Figure 10.

3. The reject criteria at intermediate time points or at end of life tests is one or more of the following failures:

   - Catastrophic (opens, shorts)
   - Non-functional
   - Outside datasheet spec limits
   - Parametric degradation >±20% of zero hour values

4. Failure rate and FITS (failures in 10^9 hours) are calculated at T_j = 100°C. χ^2 distribution at a 60% confidence level is used for calculations.

5. An activation energy of 1.4eV is assumed for the main population failures. GigaBit's activation energy experiments confirm this value.

6. Based on our early life tests on PicoLogic parts, it was found that the GaAs digital ICs require a longer duration of life tests (in the order of 2000-5000 hours) to induce sizable failures. This is due to the inherently high activation energy of GaAs devices. Hence life test predictions are generally based on lots which have undergone>2000 hours life test.

Cumulative Device Hours Summary

In order to assess the reliability of the PicoLogic family, samples of different parts from numerous production lots were subjected to long term life tests. Life test at T_j = 150°C was used to accelerate the failures. Specific products were subjected to life tests at multiple temperatures to assess the activation energy of various failure mechanisms.

Table 5 is a summary of the life tests conducted on PicoLogic parts.

Table 5

Summary of Life Tests on PicoLogic & NanoRam Parts

Product	Sample Size	Life Test Hours	Cumulative Device Hours
Design Verification[1]			
FOB 10G011 2 Stage Ripple Counter 10G060	134	1500	134,892
Static Life Test			
NOR 10G000	70	8500	520,000
NOR 10G000A	54	3000	143,352
FOB 10G011A	42	2500	101,332
PDFF 10G021A	145	6000	823,360
DCCD 10G012B	81	5000	333,168
Diode Array 16G010	21	1500	28,692
VMD 10G070	17	2000	29,516
MUX 10G040 & DMUX 10G041	172	5000	609,084
Dynamic Life Test			
Divide-By-128 10G065	49	6500	298,920
New PicoLogic Parts (10G002, 10G022, 10G061)	135	4000	494,360
Process Rel Monitors	192	1000	192,000
1K RAM 12G014	45	6500	291,342
Total @ T_j = 150°C	1157	-	4.0 Million

Note: 1. Life test results during the design verification phase were used to improve the device structures of input level shifting diodes and clamp diodes.

Analysis of Life Tests

Life test results on PicoLogic and NanoRam parts based on 4.0 million device hours indicate that a failure rate of 20 to 50 FITS can be achieved at Tj = 100°C on SSI, MSI and LSI level parts. Parts with larger production history show failure rates < 20 FITS, consistently, in our recent life test. The tables given below present a more detailed picture of the life test performed on different product groups of PicoLogic and NanoRam family:

PicoLogic Gates

Life Test Results

Product	Package	Sample Size	Life Test Hours	Rejects	Failure Mode
NOR 10G000A	LCC	54	3000	0	-
FOB 10G011A	LCC	42	2500	0	-
NOR 10G000	LCC	70	8500	6	1. Diode-Capacitor Shorts 2. Input Diode Shorts
XOR 10G002	LCC	45	4000	0	-

Failure Rate Predictions

Product	Device Hrs. $T_j = 150°C$	Equivalent HRS @ $T_j = 100°C$	REL Rejects	Failure Rate 1000 Hrs.	FITS
10G000A	143,352	38.1 Million	0	0.0024%	24
10G011A	101,332	26.9 Million	0	0.0034%	34
10G000	520,000	138.1 Million	6	0.0048%	48
10G002	138,018	35.3 Million	0	0.0026%	26

Note: Failure rate and FITS are calculated at $T_j = 100°C$ for an upper confidence level of 60% using χ^2 distribution, and activation energy of 1.4 eV.

PicoLogic Flip Flop, Comparator and Register

Life Test Results

Product	Package	Sample Size	Life Test Hours	Rejects	Failure Mode
PDFF 10G021A	LCC/FP	145	6000	1	Output Driver
DCCD 10G012B	LCC/FP	45	5000	1	Diode Capacitor Short
SR 10G022	LCC	45	4000	0	-

Failure Rate Predictions

Product	Device Hrs. $T_j = 150°C$	Equivalent HRS @ $T_j = 100°C$	REL Rejects	Failure Rate 1000 Hrs.	FITS
10G021A	823,360	210.8 Million	1	0.001%	10
10G012B	333,168	85.3 Million	1	0.0024%	24
10G022	180,000	46.1 Million	0	0.0019%	19

Note: Failure rate and FITS are calculated at $T_j = 100°C$ for an upper confidence level of 60% using χ^2 distribution and activation energy of 1.4 eV.

PicoLogic Counters

Life Test Results (Dynamic)

Product	Package	Sample Size	Life Test Hours	Rejects	Failure Mode
VariableMod. Divider-10G070	FP	17	2,000	2	Interstage source follower
7 Stage Ripple Counter-10G065	LCC/FP	49	6,500	1	Random
4 bit synchronous counter-10G061	LCC	45	4,000	0	-

Failure Rate Prediction

Product	Device Hrs. $T_j = 150°C$	Equivalent HRS @ $T_j = 100°C$	REL Rejects	Failure Rate 1000 Hrs.	FITS
10G070	29,516	7.6 Million	2	-	-
10G065	298,920	76.5 Million	1	0.0026	26
10G061	176,342	45.1 Million	0	0.002	20

Note: 1. Failure rate and FITS are calculated at $T_j = 100°C$ for an upper confidence level of 60% using χ^2 distribution and activation energy of 1.4 eV.

2. In view of the small sample sizes and low device hours, failure rate calculation on 10G070 is not statistically relevant. Data shown for reference only.

MUX/DEMUX

Life Test Results

Product	Package	Sample Size	Cumulative Device Hours	Rejects
MUX 10G040/ DEMUX 10G041	FP/LCC	172	609,084	2 + 2
Failure Mode: 1. Input current to $\phi 1$ increses beyond spec. 2. Frameshift funct. failure. 3. D-cap. failures.				

Failure Rate Prediction

Product	Device Hrs. $T_j = 150°C$	Equivalent HRS @ $T_j = 100°C$	REL Rejects	Failure Rate 1000 Hrs.	FITS
MUX/ DEMUX Family	609,084	155.9 Million	4	0.0037%	37

Note: 1. Failure rate and FITS are calculated at $T_j = 100°C$ for an upper confidence level of 60% using χ^2 distribution and activation energy of 1.4 eV.

256 X 4 SRAM

Life Test Results

Product	Package	Sample Size	Lifetest Hours	Rejects	Failure Mode
256X4 SRAM	LCC	45	6500	1	Random

Failure Rate Prediction

Product	Device Hrs. Tj = 150°C	Equivalent HRS. @ Tj = 100°C	REL Rejects	Failure Rate 1000 HRS.	FITS
12G014	291,342	74.6 Million	1	0.0027%	27

Activation Energy Results

To determine the activation energy, precision D-Flip Flop (10G021A was used as the test vehicle. Twenty eight samples (each from the same fab lot), were subjected to static bias lifetest at three junction temperatures: 175°C, 200°C and 225°C. Lifetest data on 145 parts at Tj = 150°C was also used to fit the curve. The results are given below:

Junction Temperature	Sample Size	Median Life
225°C	28	4,240 Hours
200°C	28	13,862 Hours
175°C	28	124,758 Hours
150°C	145	823,360 Hours

Arrhenius plot resulting from the above data is given in Fig. 17.

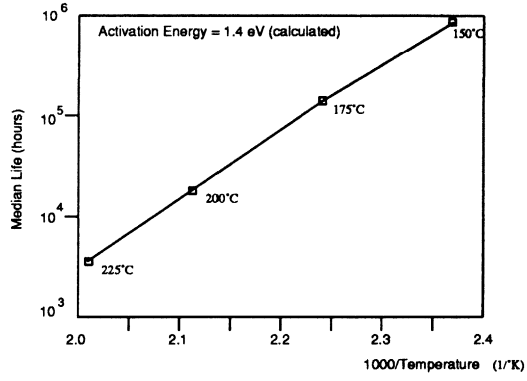


Figure 17

Arrhenius plot of the GigaBit 10G021A Precision D-Type Flip-Flop

It can be seen that the activation energy as calculated from the curve-fit data works out to 1.4 eV. It can be seen that the time taken to achieve 50% sample failures at 175°C and 200°C is relatively long. A strategy of working out median life at each of these temperatures was resorted to. This is due to the high activation energy, which is not normally experienced in silicon ICs.

Activation energy experiment is currently being repeated on 10G022 (shift register).

Periodic Process Reliability Monitor Results

The table below gives the results to date on the process reliability monitor life test. Fab lots are accepted on a LTPD of 15, which is equivalent to A/R of 0/1 for the sample sizes shown.

TEST #	SAMPLE WW	PART #	PACKAGE	FAB LOT	SAMPLE SIZE	REJECT @ 1,000 HRS.
PQ-1	38	10G061	40 LCC	L17C-703F	18	0
PQ-2	40	10G003	40 LCC	L2110F-1	15	0
PQ-3	42	10G041A	40 CLD	M23-716F	15	0
PQ-4	44	10G004	40 LCC	L19-723K	15	0
PQ-5	46	10G012B	36 FP	L18-705H	20	0
PQ-6	48	12G014	40 LCC	R6-728G	15	0
PQ-7	50	10G021A	36 LCC	L11-641G	14	0
PQ-8	2	10G061	40 LCC	L17C-736F	18	0
PQ-9	4	10G012B	40 LCC	L18-735L	15	0
PQ-10	6	10G010	40 CLD	L20C-732F	15	0
PQ-11	8	10G011B	40 LCC	L20C-734F	15	0
PQ-12	10	10G021A	40 LCC	L11-805L	15	0
PQ-13	12	10G022	40 LCC	L25-730F	15	0

Note: FAB Lot number indicates the year and work week. Eg: 703 is 1987, WW3.

Production Burn-in Yield

One of the reliability indicators in a manufacturing environment, which is perhaps least recognized, is the burn-in yield. Burn-in is normally used to weed our infant mortality failures in ICs. A high yield, (>95%) after burn-in, shows that only random failures due to inherent material flaws or poor workmanship are being screened out. On the other hand, a low yield (<75%) is indicative of serious wafer fab, test or assembly deficiencies. In such a case, burn-in may not be an effective screen, since additional failure during early life (at customer's site) is possible. Another indicator worth noting is the failure rate during early life (168-336 hours) after the infant region failures have been removed. GigaBit Logic subjects all ICs to a production burn-in screen at Tj = 150°C for periods varying from 24 to 168 hours depending on the maturity and complexity of the part. Based on the burn-in statistics compiled over the last three years on approximately 100,000 parts, GaAs ICs have shown the following figures:

- Post Burn-in Yield 98%
- Early Life Failure Rate 0.05%

The burn-in yield meets the percent defective allowable (PDA) requirement of MIL-STD-883C Method 5004.6 for Class B devices. The early life failure rate is comparable to the value obtained for silicon LSI components. It is also interesting to observe the post burn-in yield improvement over the years as a new product crosses the learning curve and attains full production status. Figure 18 below shows the yield vs. time curve for a family of GaAs ICs. It is our experience that all new products start off with 80-85% yield and reach a 95% or greater average yield, after the design and test issues are resolved. On GigaBit's most mature products, burn-in yields of 98% are typically experienced.

MIL-STD-883C Screens

PicoLogic packages are currently being evaluated to MIL-STD-883C, Class B levels of screening to establish base line reliability levels. When completed, selected PicoLogic parts will be made available to customers with Class-B screening. The proposed Class-B screening is given on page 39 for reference.

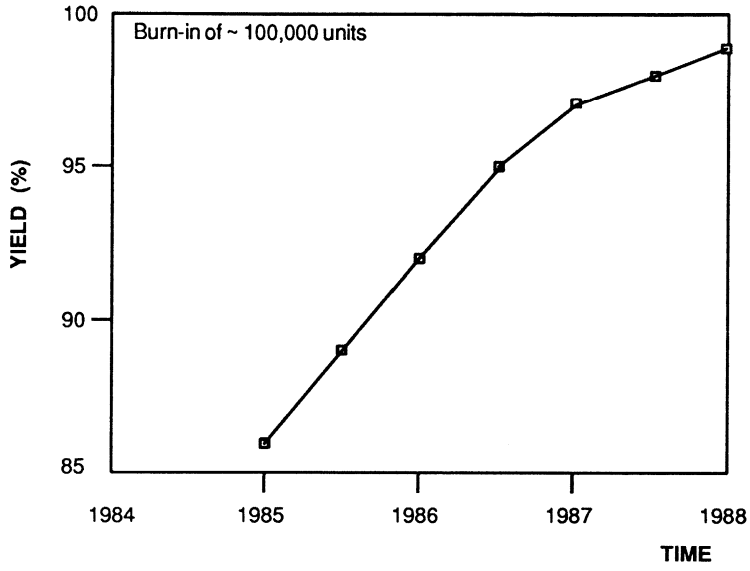


Figure 18

Burn-in yield vs time showing continued improvement over approximately 3 years

MIL-STD-883C Class B Screening

SCREEN	883C METHOD	CONDITIONS	SAMPLE SIZE
1. Internal Visual	2010	Condition A	100%
2. Stabilization Bake	1008	24 Hrs. @ 150°C	100%
3. Temp. Cycling	1010	-65°C to 150°C - 10 cycles	100%
4.Const. Acceleration	2001	Condition B (10,000 g) Y1 axis only	100%
5. Visual Inspection	-	-	100%
6. Burn-in Test	1015	160 Hrs. @ Tj = 150°C	100%
7. Post burn-in Electrical Test	-	Per datasheet spec.	100%
8. Percent defective (PDA)	-	5% allowed	All lots
9. Final Electrical Test	-	Per device specifications @ 25°C and temperature extremes.	100%
10. External Visual	2009	-	100%

Electrostatic Discharge (ESD) Sensitivity Test

The fanout buffer (10G011) was used as the ESD test vehicle to assess the ESD sensitivity of input and clamp pins to other electrodes within the IC. An ESD sensitivity tester ICMS 2400 was used to provide the Human Body Model circuit in accordance with MIL-STD-883C Method 3015.2 [7]. Functional tests were done on a Megatest Q2/52 after each pulse amplitude increase. Typical results are shown in Table 6.

Table 6

ESD Sensitivity Test

Fanout Buffer Lot 51300270

Parameter	Typical Values for Device Damage Positive Pulse	Negative Pulse
Input-V_{EE}	300V	1100V
Input-V_{DDL}	400V	500V
Input-V_{SS}	700V	800V
Input-(V_{ICL}-V_{ICH})	800V	900V
Input-All pins	600V	1200V
V_{ICL}-All Pins	1900V	1700V
V_{ICH}-All Pins	1200V	1100V
V_{LCL}-All Pins	300V	200V
V_{DCH}-All Pins	1200V	-
V_{DCL}-All Pins	2200V	-

CHAPTER X

RELIABILITY CONCLUSIONS

- The PicoLogic process is highly stable under thermal stress as shown by the results of 250°C (nitrogen purge) storage tests extending to 4 million device hours.
- The basic Schottky gate FET structure used in the PicoLogic IC shows extremely high parametric stability. This is based on 7500 hours of static life tests on discrete FETS.
- The reject rate after the Infant Mortality Screen for GaAs is comparable with those obtained in silicon ICs
- Life test results based on 4 million hours of tests, indicate that a reliability level of ≈ 25 FITS (@ Tj = 100°C) can be consistently obtained on production level PicoLogic and Nanoram parts.
- An activation energy of 1.4 eV has been arrived at based on multiple temperature life tests.
- No significant difference is observed in the failure rate of static life test compared to dynamic life test.
- Extremely good parametric stability has been seen on PicoLogic parts at the end-of-life testing.
- No dominant failure mechanism (related to GaAs MESFET process) has been observed to date.
- PicoLogic ICs are classified in category-A of ESD sensitivity (20-2000V) as per MIL-STD-883C Method 3015.2. Adequate ESD precautions are required when using PicoLogic parts in order to not limit the useful life.
- The PicoLogic family has demonstrated reliability levels comparable to equivalent silicon bipolar technologies.
- As the starting material (GaAs wafers) quality improves, and as the technology matures, an even higher reliability level can be expected from GigaBit GaAs ICs.

APPENDIX I

RECOMMENDATIONS FOR OPERATION AND HANDLING

Even the most reliable IC will fail in field use if subjected to certain stresses beyond the rated limits of the device. Such limitations which are not explicitly stated in the datasheet pertain to ESD, transient voltages, soldering heat, mechanical stress, etc. It is recommended that the user follow these recommendations to retain the inherent reliability of the ICs.

Electrostatic Damage

Measurements on PicoLogic devices are based on the human body model (as prescribed in MIL-STD-883C method 3015.2). They have shown sensitivity to ESD, starting from as low a voltage as 300V at the input leads. PicoLogic inputs are designed in such a way as to offer the utmost speed of operation. Hence, their ESD sensitivity is higher than other pins. However, corner pins have not shown any more susceptibility to ESD than the others.

GigaBit devices are packed in conductive foam in an anti-static box. The following handling precautions should be followed when using PicoLogic devices:

- Use conductive work satations (metalic or conductive plastic table tops connected to ground) to eliminate static build up.
- Control relative humidity to RH 50% or more. A small humidifier can be used to ensure this.
- Ground all handling personnel with a conductive bracelet or wrist strap through a 1Mohm resistor.
- Ground all test equipment properly and make sure that soldering iron tips are grounded.
- Avoid the use of dresses, smocks and shoes made from static generating materials such as nylon. Natural materials like cotton help reduce static build up.
- Devices should be in conductive carriers until thery are soldered. It is also desirable to store completed PCBs with the connectors wrapped in conductive foam in antistatic boxes.
- If vapor degreasers are used, the baskets must be grounded to an earth ground. Operators must also be grounded through adequate protective resistors.
- Compressed air or nitrogen lines used for cleaning must be fitted with static eliminators in the form of ionizers.
- Avoid use of solvent spray or aerosol cleaning unless the module or circuit is grounded fully.

Transient Voltages

Transient voltages in excess of the datasheet absolute maximum ratings may damage the devices. Hence, do not insert or remove the devices with power applied. Ensure that power supply transients that occur during power turn-on or off, do not exceed the absolute maximum ratings specified in the datasheet. Surface mount packages such as Leadless Chip Carriers (LCCs) have the adjacent leads very close to each other. Hence, extreme care needs to be taken when touching these leads with oscilloscope probes or test tips. Inadvertent shorting of two adjacent leads may lead to transient circuit conditions high enough to damage the device.

Soldering Heat

During soldering, no lead should be subjected to a temperature of 250°C for a period exceeding 10 seconds. Continuous exposure to temperatures in excess of 250° for periods ≥30 min. may change the parameters of the device. Please contact GigaBit Logic's applications department for special precautions necessary for using vapor-phase soldering.

Heatsinking

Adequate heatsinking should be provided for parts that are mounted on PCBs, so that the devices do not exceed the maximum temperature rating specified in the datasheet. A conductive epoxy such as Abelstik 36-2, 88-1 (or equivalent) or a lead tin solder may be used when mounting surface mount devices on PCBs. It should be kept in mind

that the heat path is from the bottom portion of GigaBit 36 I/O packages and from the top surface of GigaBit 40 I/O packages. For devices with higher power dissipation such as the MUX, DEMUX and 1K Static RAM additional heat removal in the form of a metal heat sink attached to the lid and forced air cooling are recommended. For additional information, please refer to GigaBit Logic's Application Note on "Thermal Management of PicoLogic and NanoRam GaAs Digital IC Families". [6]

Power Supply Sequencing

PicoLogic ICs are generally free from failure due to power supply sequencing. Neither latch up nor device breakdown occur due to the order in which voltages are applied. Generally, all supplies should be simultaneosuly applied. However, the presence of V_{SS} and the absence of V_{EE} will result in a substantial increase of I_{SS} and a corresponding increase in power dissipation during the period of time that V_{EE} is off. The potential decrease in reliability if these conditions were sustained for an extended period would in some cases justify the use of an interlock circuit. Such a circuit would sense the absence of V_{EE} and disconnect V_{SS}.

Unused Inputs

There is no reliability implication from leaving unused inputs open. However, it is advisable to return such inputs to V_{DDO} or V_{DDL} (nominally 0V) to set a logic high and to V_{SS} (-3.4V) or V_{TT} (-2V) to set a logic low. A 1K ohm current limiting resistor is recommended, in series between any power supply connected to an input, only when the input diode clamps V_{ICH} and V_{ICL} are used to clamp the input signal swing to a range tighter than V_{DDL} to V_{SS}. This will prevent excess current flow through the enabled clamp diodes. Unused outputs can always be left floating. [10]

Mechanical Stress

GigaBit Logic packages can withstand the normal mechanical stress of handling during mounting, soldering, etc. However, any torque applied in such a way as to bend the package will result in loss of hermeticity or breakage of the ceramic or glass sidewalls. Hence, avoid use of pliers to hold the part. **The leads of the GigaBit 36 I/O flat package should only be formed using a special tool designed for this purpose.**

Absolute Maximum Ratings

In addition to the precautions listed above, the user is advised to strictly follow the Absolute Maximum Ratings stated in the datasheets of each PicoLogic device. Exceeding any of these ratings, even for a short duration, may result in degradation of the part and impair its useful life.

Maximum Operating Temperature

The PicoLogic family is being characterized for operation over the case temperature range of T_C = -55 to +125°, as measured at case bottom. However, when using medium and higher power parts, it is recommended that the continuous operating die temperature be maintained ≤125°C, via proper thermal management. This is prescribed with the objective to guarantee a life time ≥100,000 hours.

APPENDIX II

EXPLANATION OF PROCESS CONTROL MONITOR (PCM) TEST PATTERNS

The PCM Test Patterns shown in Figure 4 of Chapter IV are comprised of the following test structures:

A) 50μm wide horizontal FET with backgate probe
B) 50μm wide horizontal saturated resistor
C) 50μm horizontal GaAs isolation gap
D) 50μm horizontal proton implanted isolation gap
E) Logic level shift diode
F) Input level shift diode
G) 50μm vertical gated active load with backgate probe
H) 50μm wide vertical saturated resistor
I) 50μm wide horizontal gated active resistor
J) TLM ohmic contact structure
K) N^- van der Pauw cross pattern
L) N^+ van der Pauw cross pattern

The basic parameters measured are as follows:

1. Ohmic Contact Resistivity (R_C)

The TLM pattern consists of four 50μm wide resistors (N^- and N^+ implants) with varying lengths (3, 6, 9, & 12μm). Resistances of these four resistors are measured by forcing a known current through the TLM pattern and measuring the voltage drop across each resistor. A linear least squares fit of these four values results in a plot similar to Figure 19. R_C is calculated as:

$$R_C = \frac{Y\,intercept}{2} \times \text{width in mm.}$$

2. Sheet Resistivity of N^-/N^+ Implants (R_O)

R_O is the slope of the line in Fig. 19 multiplied by width in μm.

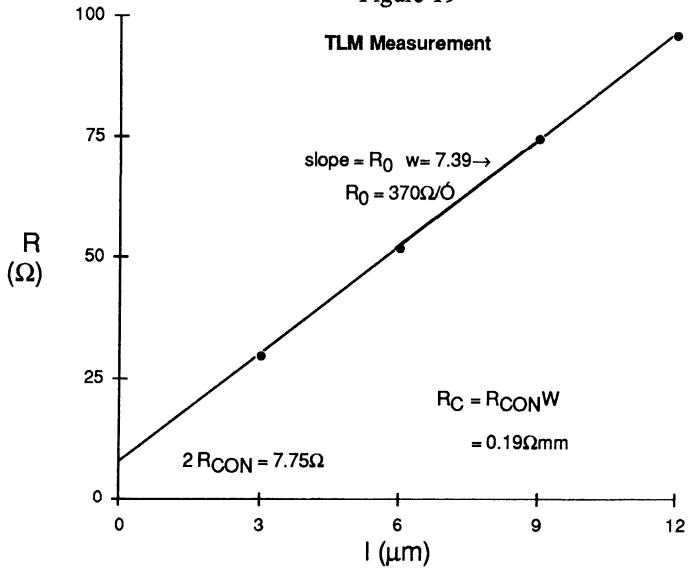
3. Sheet Resistivity of N^+ implant (R_SN^+) and N^- Implant (R_SN^-)

In the van der Pauw cross pattern, current is forced through one pair of arms while the voltage drop is measured across the opposite pair of arms. The sheet resistivity of the particular implant (N^+ or N^-) is given by the equation:

$$R_S = \frac{\pi}{\ln 2} \frac{V}{I}$$

The unit of R_SN^+ and R_SN^- is ohms/square.

Figure 19



4. Pinch-Off Voltage (V_P)

A 50μm wide horizontal FET is used to measure V_P, I_{DSS}, K, G_m, R_{ON}, and R_S. Gate voltage V_{GS} and drain-source current I_{DS} have a square law relationship given by the equation

$$I_{DS} = K (V_G - V_P)^2$$

where V_P = Pinch-Off Voltage of the FET

& K = The Proportionality Consta21

The drain is set at 2.5 volts and the source is set at 0 volts. V_{GS} is varied from ~-0.3 to -0.8 volts and I_{DS} is measured at each V_{GS}. A line is fit to the linear region of the plot of $\sqrt{I_{DS}}$ as a function of V_{GS}. (Please see Figure 20) The extrapolated value of the line to $\sqrt{I_{DS}} = 0$ is defined as V_P

5. Proportionality Constant (K)

In the plot of Figure 20, K is the slope of the line. The unit of K is $\mu A/V^2 \mu m$ since thse K value is normalized to a 1 micron wide FET.

6. Drain-Source Saturated Current (I_{DSS})

I_{DSS} is defined at the current (in mA) when V_{DS} = 2.5V and V_{GS} = 0 volts. (Please See Figure 21)

7. On-Resistance of the FET (R_{ON})

R_{ON} is defined as $\partial V_{DS}/\partial I_{DS}$ as I_{DS} goes to zero and is measured from the slope of the V_{DS} vs. I_{DS} curve for V_{GS} = 0 volts in the plot of Figure 19.

8. Transconductance (G_m)

The transconductance of the FET is defined as $G_m = \partial I_{DS}/\partial V_{GS}$ and is evaluated for D-MESFETs at V_{GS} = 0. Substituting into the equation of Section 4 yields $G_m = -2KV_P$. However, due to the non-linearity of the V_{GS} vs. $\sqrt{I_{DS}}$ plot, G_m is measured locally as the slope of the I_{DS} vs. V_{GS} plot at V_{GS} = 0. This value is normalized to a 1mm wide FET and designated G_m.

The unit is milliSiemens/mm where Siemens is the unit of conductance (current/voltage). Please See Figure 22.

Figure 20

V_{GS} vs. $\sqrt{I_{DS}}$

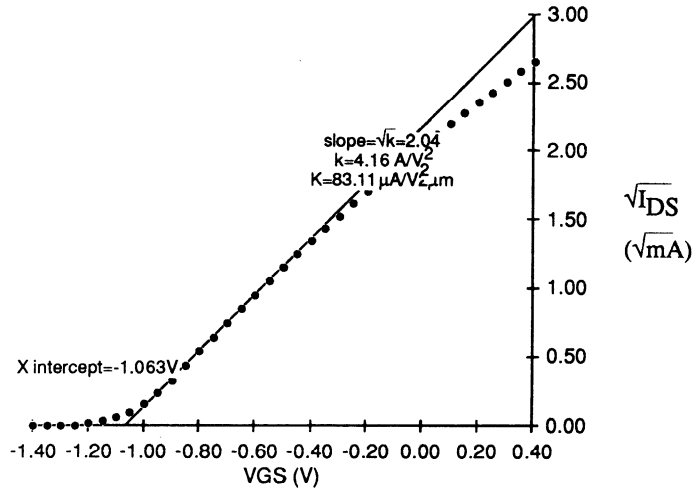


Figure 21

FET V_{DS} vs. I_{DS} Characteristics

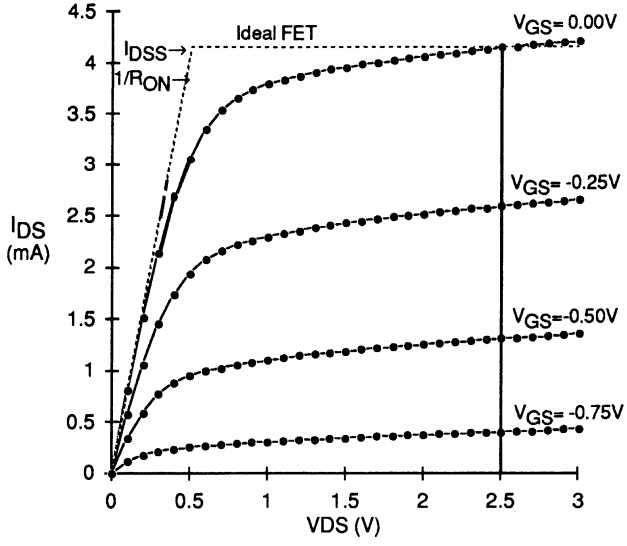
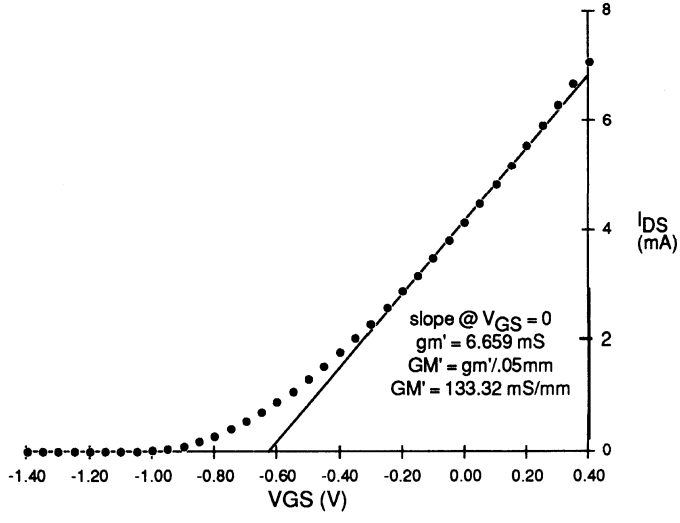


Figure 22

V_{GS} vs. I_{DS}



9. Source Resistance (R_S)

R_S is defined as $\partial V_{GS}/\partial I_{DS}$ where V_{DS} = 2.5V and I_{GS} = 100μA and is measured from the slope of the I_{DS} vs. V_{GS} plot under these conditions. R_S can be viewed as the cause of the deviation of the FET from the ideal linear relationship. (Please see Figure 23)

10. Backgating (B_G)

Backgating is the percentage reduction in the drain current when a negative bias is applied to an ohmic contact 10μm away from a conducting FET. Structure A of Figure 4 (FET with backgate probe) is used for this measurement. BG is the ratio in percentage of I_{DSS} at V_{BG} = 0V to I_{DSS} at V_{BG} = -5V. This is expressed by the following equation:

$$\frac{I_{DSS} @ V_{BG} = -5V}{I_{DSS} @ V_{BG} = 0V} \times 100\%$$

11. Isolation ISO1 and ISO2

ISO1 is the leakage current at 2 volts between two 50μm wide ohmic contact regions 3μm apart with a 1.6μm wide strip of proton implanted substrate between them.

ISO2 is measured on the same pattern as the above, but without any proton implant.

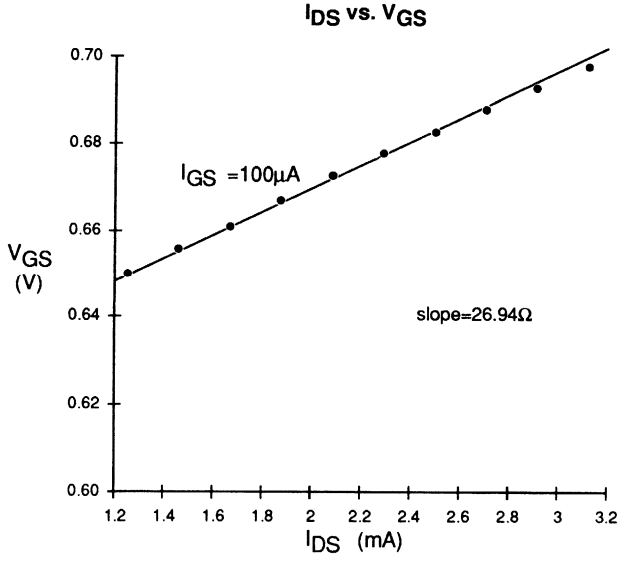
12. Forward Voltage V_F

V_F is defined as the voltage across the diode when the current reaches 160μA. It is measured on the logic level shift diode patterns as well as the input level shift diode patterns.

13. Breakdown Voltage V_{BR}

V_{BR} is defined as the reverse voltage across the diode that is required to attain a reverse current of 2μA.

Figure 23



14. Ideality Factor N

The current flowing through a Schottky diode under forward bias can be expressed in terms of the current density through the barrier region by the equation

$$J = J_S \exp (qV/NK_BT)$$

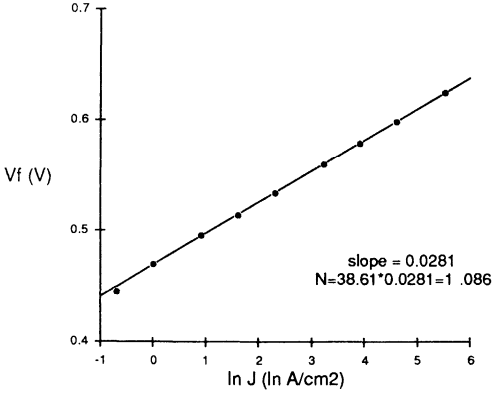
where J_S is the saturation current density, q is the electron charge, V is the applied voltage, K_B is Boltzman's constant, T is the ambient temperature in Kelvin and N is the ideality factor. N can be expressed as the equation

$$N = (q/K_BT) (\partial V/\partial \ln J)$$

N is a dimensionless value and is computed from the slope of the plot of V as a funciton of ln J at currents in the range 10nA to 5μA as shown in Figure 24.

Figure 24

ln J vs. V_F



APPENDIX III

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2. R. C. Eden, A. R. Livingston and B. M. Welch, "Integrated Circuits: The Case for Gallium Arsenide", IEEE Spectrum, December 1983.

3. R. C. Eden, B. M. Welch et al., "The Prospect for Ultra High-Speed VLSI GaAs Digital Logic", IEEE Journal of Solid State Circuits, Vol. SC-14, No. 2, April 1979.

4. B. M. Welch, Y. D. Shen et al, "LSI Processing Technology for Planar GaAs Integrated Circuits", IEEE Transactions on Electron Devices, Vol. ED-27, No. 6, June 1980.

5. T. Gheewala and D. MacMillan, "High-Speed GaAs Logic Systems Require Special Packaging", EDN, May 17, 1984.

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8. W. J. Dixon and F. J. Massey, "Introduction to Statistical Analysis", Third Edition, McGraw Hill, New York, 1969.

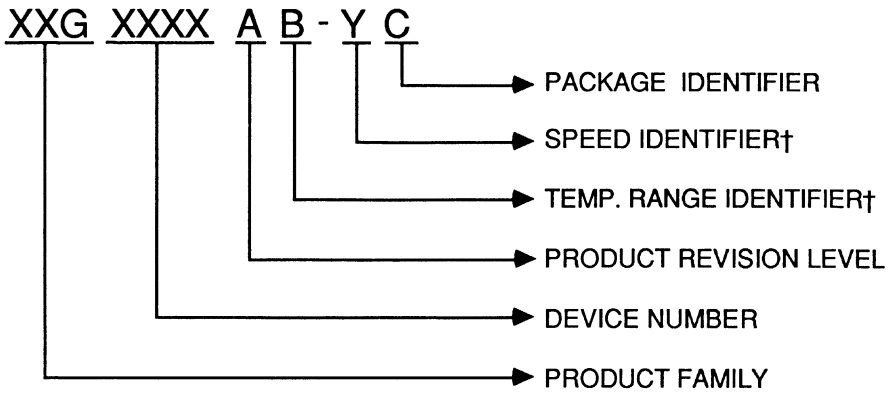
9. N. G. Einspruch (Editor), "VLSI Handbook", Academic Press Inc., Orlando, Florida, 1985 (chapter 32 on radiation effects and radiation hardening of VLSI circuits).

10. J. H. Kemps, "The Operation and Application of PicoLogic GaAs Integrated Circuits", Application Note 1, GigaBit Logic, Newbury Park, CA.

ORDERING INFORMATION AND PACKAGE MECHANICAL DRAWINGS

TABLE OF CONTENTS

CIRCUIT PART NUMBER DESCRIPTION



† Absence of character indicates nominal.

PRODUCT FAMILY

10G= PicoLogic™ Family
12G= NanoRam™ Family
14G= NanoRom™ Family
16G= Analog and Interface Products
80G= ASIC Products
90G= Prototyping and Support Products

PACKAGE IDENTIFIER

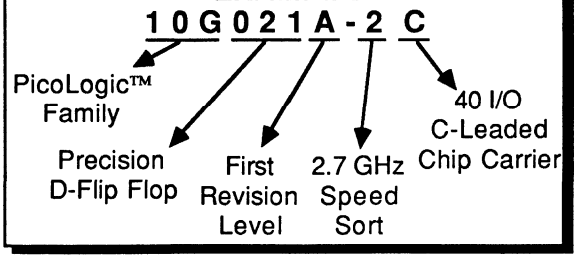
C1 ····· 68 I/O Leaded Chip Carrier
C ····· 40 I/O C-Leaded Chip Carrier
L ····· 40 I/O Leadless Chip Carrier
F ····· 36 I/O Flat Package
L36* ····· 36 I/O Leadless Chip Carrier
H ····· Hybrid Package
X ····· Unpackaged Die

*Note: Characters "36" not marked on package.

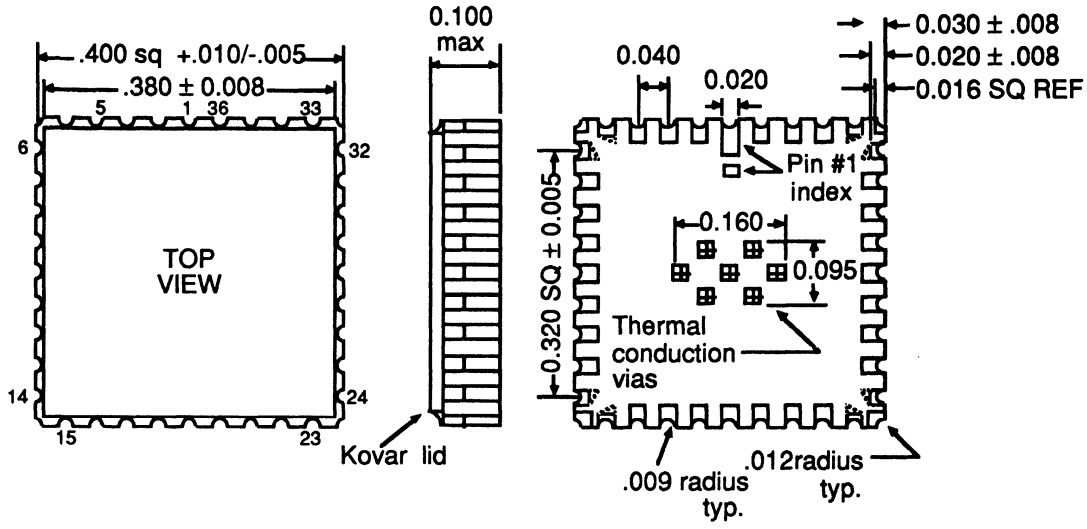
EXTENDED TEMPERATURE IDENTIFIER

K = -40°C to + 100°C
M = -55°C to + 125°C

EXAMPLE

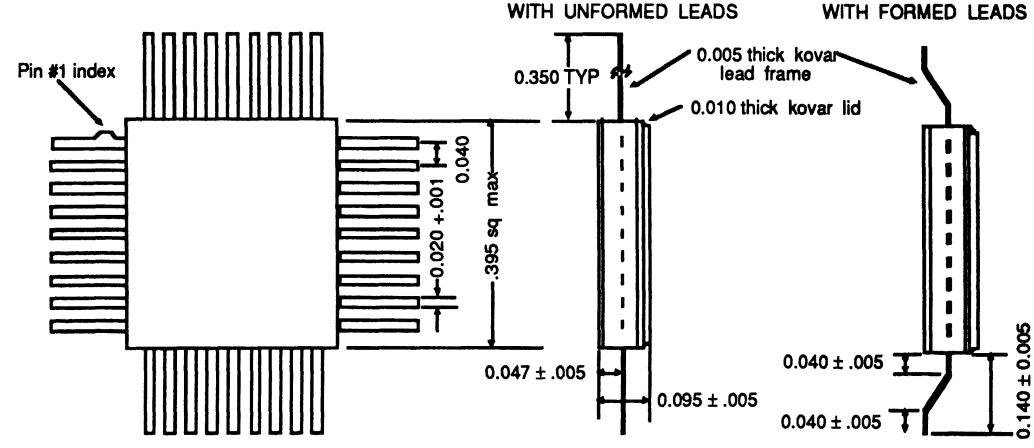


36 I/O LEADLESS CHIP CARRIER (TYPE "L36")

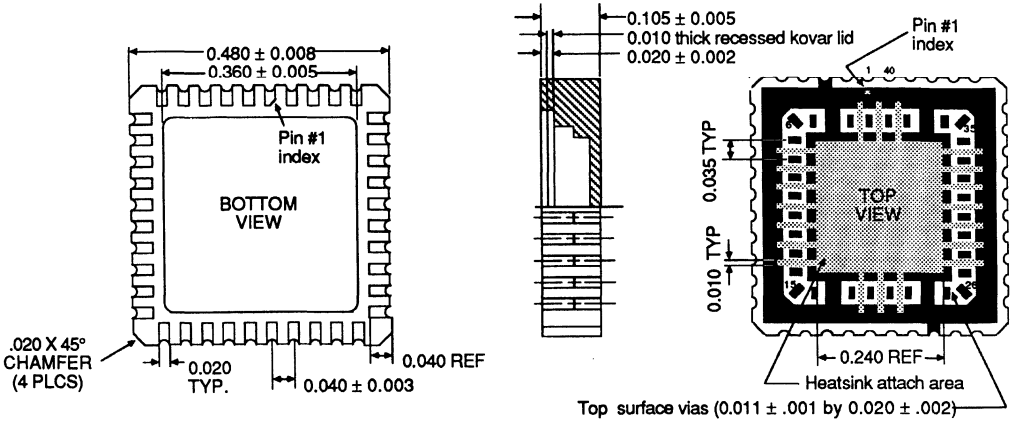


NOTES:
1) The package bottom thermal vias, top lid surface and 4 metallized corner castellations (when present) are all at Vss potential.
2) All dimensions in inches.
3) Plin #1 identifier may be an elongated pad or small, square gray marker.

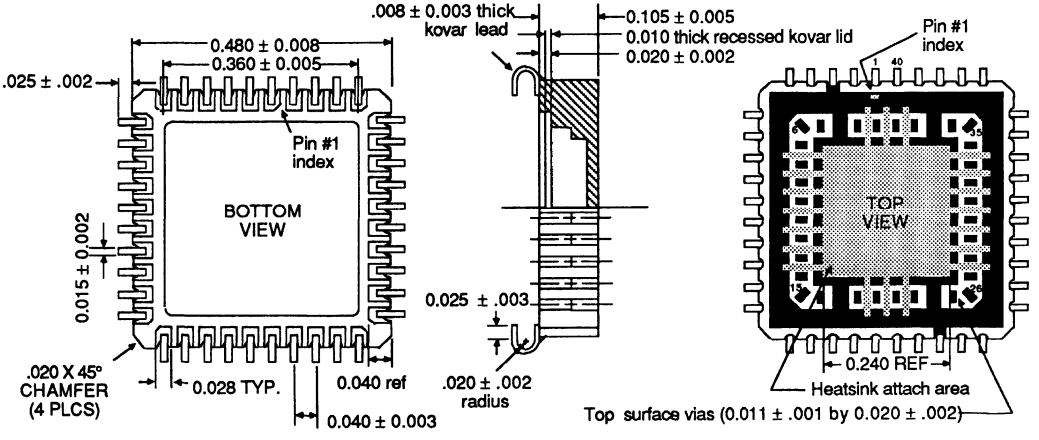
36 I/O LEAD FLATPACK (TYPE "F")



40 I/O LEADLESS CHIP CARRIER (TYPE "L")



40 I/O "C"-LEADED CHIP CARRIER (TYPE "C")



NOTES:

(1) Footprint is JEDEC standard outline.
(2) Top surface vias (for terminating resistors and decoupling capacitors) are not available on pins 3,4,17, 18, 23,24,37 and 38. The diagonal vias are numbered.
(3) Top surface metal (not including vias) and pins 3 and 23 are fixed at VTT potential.
(4) Recommended top surface chip resistors are 0.040 long by 0.020 wide by 0.010 thick typ, 100 mw min. nominal power rating (Mini-Systems MSR-21 or equivalent.)
(5) Recommended top surface chip capacitors are 0.040 long by 0.030 wide by 0.020 thick typ, 25V VDCW, 1000 pf, min. (Johanson R09 case or equivalent).
(6) Recommended heatsinks are GBL P/Ns 90GHS40A and 90GHS40B.
(7) Thermally conductive, electrically non-conductive epoxy is recommended for heatsink attachment (Ablestick 789-4 or 561K, or Thermalloy Thermalbond™ or equivalent.)
(8) "L" and "C" packages are dimensionally identical except for contact finger width.
(9) All dimensions in inches.

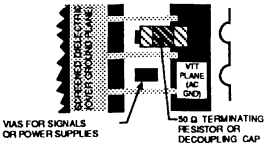
TOP SURFACE LEGEND:

Metalized Ceramic.....

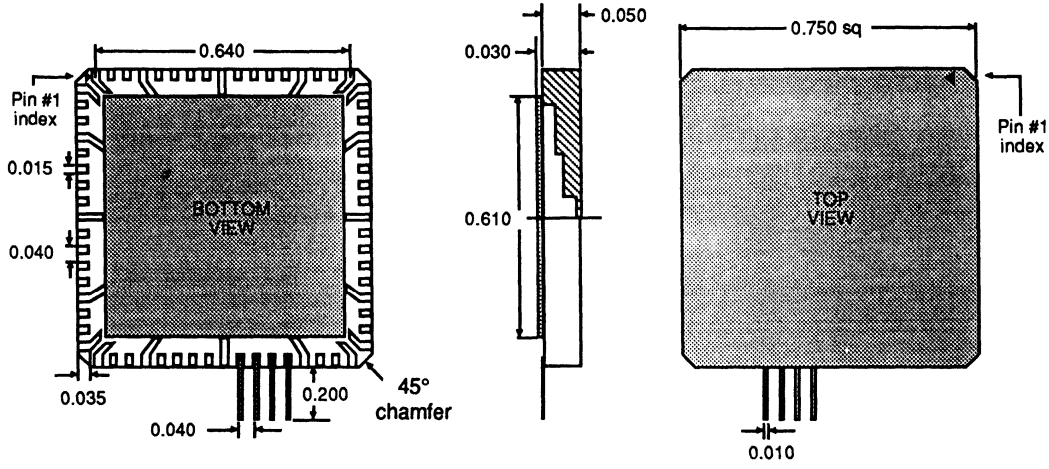
Screened Dielectric.....

Bare Ceramic.....

Top Surface Terminating/Decoupling Detail



68 PIN CHIP CARRIER (C1)



1) All dimensions in inches.
2) Package lid, bottom surface and pins 4, 9, 14, 21, 26, 31, 38, 43, 48, 55, 60, 65 are at common potential (system ground).

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